

AM26LS32AC, AM26LS33AC, AM26LS32AM, AM26LS33AM QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS115C – OCTOBER 1980 – REVISED APRIL 2000

- **AM26LS32A Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B, EIA/TIA-423-B, and ITU Recommendations V.10 and V.11**
- **AM26LS32A Has ± 7 -V Common-Mode Range With ± 200 -mV Sensitivity**
- **AM26LS33A Has ± 15 -V Common-Mode Range With ± 500 -mV Sensitivity**
- **Input Hysteresis . . . 50 mV Typical**
- **Operates From a Single 5-V Supply**
- **Low-Power Schottky Circuitry**
- **3-State Outputs**
- **Complementary Output-Enable Inputs**
- **Input Impedance . . . 12 k Ω Min**
- **Designed to Be Interchangeable With Advanced Micro Devices AM26LS32™ and AM26LS33™**

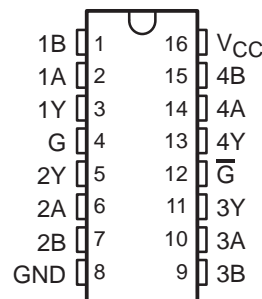
description

The AM26LS32A and AM26LS33A devices are quadruple differential line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that, if the inputs are open, the outputs are always high.

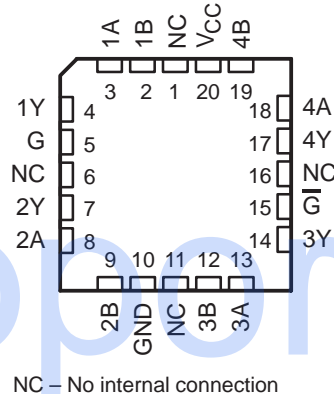
Compared to the AM26LS32 and the AM26LS33, the AM26LS32A and AM26LS33A incorporate an additional stage of amplification to improve sensitivity. The input impedance has been increased, resulting in less loading of the bus line. The additional stage has increased propagation delay; however, this does not affect interchangeability in most applications.

The AM26LS32AC and AM26LS33AC are characterized for operation from 0°C to 70°C. The AM26LS32AM and AM26LS33AM are characterized for operation over the full military temperature range of -55°C to 125°C.

AM26LS32AC, AM26LS33AC . . . D OR N PACKAGE
AM26LS32AM, AM26LS33AM . . . J PACKAGE
(TOP VIEW)



AM26LS32AM, AM26LS33AM . . . FK PACKAGE
(TOP VIEW)



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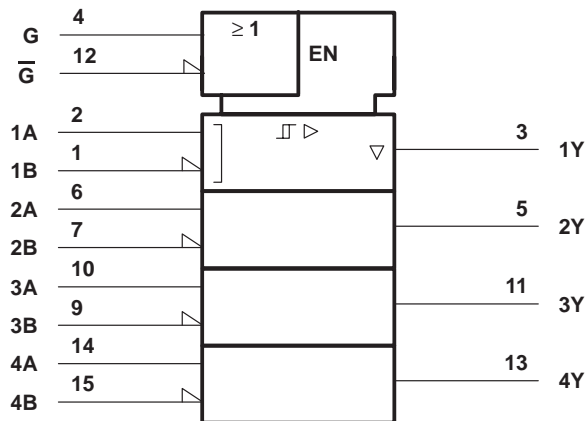
SLLS115C – OCTOBER 1980 – REVISED APRIL 2000

FUNCTION TABLE
(each receiver)

DIFFERENTIAL A – B	ENABLES		OUTPUT Y
	G	\overline{G}	
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT-} \leq V_{ID} \leq V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

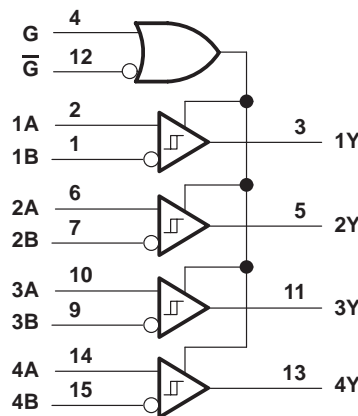
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

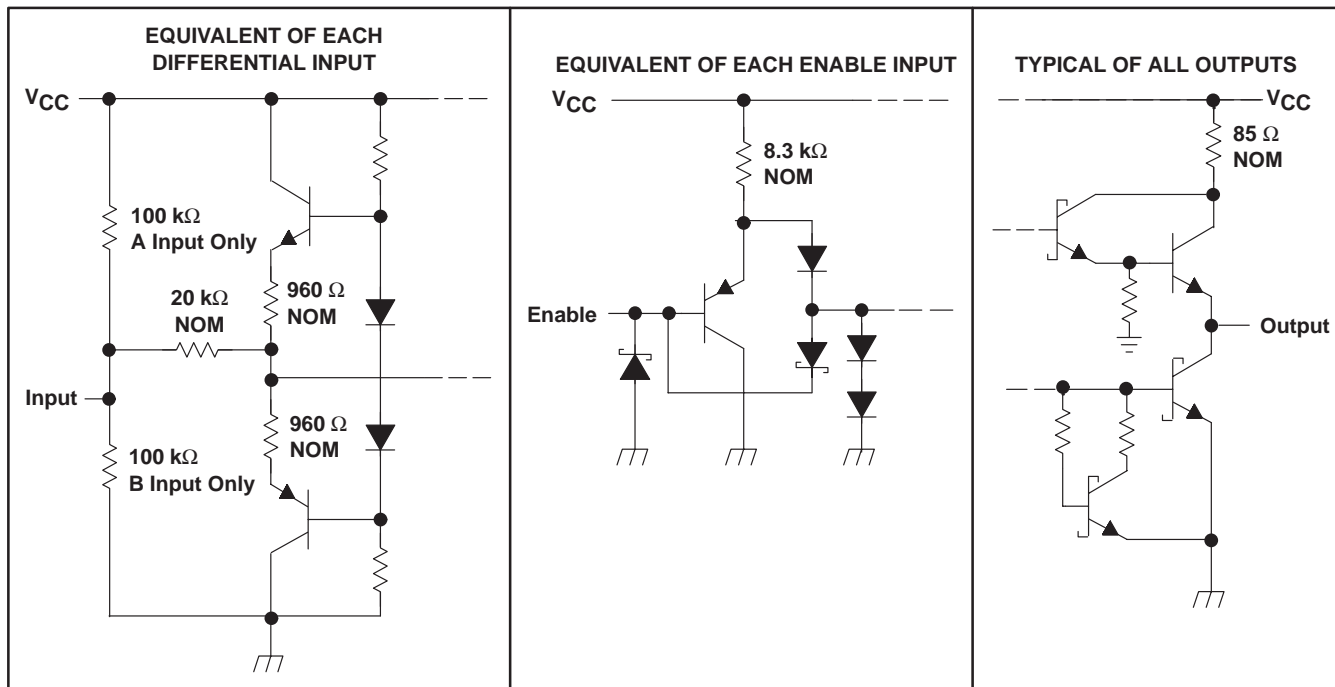
logic diagram (positive logic)



AM26LS32AC, AM26LS33AC, AM26LS32AM, AM26LS33AM QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS115C – OCTOBER 1980 – REVISED APRIL 2000

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I : Any differential input	± 25 V
Other inputs	7 V
Differential input voltage, V_{ID} (see Note 2)	± 25 V
Continuous total power dissipation	See Dissipation Rating Table
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
N package	67°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Case temperature for 60 seconds, T_C : FK package	260°C
Storage temperature range, T_{Stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
 2. Differential voltage values are at the noninverting (A) input terminals with respect to the inverting (B) input terminals.
 3. The package thermal impedance is calculated in accordance with JESD 51.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW

AM26LS32AC, AM26LS33AC, AM26LS32AM, AM26LS33AM QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS115C – OCTOBER 1980 – REVISED APRIL 2000

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	AM26LS32AC, AM26LS33AC	4.75	5	5.25	V
	AM26LS32AM, AM26LS33AM	4.5	5	5.5	
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}		0.8			V
Common-mode input voltage, V_{IC}	AM26LS32AC, AM26LS32AM	± 7			V
	AM26LS33AC, AM26LS33AM	± 15			
High-level output current, I_{OH}		-440			μA
Low-level output current, I_{OL}		8			mA
Operating free-air temperature, T_A	AM26LS32AC, AM26LS33AC	0			$^{\circ}C$
	AM26LS32AM, AM26LS33AM	-55			

electrical characteristics over recommended ranges of V_{CC} , V_{IC} , and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$V_O = V_{OHmin}$, $I_{OH} = -440 \mu A$	AM26LS32A			0.2	V
			AM26LS33A			0.5	
V_{IT-}	Negative-going input threshold voltage	$V_O = 0.45 V$, $I_{OL} = 8 mA$	AM26LS32A			-0.2‡	V
			AM26LS33A			-0.5‡	
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				50		mV
V_{IK}	Enable input clamp voltage	$V_{CC} = MIN$,	$I_I = -18 mA$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = MIN$, $V_{ID} = 1 V$, $V_{I(G)} = 0.8 V$, $I_{OH} = -440 \mu A$	AM26LS32AC AM26LS33AC			2.7	V
			AM26LS32AM AM26LS33AM			2.5	
V_{OL}	Low-level output voltage	$V_{CC} = MIN$, $V_{ID} = -1 V$, $V_{I(G)} = 0.8 V$	$I_{OL} = 4 mA$			0.4	V
			$I_{OL} = 8 mA$			0.45	
I_{OZ}	Off-state (high-impedance state) output current	$V_{CC} = MAX$	$V_O = 2.4 V$			20	μA
			$V_O = 0.4 V$			-20	
I_I	Line input current	$V_I = 15 V$,	Other input at -10 V to 15 V			1.2	mA
		$V_I = -15 V$,	Other input at -15 V to 10 V			-1.7	
$I_{I(EN)}$	Enable input current	$V_I = 5.5 V$				100	μA
I_{IH}	High-level enable current	$V_I = 2.7 V$				20	μA
I_{IL}	Low-level enable current	$V_I = 0.4 V$				-0.36	mA
r_I	Input resistance	$V_{IC} = -15 V$ to 15 V,	One input to ac ground	12	15		k Ω
I_{OS}	Short-circuit output current§	$V_{CC} = MAX$		-15		-85	mA
I_{CC}	Supply current	$V_{CC} = MAX$,	All outputs disabled		52	70	mA

† All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$, and $V_{IC} = 0$.

‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

§ Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.



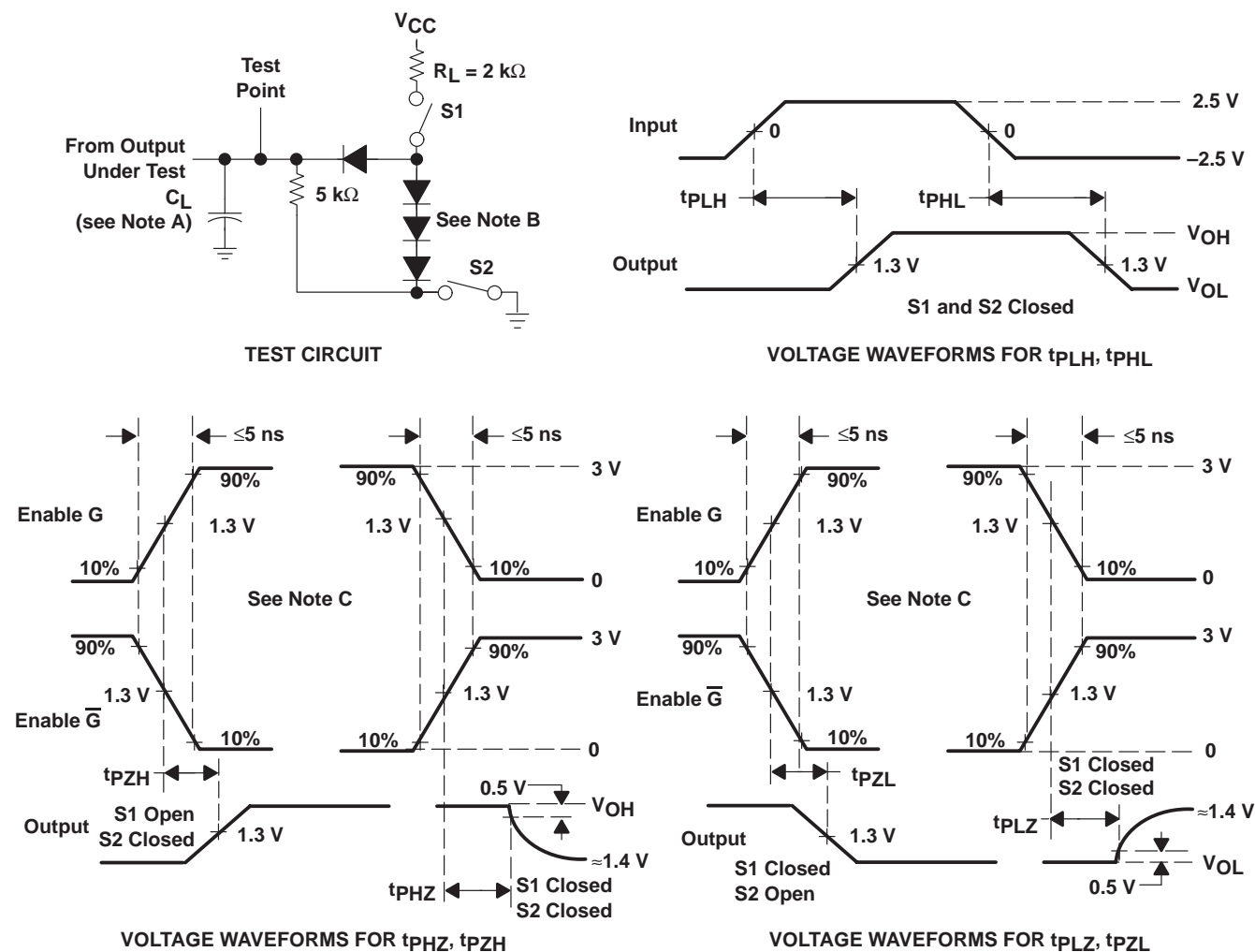
AM26LS32AC, AM26LS33AC, AM26LS32AM, AM26LS33AM QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS115C – OCTOBER 1980 – REVISED APRIL 2000

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15\text{ pF}$, See Figure 1		20	35	ns
t_{PHL} Propagation delay time, high-to-low-level output	$C_L = 15\text{ pF}$, See Figure 1		22	35	ns
t_{PZH} Output enable time to high level	$C_L = 15\text{ pF}$, See Figure 1		17	22	ns
t_{PZL} Output enable time to low level	$C_L = 15\text{ pF}$, See Figure 1		20	25	ns
t_{PHZ} Output disable time from high level	$C_L = 5\text{ pF}$, See Figure 1		21	30	ns
t_{PLZ} Output disable time from low level	$C_L = 5\text{ pF}$, See Figure 1		30	40	ns

PARAMETER MEASUREMENT INFORMATION



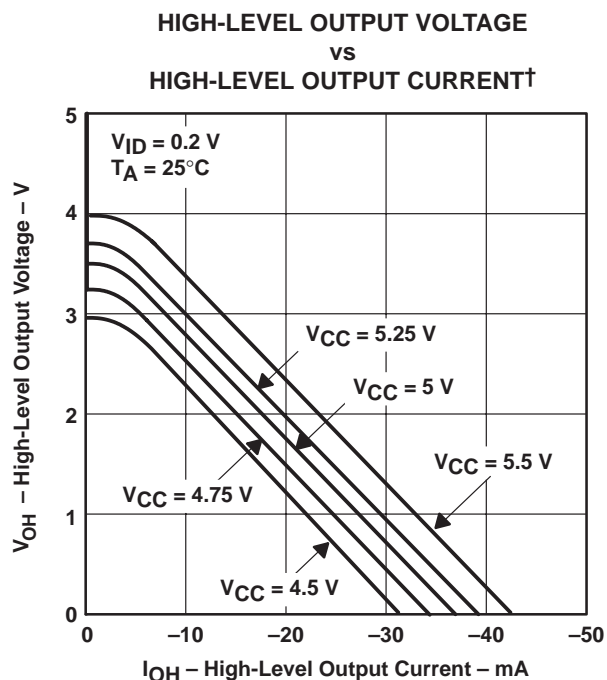
- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Enable G is tested with \bar{G} high; \bar{G} is tested with G low.

Figure 1

AM26LS32AC, AM26LS33AC, AM26LS32AM, AM26LS33AM QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS115C – OCTOBER 1980 – REVISED APRIL 2000

TYPICAL CHARACTERISTICS



† $V_{CC} = 5.5$ V and $V_{CC} = 4.5$ V applies to M-suffix devices only.

Figure 2

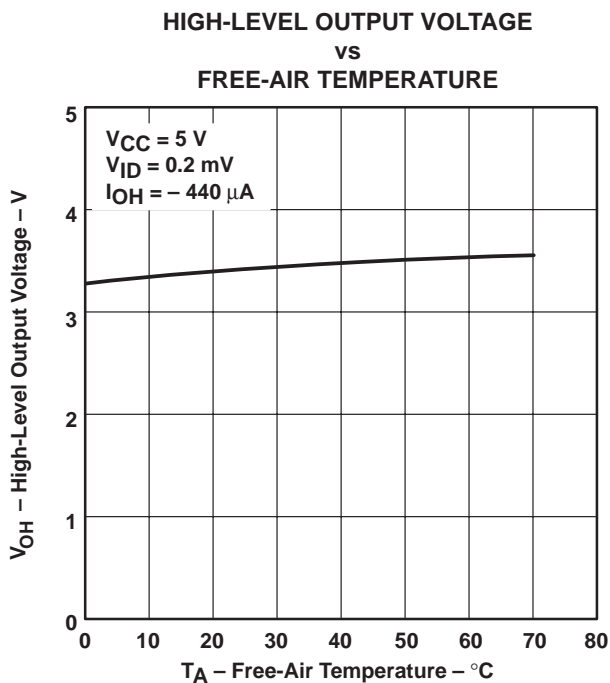


Figure 3

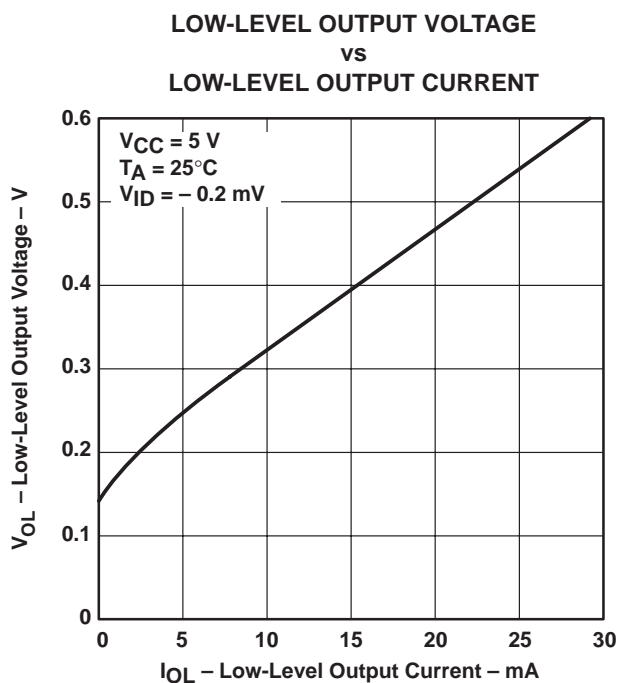


Figure 4

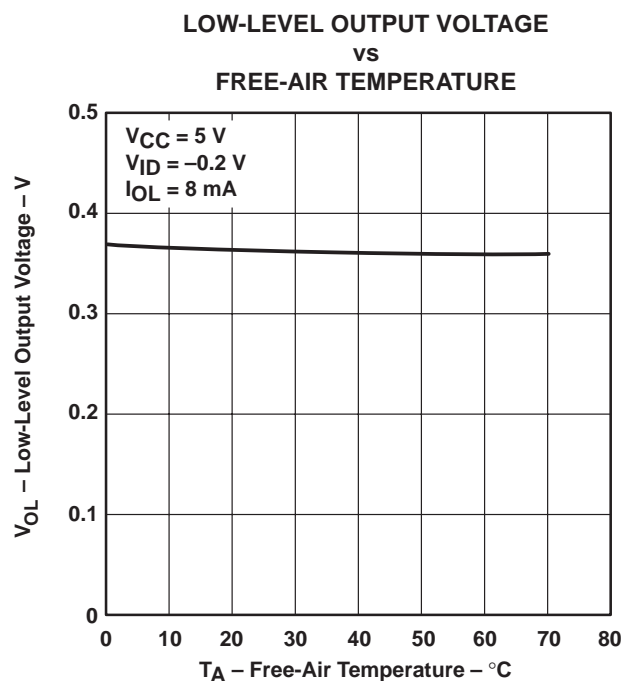


Figure 5



TYPICAL CHARACTERISTICS

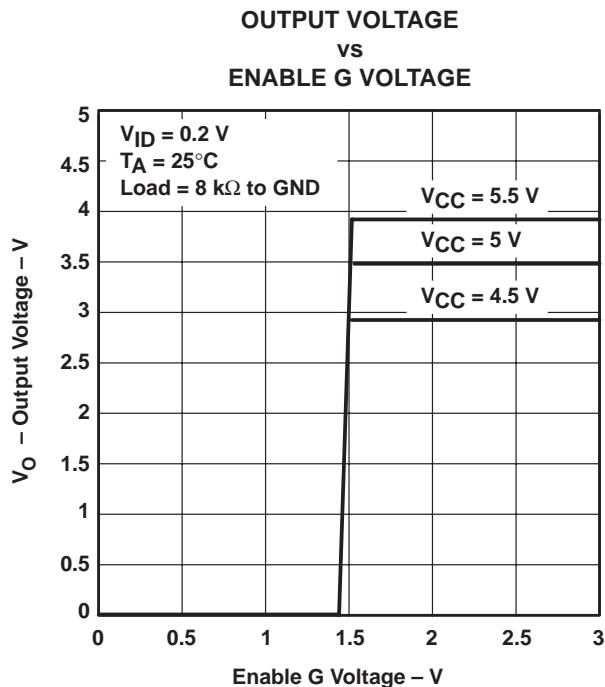


Figure 6

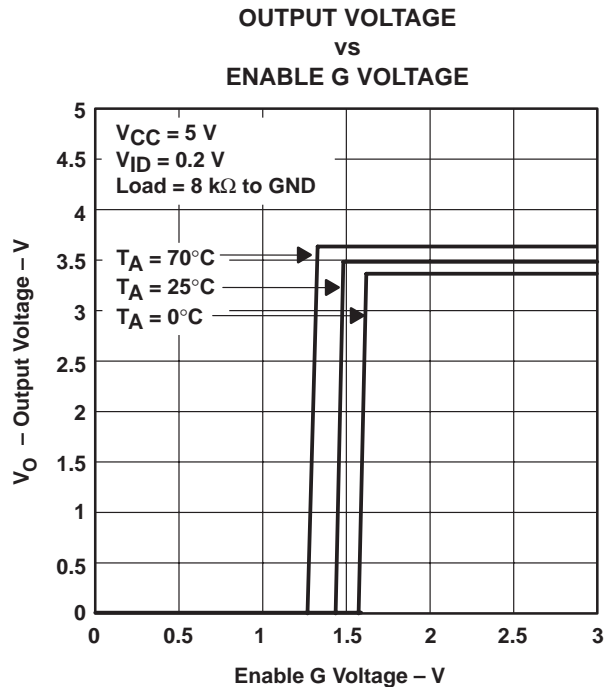


Figure 7

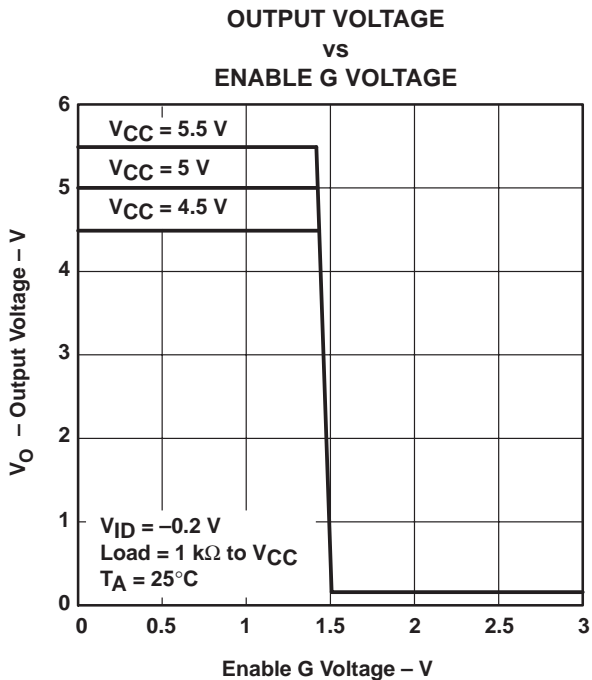


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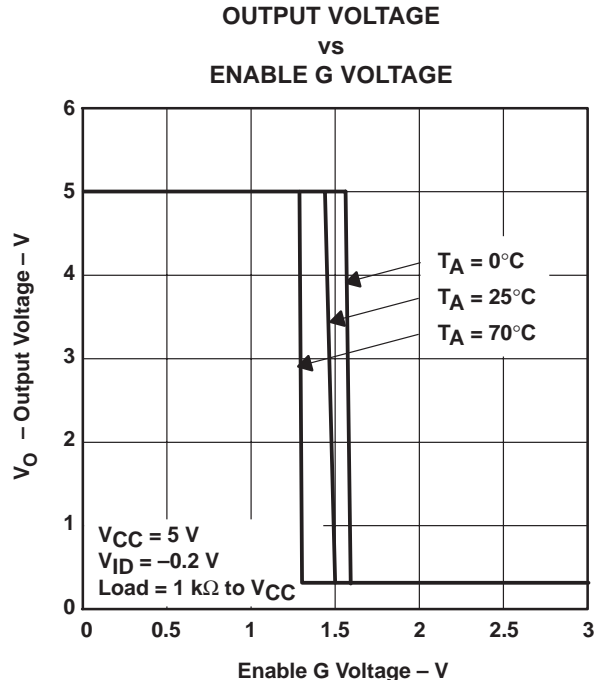
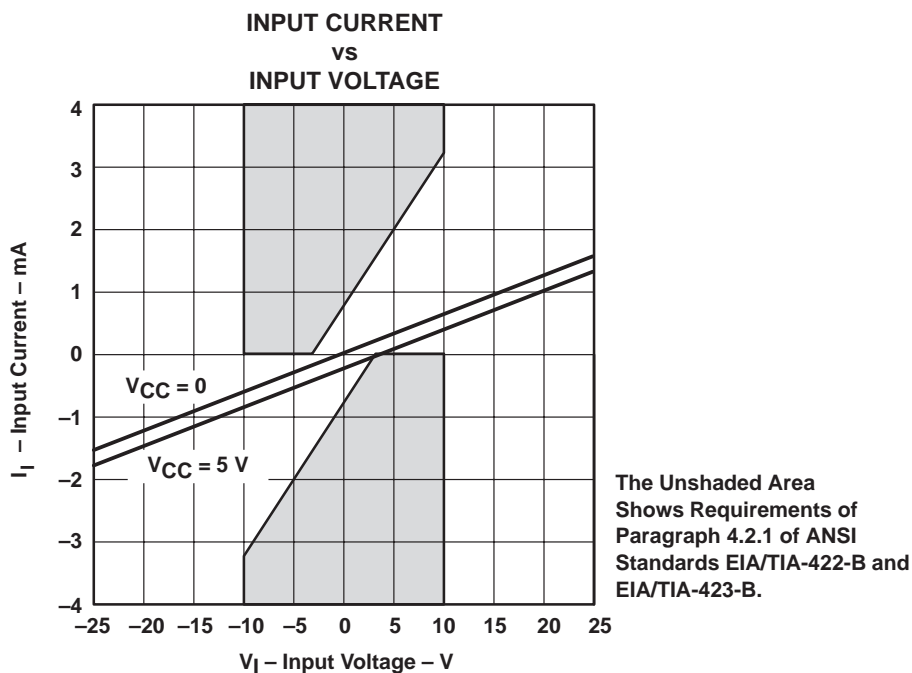
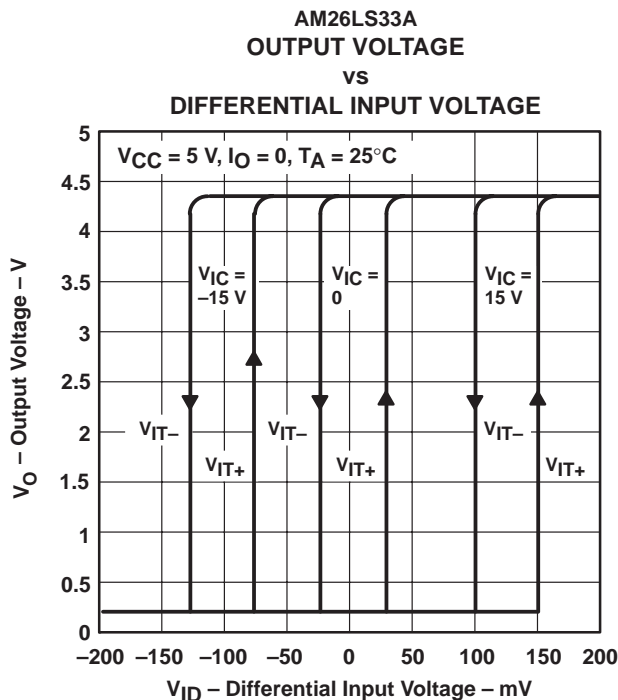
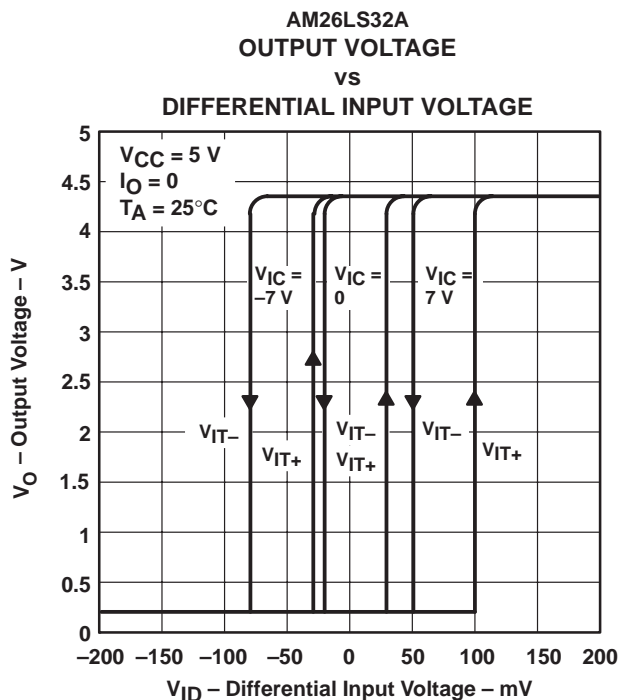


Figure 9

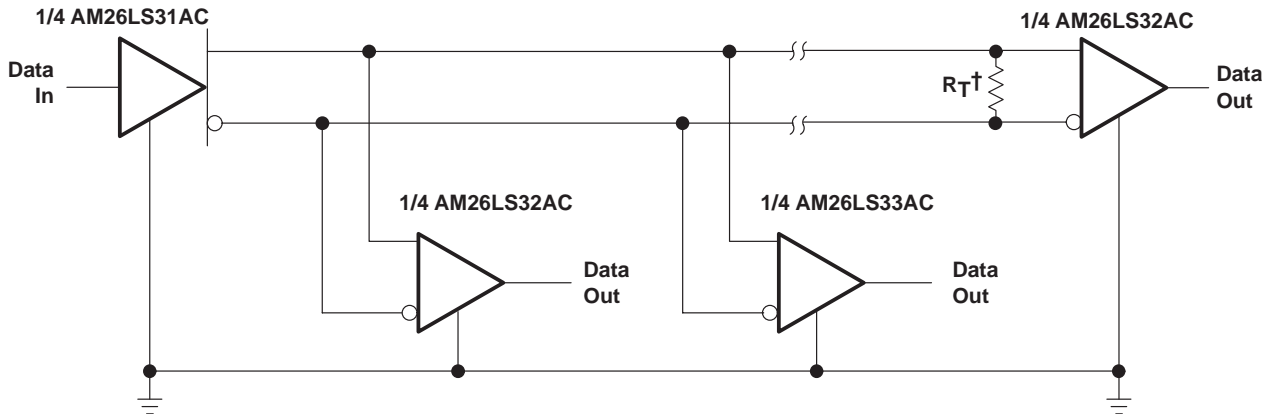
AM26LS32AC, AM26LS33AC, AM26LS32AM, AM26LS33AM QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS115C – OCTOBER 1980 – REVISED APRIL 2000

TYPICAL CHARACTERISTICS



APPLICATION INFORMATION



† R_T equals the characteristic impedance of the line.

Figure 13. Circuit With Multiple Receivers

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