

SECTION 5

SCR CHARACTERISTICS

Edited and Updated

SCR TURN-OFF CHARACTERISTICS

In addition to their traditional role of power control devices, SCRs are being used in a wide variety of other applications in which the SCR's turn-off characteristics are important. As in example — reliable high frequency inverters and converter designs (<20 kHz) require a known and controlled circuit-commutated turn-off time (t_q). Unfortunately, it is usually difficult to find the turn-off time of a particular SCR for a given set of circuit conditions.

This section discusses t_q in general and describes a circuit capable of measuring t_q . Moreover, it provides data and curves that illustrate the effect on t_q when other parameters are varied, to optimize circuit performance.

SCR TURN-OFF MECHANISM

The SCR, being a four layer device (P-N-P-N), is represented by the two interconnected transistors, as shown in Figure 5.1. This regenerative configuration allows the device to turn on and remain on when the gate trigger is removed, as long as the loop gain criteria is satisfied; i.e., when the sum of the common base current gains (α) of both the equivalent NPN transistor and PNP transistor, exceed one. To turn off the SCR, the loop gain must be brought below unity, whereby the on-state principal current (anode current i_T) limited by the external circuit impedance, is reduced below the holding current (I_H). For ac line applications, this occurs automatically during the negative going portion of the waveform. However, for dc applications (inverters, as an example), the anode current must be interrupted or diverted; (diversion of the anode current is the technique used in the t_q test fixture described later in this application note).

SCR TURN-OFF TIME t_q

Once the anode current in the SCR ceases, a period of time must elapse before the SCR ceases to block a forward voltage. This period is the SCR's turn-off time, t_q , and is dependent on temperature, forward current, and other parameters. The turn-off time phenomenon can be understood by considering the three junctions that make up the SCR. When the SCR is in the conducting state, each of the three junctions is forward biased and the N and P regions (base regions) on either side of J2 are heavily saturated with holes and electrons (stored charge). In order to turn off the SCR in a minimum amount of time, it

is necessary to apply a negative (reverse) voltage to the device anode, causing the holes and electrons near the two end junctions, J1 and J3, to diffuse to these junctions. This causes a reverse current to flow through the SCR. When the holes and electrons near junctions J1 and J3 have been removed, the reverse current will cease and junctions J1 and J3 will assume a blocking state. However, this does not complete the recovery of the SCR since a high concentration of holes and electrons still exist near the center junction, J2. This concentration decreases by the recombination process and is largely independent of the external circuit. When the hole and electron concentration near junction J2 has reached some low value, junction J2 will assume its blocking condition and a forward voltage can, after this time, be applied without the SCR switching back to the conduction state.

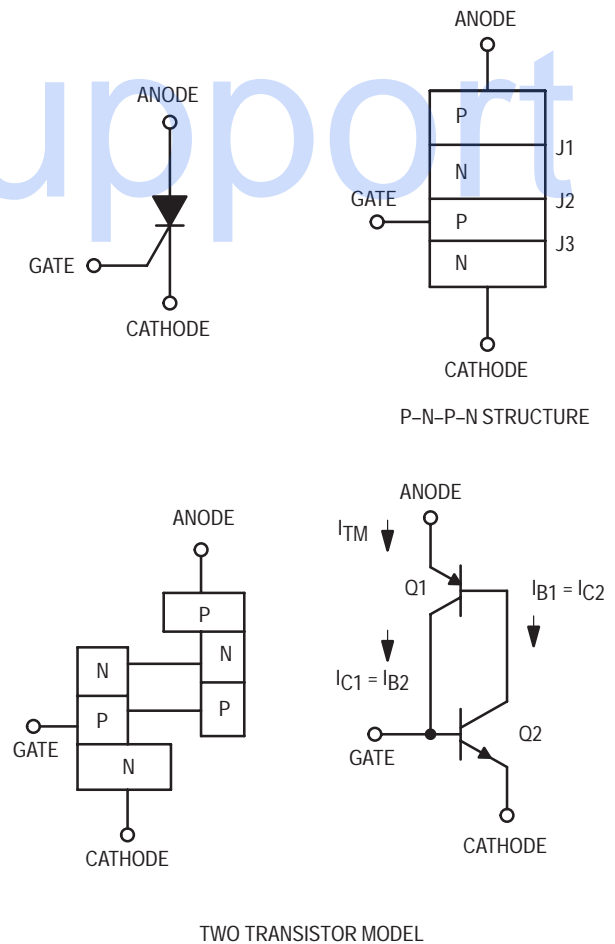


Figure 5.1. Two Transistor Analogy of an SCR

t_q MEASUREMENT

When measuring SCR turn-off time, t_q , it is first necessary to establish a forward current for a period of time long enough to ensure carrier equilibrium. This must be specified, since I_{TM} has a strong effect on the turn-off time of the device. Then, the SCR current is reversed at a specified di/dt rate, usually by shunting the SCR anode to some negative voltage through an inductor. The SCR will then display a “reverse recovery current,” which is the charge clearing away from the junctions. A further waiting time must then elapse while charges recombine, before a forward voltage can be applied. This forward voltage is ramped up a specified dv/dt rate. The dv/dt delay time is reduced until a critical point is reached where the SCR can no longer block the forward applied voltage ramp. In effect, the SCR turns on and consequently, the ramp voltage collapses. The elapsed time between this critical point and the point at which the forward SCR current passes through zero and starts to go negative (reverse recovery phase), is the t_q of the SCR. This is illustrated by the waveforms shown in Figure 5.2.

t_q GENERAL TEST FIXTURE

The simplified circuit for generating these waveforms is schematically illustrated in Figure 5.3. This circuit is implemented with as many as eight transformers including variacs, and in addition to being very bulky, has been known to be troublesome to operate. However, the configuration is relevant and, in fact, is the basis for the design, as described in the following paragraphs.

t_q TEST FIXTURE BLOCK DIAGRAMS AND WAVEFORMS

The block diagram of the t_q Test Fixture, illustrated in Figure 5.4, consists of four basic blocks: A Line

Synchronized Pulse Generator establishes system timing; a Constant Current Generator (variable in amplitude) powers the Device Under Test (DUT); a di/dt Circuit controls the rate of change of the SCR turn-off current; and the dv/dt Circuit reapplies a controlled forward blocking voltage. Note from the waveforms illustrated that the di/dt circuit, in parallel with the DUT, diverts the constant current from the DUT to produce the described anode current I_{TM} .

t_q TEST FIXTURE CHARACTERISTICS

The complete schematic of the t_q Test Fixture and the important waveforms are shown in Figures 5.5 and 5.6, respectively.

A CMOS Gate is used as the Line Synchronized Pulse Generator, configured as a wave shaping Schmitt trigger, clocking two cascaded monostable multivibrators for delay and pulse width settings (Gates 1C to 1F). The result is a pulse generated every half cycle whose width and position (where on the cycle it triggers) are adjustable by means of potentiometers R2 and R3, respectively. The output pulse is normally set to straddle the peak of the ac line, which not only makes the power supplies more efficient, but also allows a more consistent oscilloscope display. This pulse shown in waveform A of Figure 5.6 initiates the t_q test, which requires approximately 0.5 ms to assure the device a complete turn on. A fairly low duty cycle results, (approximately 5%) which is important in minimizing temperature effects. The repetitive nature of this test permits easy oscilloscope viewing and allows one to readily “walk in” the dv/dt ramp. This is accomplished by adjusting the appropriate potentiometer (R7) which, every 8.33 ms (every half cycle) will apply the dv/dt ramp at a controlled time delay.

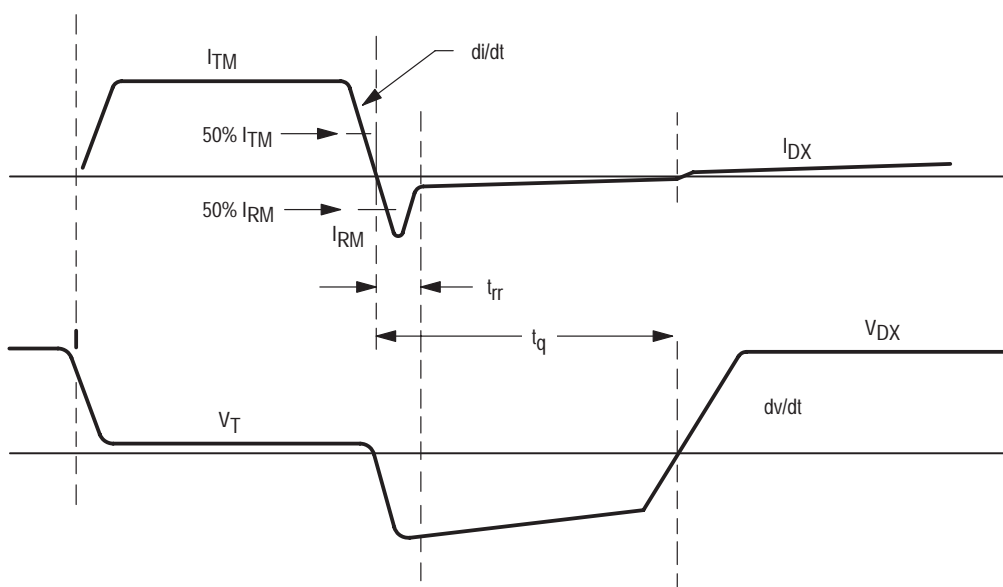


Figure 5.2. SCR Current and Voltage Waveforms During Circuit-Commutated Turn-Off

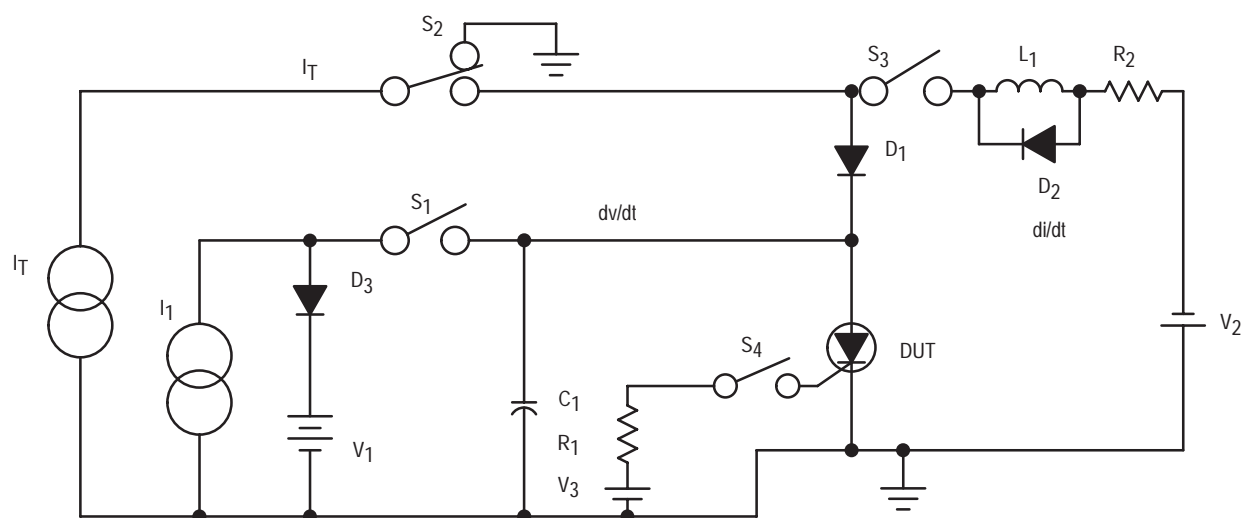


Figure 5.3. Simplified t_q Test Circuit

To generate the appropriate system timing delays, four RC integrating network/comparators are used, consisting of op-amps U2, U5 and U6.

Op-amp U2A, along with transistor Q2, opto-coupler U4 and the following transistors Q6 and Q7, provide the gate drive pulse to the DUT (see waveforms B, C and D of Figure 5.6). The resulting gate current pulse is about 50 μ s wide and can be selected, by means of switch S2, for an I_{GT} of from about 1 mA to 90 mA. Opto-coupler U4, as well as U1 in the Constant Current Circuit, provide electrical isolation between the power circuitry and the low level circuitry.

The Constant Current Circuit consists of an NPN Darlington Q3, connected as a constant current source driving a PNP tri-Darlington (Darlington Q4, Bipolar Q5). By varying the base voltage of Q3 (with Current Control potentiometer R4), the collector current of Q3 and thus the base voltage of Q4 will also vary. The PNP output transistor Q5 (MJ14003) (rated at 70 A), is also configured as a constant current source with four, parallel connected emitter resistors (approximately 0.04 ohms, 200 W), thus providing as much as 60 A test current. Very briefly, the circuit operates as follows: — CMOS Gate IE is clocked high, turning on, in order, a) NPN transistor Q16, b) PNP transistor Q1, c) optocoupler U3, and d) transistors Q3, Q4 and Q5. The board mounted Current Set potentiometer R5, sets the maximum output current and R4, the Current Control, is a front panel, multiturn potentiometer.

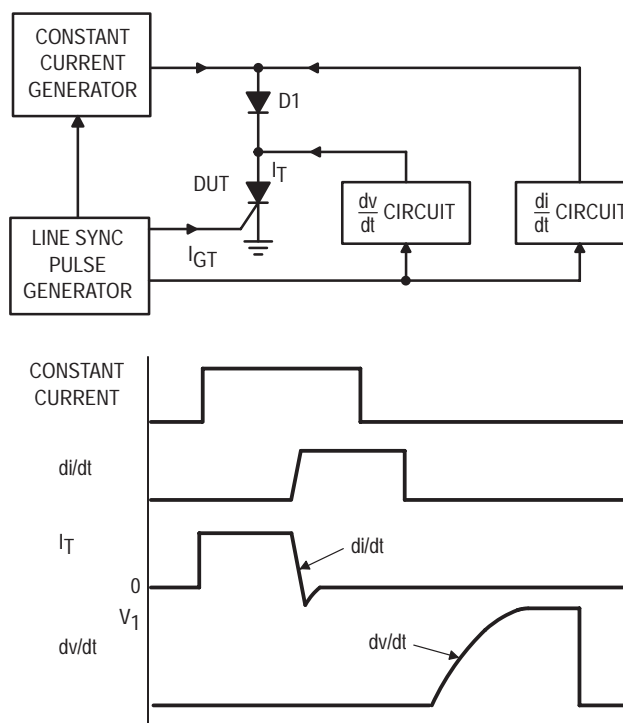


Figure 5.4. Block Diagram of the t_q Test Fixture and Waveforms



Time delay for the di/dt Circuit is derived from cascaded op-amps U2B and U5 (waveforms F and G of Figure 5.6). The output gate, in turn, drives NPN transistor Q8, followed by PNP transistor Q9, whose output provides the gate drive for the three parallel connected N-channel power MOSFET transistors Q10–Q12 (waveforms H of Figure 5.6). These three FETs (MTM15N06), are rated at 15 A continuous drain current and 40 A pulsed current and thus can readily divert the maximum 60 A constant current that the Fixture can generate. The results of this diversion from the DUT is described by waveforms E, H and I of Figure 5.6, with the di/dt of I_{TM} dictated by the series inductance L1. For all subsequent testing, the inductor was a shorting bar, resulting in very little inductance and consequently, the highest di/dt (limited primarily by wiring inductance). When a physical inductor L1 is used, a clamp diode, scaled to the diverted current, should be placed across L1 to limit “inductive kicks.”

dv/dt CIRCUIT

The last major portion of the Fixture, the dv/dt Circuit, is variable time delayed by the multi-turn, front panel t_q Time Control potentiometer R7, operating as part of an integrator on the input of comparator U6. Its output (waveform J of Figure 5.6) is used to turn-off, in order, a) normally on NPN transistor Q13, b) PNP transistor Q14 and c) N-channel power MOSFET Q15 (waveform L of Figure 5.6). This FET is placed across ramp generating capacitor C1, and when unclamped (turned off), the capacitor is allowed to charge through resistor R1 to the supply voltage +V₁. Thus, the voltage appearing on the drain will be an exponentially rising voltage with a dv/dt dictated by R1, C1, whose position in time can be advanced or delayed. This waveform is then applied through a blocking diode to the anode of the DUT for the forward blocking voltage test.

Another blocking diode, D1, also plays an important role in t_q measurements and must be properly selected. Its purpose is to prevent the dv/dt ramp from feeding back into the Current Source and di/dt Circuit and also to momentarily apply a reverse blocking voltage (a function of –V₂ of the di/dt circuit) to the DUT. Consequently, D1 must have a reverse recovery time t_{rr} greater than the DUT, but less than the t_q time. When measuring standard recovery SCRs, its selection — fast recovery rectifiers or standard recovery — is not that critical, however, for fast recovery, low t_q SCRs, the diode must be tailored to the DUT to produce accurate results. Also, the current rating of the diode must be compatible with the DUT test current. These effects are illustrated in the waveforms

shown in Figure 5.7 where both a fast recovery rectifier and standard recovery rectifier were used in measuring t_q of a standard 2N6508 SCR. Although the di/dt's were the same, the reverse recovery current I_{RM} and t_{rr} were greater with the standard recovery rectifier, resulting in a somewhat shorter t_q (59 μ s versus 63 μ s). In fact, t_q is affected by the initial conditions (I_{TM} , di/dt, I_{RM} , dv/dt, etc.) and these conditions should be specified to maintain measurement repeatability. This is later described in the published curves and tables.

Finally, the resistor R1 and the resultant current I_1 in the dv/dt circuit must meet certain criteria: I_1 should be greater than the SCR holding current so that when the DUT does indicate t_q limitation, it latches up, thus suppressing the dv/dt ramp voltage; and, for fast SCRs (low t_q), I_1 should be large enough to ensure measurement repeatability. Typical values of I_1 for standard and fast SCRs may be 50 mA and 500 mA, respectively. Obviously, for high forward blocking voltage + V₁ tests, the power requirements must be met.

EFFECTS OF GATE BIAS ON t_q

Examples of the effects of I_1 on t_q are listed in Table 5.III whereby standard and fast SCRs were tested with about 50 mA and 1 A, respectively. Note that the low t_q SCR's required fast recovery diodes and high I_1 current.

TEST FIXTURE POWER SUPPLIES

Most of the power supplies for the system are self contained, including the +12 V supply for the Constant Current Circuit. This simple, unregulated supply furnishes up to 60 A peak pulsed current, primarily due to the line synchronized operation of the system. Power supplies +V₁ and –V₂, for this exercise, were external supplies, since they are variable, but they can be incorporated in the system. The reverse blocking voltage to the DUT is supplied by –V₂ and is typically set for about –10 V to –20 V, being limited to the breakdown voltage of the diverting power MOSFETS ($V_{DSS} = 60$ V). The +12 V unregulated supply can be as high as +20 V when unloaded; therefore, –V₂ (MAX), in theory, would be –40 V but should be limited to less than –36 V due to the 56 V protective Zener across the drain–source of the FETs. Also, –V₂ must be capable of handling the peak 60 A, diverting current, if so required.

The reapplied forward blocking voltage power supply +V₁, may be as high as the DUT V_{DRM} which conceivably can be 600 V, 1,000 V or greater and, since this supply is on most of the time, must be able to supply the required I_1 . Due to the sometimes high power requirements, +V₁ test conditions may have to be reduced for extremely fast SCRs.

PARAMETERS AFFECTING t_q

To see how the various circuit parameters can affect t_q , one condition at a time is varied while the others are held constant. The parameters to be investigated are a) forward current magnitude (I_{TM}), b) forward current duration, c) rate of change of turn-off current (di/dt), d) reverse-current magnitude (I_{RM}), e) reverse voltage (V_{RM}), f) rate of reapplied forward voltage (dv/dt), g) magnitude limit of reapplied voltage, h) gate-cathode resistance and i) gate drive magnitude (I_{GT}).

Typical data of this kind, taken for a variety of SCRs, including standard SCRs, high speed SCRs, is con-

densed and shown in Table 5.1. The data consists of the different conditions which the particular SCR types were subjected to; ten SCRs of each type were serialized and tested to each condition and the ten t_q 's were averaged to yield a "typical t_q ."

The conditions listed in Column A in Table 5.1, are typical conditions that might be found in circuit operation. Columns B through J in Table 5.1, are in order of increasing t_q ; the conditions listed in these columns are only the conditions that were modified from those in Column A and if a parameter is not listed, it is the same as in Column A.

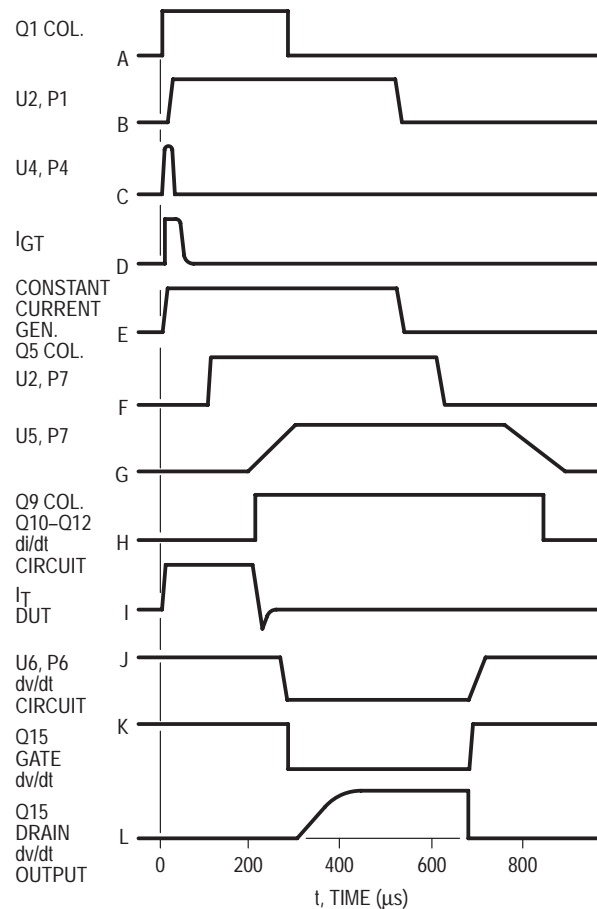
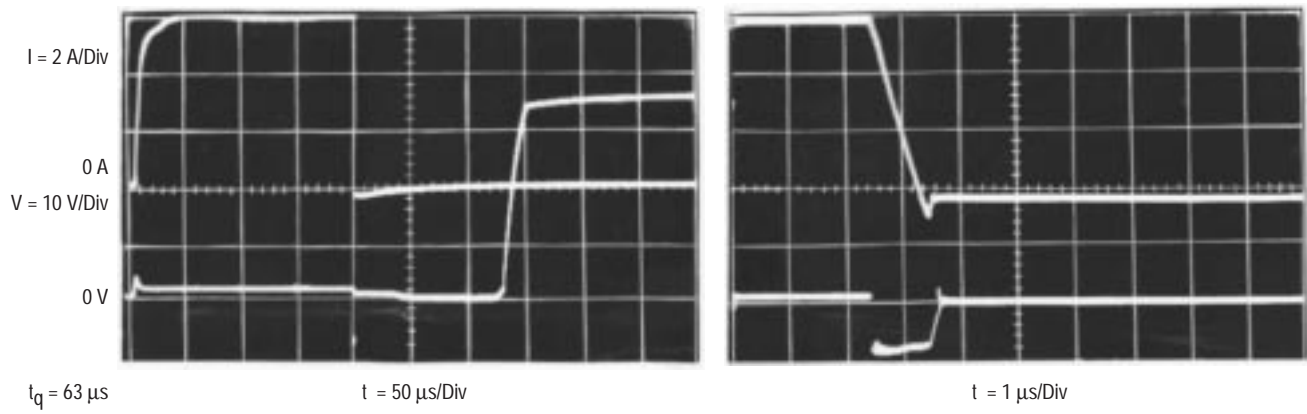
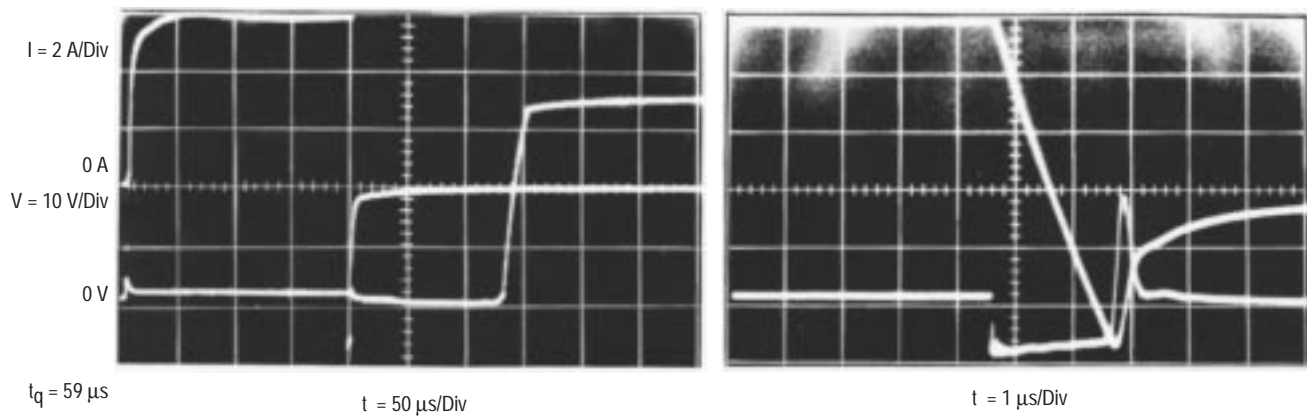


Figure 5.6. t_q Test Fixture System Waveforms



D1 = MR856, FAST RECOVERY RECTIFIER



D1 = 1N5402, STANDARD RECOVERY RECTIFIER

Figure 5.7. The Effects of Blocking Diode D1 on t_q of a 2N6508 SCR

Table 5.1. Parameters Affecting t_q

Device	A	B	C	D	E	F	G	H	I
2N6508 25 A 600 V	$R_{GK} = 1\text{ k}$ $dv/dt = 15\text{ V}/\mu\text{s}$ $I_{TM} = 25\text{ A}$ $I_{RM} = 14\text{ A}$ $di/dt = -100\text{ A}/\mu\text{s}$ $I_{TM}\text{ duration} = 275\text{ }\mu\text{s}$ $I_{GT} = 30\text{ mA}$ $t_{p\text{ }t_q} = 68\text{ }\mu\text{s}$	$R_{GK} = 100$ $dv/dt = 2.4\text{ V}/\mu\text{s}$ $I_{TM} = 1\text{ A}$ $I_{RM} = 1.8\text{ A}$ $di/dt = 32\text{ A}/\mu\text{s}$ $t_{p\text{ }t_q} = 42\text{ }\mu\text{s}$	$R_{GK} = 100$ $dv/dt = 2.4\text{ V}/\mu\text{s}$ $I_{TM} = 2\text{ A}$ $I_{RM} = 50\text{ mA}$ $di/dt = 0.5\text{ }\mu\text{s}$ $t_{p\text{ }t_q} = 45\text{ }\mu\text{s}$	$R_{GK} = 100$ $dv/dt = 2.4\text{ V}/\mu\text{s}$ $I_{RM} = 50\text{ mA}$ $di/dt = 0.45\text{ A}/\mu\text{s}$ $t_{p\text{ }t_q} = 49\text{ }\mu\text{s}$	$R_{GK} = 100$ $dv/dt = 2.4\text{ V}/\mu\text{s}$ $t_{p\text{ }t_q} = 60\text{ }\mu\text{s}$	$R_{GK} = \infty$ $dv/dt = 2.4\text{ V}/\mu\text{s}$ $t_{p\text{ }t_q} = 64\text{ }\mu\text{s}$	$R_{GK} = 100$ $dv/dt = 2.4\text{ V}/\mu\text{s}$ $I_{TM} = 37\text{ A}$ $t_{p\text{ }t_q} = 64\text{ }\mu\text{s}$	$R_{GK} = 100$ $t_{p\text{ }t_q} = 65\text{ }\mu\text{s}$	$I_{GT} = 90\text{ mA}$ $t_{p\text{ }t_q} = 68\text{ }\mu\text{s}$
2N6399 12 A	$R_{GK} = 1\text{ k}$ $dv/dt = 90\text{ V}/\mu\text{s}$ $I_{TM} = 12\text{ A}$ $I_{RM} = 11\text{ A}$ $di/dt = -100\text{ A}/\mu\text{s}$ $I_{TM}\text{ duration} = 275\text{ }\mu\text{s}$ $I_{GT} = 30\text{ mA}$ $t_{p\text{ }t_q} = 48\text{ }\mu\text{s}$	$R_{GK} = 100$ $dv/dt = 2.5\text{ V}/\mu\text{s}$ $I_{TM} = 1\text{ A}$ $I_{RM} = 50\text{ mA}$ $di/dt = -0.5\text{ A}/\mu\text{s}$ $t_{p\text{ }t_q} = 30\text{ }\mu\text{s}$	$R_{GK} = 100$ $dv/dt = 2.5\text{ V}/\mu\text{s}$ $I_{TM} = 1\text{ A}$ $I_{RM} = 2.7\text{ A}$ $di/dt = 56\text{ A}/\mu\text{s}$ $t_{p\text{ }t_q} = 31\text{ }\mu\text{s}$	$R_{GK} = 100$ $dv/dt = 2.5\text{ V}/\mu\text{s}$ $I_{RM} = 50\text{ mA}$ $di/dt = 32\text{ A}/\mu\text{s}$ $t_{p\text{ }t_q} = 32\text{ }\mu\text{s}$	$R_{GK} = 100$ $dv/dt = 2.5\text{ V}/\mu\text{s}$ $I_{TM} = 18\text{ A}$ $I_{RM} = 50\text{ mA}$ $di/dt = 0.3\text{ A}/\mu\text{s}$ $t_{p\text{ }t_q} = 33\text{ }\mu\text{s}$	$R_{GK} = \infty$ $dv/dt = 2.5\text{ V}/\mu\text{s}$ $I_{RM} = 50\text{ mA}$ $di/dt = 0.35\text{ A}/\mu\text{s}$ $t_{p\text{ }t_q} = 35.5\text{ }\mu\text{s}$	$R_{GK} = 100$ $t_{p\text{ }t_q} = 45\text{ }\mu\text{s}$	$I_{GT} = 90\text{ mA}$ $t_{p\text{ }t_q} = 48\text{ }\mu\text{s}$	

Table 5.1. Continued

Device	A	B	C	D	E	F	G	H	I
C106B 4 A	$I_{GT} = 1 \text{ mA}$ $R_{GK} = 1 \text{ k}$ $dv/dt = 5 \text{ V}/\mu\text{s}$ $I_{TM} = 4 \text{ A}$ $I_{RM} = 4 \text{ A}$ $di/dt = 50 \text{ A}/\mu\text{s}$ $I_{TM} \text{ duration} = 275 \mu\text{s}$ $V_{DX} = 50 \text{ V}$	$I_{TM} = 2 \text{ A}$ $I_{RM} = 2.5 \text{ A}$ $di/dt = -30 \text{ A}/\mu\text{s}$ $V_{DX} = 50 \text{ V}$	$I_{TM} = 6 \text{ A}$ $I_{RM} = -1 \text{ A}/\mu\text{s}$ $di/dt = -1 \text{ A}/\mu\text{s}$ $V_{DX} = 150 \text{ V}$	$I_{TM} = 6 \text{ A}$ $I_{RM} = 0.1 \text{ A}$ $di/dt = -1 \text{ A}/\mu\text{s}$ $V_{DX} = 50 \text{ V}$	$dv/dt = 1.4 \text{ V}/\mu\text{s}$ $I_{TM} = 2 \text{ A}$ $I_{RM} = 0.2 \text{ A}$ $di/dt = -1.4 \text{ A}/\mu\text{s}$	$-V_2 = 35 \text{ V}$ $I_{RM} = 0.2 \text{ A}$ $di/dt = -1.4 \text{ A}/\mu\text{s}$	$I_{RM} = 0.15 \text{ A}$ $-V_2 = 4 \text{ V}$ $di/dt = -1.4 \text{ A}/\mu\text{s}$	$dv/dt = 1.4 \text{ V}/\mu\text{s}$ $I_{RM} = 0.15 \text{ A}$ $di/dt = 1.4 \text{ A}/\mu\text{s}$	$I_{GT} = 90 \text{ mA}$ $dv/dt = 1.4 \text{ V}/\mu\text{s}$ $I_{RM} = 2 \text{ A}$ $di/dt = -1.4 \text{ A}/\mu\text{s}$
	$typ t_q = 28 \mu\text{s}$	$typ t_q = 25 \mu\text{s}$	$typ t_q = 26 \mu\text{s}$	$typ t_q = 26 \mu\text{s}$	$typ t_q = 26 \mu\text{s}$	$typ t_q = 27 \mu\text{s}$	$typ t_q = 27 \mu\text{s}$	$typ t_q = 27 \mu\text{s}$	$typ t_q = 27 \mu\text{s}$
2N6240 4 A	$R_{GK} = 1 \text{ k}$ $dv/dt = 40 \text{ V}/\mu\text{s}$ $I_{TM} = 4 \text{ A}$ $I_{RM} = 4 \text{ A}$ $di/dt = 50 \text{ A}/\mu\text{s}$ $I_{TM} \text{ duration} = 275 \mu\text{s}$ $I_{GT} = 1 \text{ mA}$ $V_{DX} = 50 \text{ V}$	$R_{GK} = 100$ $dv/dt = 1.3 \text{ V}/\mu\text{s}$ $I_{TM} = 1 \text{ A}$ $I_{RM} = 50 \text{ mA}$ $di/dt = -0.5 \text{ A}/\mu\text{s}$ $I_{GT} = 90 \text{ mA}$ $V_{DX} = 150 \text{ V}$	$R_{GK} = 100$ $dv/dt = 1.75 \text{ V}/\mu\text{s}$ $I_{TM} = 1 \text{ A}$ $I_{RM} = 50 \text{ mA}$ $di/dt = -0.5 \text{ A}/\mu\text{s}$ $I_{GT} = 90 \text{ mA}$	$R_{GK} = 100$ $dv/dt = 1.75 \text{ V}/\mu\text{s}$ $I_{RM} = 50 \text{ mA}$ $di/dt = -0.5 \text{ A}/\mu\text{s}$ $I_{GT} = 90 \text{ mA}$	$dv/dt = 1.75 \text{ V}/\mu\text{s}$ $R_{GK} = 100$ $I_{TM} = 6 \text{ A}$ $I_{RM} = 50 \text{ mA}$ $di/dt = -0.5 \text{ A}/\mu\text{s}$ $I_{GT} = 90 \text{ mA}$	$R_{GK} = 100$ $I_{RM} = 50 \text{ mA}$ $di/dt = -0.5 \text{ A}/\mu\text{s}$ $I_{GT} = 90 \text{ mA}$	$R_{GK} = 100$ $I_{GT} = 90 \text{ mA}$	$R_{GK} = \infty$ $dv/dt = 1.75 \text{ V}/\mu\text{s}$ $I_{TM} = 1 \text{ A}$ $I_{RM} = 50 \text{ mA}$ $di/dt = -0.5 \text{ A}/\mu\text{s}$ $I_{GT} = 90 \text{ mA}$	$I_{GT} = 90 \text{ mA}$
	$typ t_q = 44.8 \mu\text{s}$	$typ t_q = 26 \mu\text{s}$	$typ t_q = 26.2 \mu\text{s}$	$typ t_q = 27.7 \mu\text{s}$	$typ t_q = 28.6 \mu\text{s}$	$typ t_q = 30 \mu\text{s}$	$typ t_q = 32.7 \mu\text{s}$	$typ t_q = 37.2 \mu\text{s}$	$typ t_q = 41.4 \mu\text{s}$
MCR100-6 0.8 A	$R_{GK} = 1 \text{ k}$ $dv/dt = 160 \text{ V}/\mu\text{s}$ $I_{TM} = 0.8 \text{ A}$ $I_{RM} = 0.8 \text{ A}$ $di/dt = 12 \text{ A}/\mu\text{s}$ $V_{DX} = 50 \text{ V}$ $I_{TM} \text{ duration} = 275 \mu\text{s}$	$dv/dt = 30 \text{ V}/\mu\text{s}$ $I_{TM} = 0.25 \text{ A}$ $I_{RM} = 40 \text{ mA}$ $di/dt = -0.6 \text{ A}/\mu\text{s}$	$dv/dt = 30 \text{ V}/\mu\text{s}$ $I_r = 40 \text{ mA}$ $di/dt = -0.8 \text{ A}/\mu\text{s}$	$-V_2 = 9 \text{ V}$ $I_{RM} = 20 \text{ mA}$ $di/dt = -0.4 \text{ A}/\mu\text{s}$	$-V_2 = 1 \text{ V}$ $I_r = 40 \text{ mA}$ $di/dt = -0.8 \text{ A}/\mu\text{s}$	$dv/dt = 30 \text{ V}/\mu\text{s}$ $I_{TM} = 1.12 \text{ A}$ $I_{RM} = 40 \text{ mA}$ $di/dt = -0.8 \text{ A}/\mu\text{s}$	$dv/dt = 30 \text{ V}/\mu\text{s}$ $I_{RM} = 1.12 \text{ A}$ $I_{RM} = 40 \text{ mA}$ $di/dt = -0.8 \text{ A}/\mu\text{s}$ $V_{DX} = 100 \text{ V}$		
	$typ t_q = 14.4 \mu\text{s}$	$typ t_q = 12.7 \mu\text{s}$	$typ t_q = 13.5 \mu\text{s}$	$typ t_q = 13.7 \mu\text{s}$	$typ t_q = 13.9 \mu\text{s}$	$typ t_q = 14.4 \mu\text{s}$	$typ t_q = 14.4 \mu\text{s}$		
2N5064 0.8 A	$R_{GK} = 1 \text{ k}$ $dv/dt = 30 \text{ V}/\mu\text{s}$ $I_{TM} = 0.8 \text{ A}$ $I_{RM} = 0.8 \text{ A}$ $di/dt = 12 \text{ A}/\mu\text{s}$ $I_{TM} \text{ duration} = 275 \mu\text{s}$ $V_{DX} = 50 \text{ V}$	$dv/dt = 5 \text{ V}/\mu\text{s}$ $I_{TM} = 0.2 \text{ A}$ $I_{RM} = 50 \text{ mA}$ $di/dt = -0.6 \text{ A}/\mu\text{s}$	$dv/dt = 5 \text{ V}/\mu\text{s}$ $I_{RM} = 50 \text{ mA}$ $di/dt = -0.8 \text{ A}/\mu\text{s}$	$dv/dt = 5 \text{ V}/\mu\text{s}$ $I_{TM} = 1.12 \text{ A}$ $I_{RM} = 50 \text{ mA}$ $di/dt = -0.8 \text{ A}/\mu\text{s}$	$I_{RM} = 40 \text{ mA}$ $-V_2 = 9 \text{ V}$ $di/dt = -0.45 \text{ A}/\mu\text{s}$	$I_{RM} = 40 \text{ mA}$ $-V_2 = 1 \text{ V}$ $di/dt = -0.8 \text{ A}/\mu\text{s}$	$V_{DX} = 100 \text{ V}$ $dv/dt = 5 \text{ V}/\mu\text{s}$ $I_{TM} = 1.12 \text{ A}$ $I_{RM} = 50 \text{ mA}$ $di/dt = -0.8 \text{ A}$		
	$typ t_q = 28.9 \mu\text{s}$	$typ t_q = 27 \mu\text{s}$	$typ t_q = 30 \mu\text{s}$	$typ t_q = 31 \mu\text{s}$	$typ t_q = 31.2 \mu\text{s}$	$typ t_q = 31.4 \mu\text{s}$	$typ t_q = 31.7 \mu\text{s}$		
2N5061 0.8 A	$dv/dt = 10 \text{ V}/\mu\text{s}$ $I_{TM} = 0.8 \text{ A}$ $I_{RM} = 0.8 \text{ A}$ $di/dt = 18 \text{ A}/\mu\text{s}$ $I_{TM} \text{ duration} = 275 \mu\text{s}$ $R_{GK} = 1 \text{ k}$ $V_{DX} = 30 \text{ V}$	$dv/dt = 3.5 \text{ V}/\mu\text{s}$ $I_{TM} = 0.25 \text{ A}$ $I_{RM} = 40 \text{ mA}$ $di/dt = -0.7 \text{ A}/\mu\text{s}$	$dv/dt = -3.5 \text{ V}/\mu\text{s}$ $I_{RM} = 40 \text{ mA}$ $di/dt = -0.8 \text{ A}/\mu\text{s}$	$dv/dt = 3.5 \text{ V}/\mu\text{s}$ $I_{TM} = 1.12 \text{ A}$ $I_{RM} = 40 \text{ mA}$ $di/dt = -0.8 \text{ A}/\mu\text{s}$ $V_{DX} = 60 \text{ V}$	$dv/dt = 3.58 \mu\text{s}$ $I_{TM} = 1.12 \text{ A}$ $I_{RM} = 40 \text{ mA}$ $di/dt = -0.7 \text{ A}/\mu\text{s}$	$-V_2 = 4 \text{ V}$ $I_{RM} = 20 \text{ mA}$ $di/dt = -0.2 \text{ A}/\mu\text{s}$	$-V_2 = 1 \text{ V}$ $I_{RM} = 40 \text{ mA}$ $di/dt = -0.8 \text{ A}/\mu\text{s}$		
	$typ t_q = 31.7 \mu\text{s}$	$typ t_q = 19.1 \mu\text{s}$	$typ t_q = 19 \mu\text{s}$	$typ t_q = 19.8 \mu\text{s}$	$typ t_q = 20.2 \mu\text{s}$	$typ t_q = 30 \mu\text{s}$	$typ t_q = 30.2 \mu\text{s}$		

Table 5.2 is a condensed summary of Table 5.1 and shows what happens to the t_q of the different devices when a parameter is varied in one direction or the other.

THE EFFECT OF CHANGING PARAMETERS ON t_q

From Tables 5.1 and 5.2, it is clear that some parameters affect t_q more than others. The following discussion describes the effect on t_q of the various parameters.

FORWARD CURRENT MAGNITUDE (I_{TM})

Of the parameters that were investigated, forward-current magnitude and the di/dt rate have the strongest effect on t_q . Varying the I_{TM} magnitude over a realistic range of I_{TM} conditions can change the measured t_q by about 30%. The change in t_q is attributed to varying current densities (stored charge) present in the SCR's junctions as the I_{TM} magnitude is changed. Thus, if a large SCR must have a short t_q when a low I_{TM} is present, a large gate trigger pulse (I_{GT} magnitude) would be advantageous. This turns on a large portion of the SCR to minimize the high current densities that exists if only a small portion of the SCR were turned on (by a weak gate pulse) and the low I_{TM} did not fully extend the turned on region.

In general, the SCR will exhibit longer t_q times with increasing I_{TM} . Increasing temperature also increases the t_q time.

di/dt RATE

Varying the turn-off rate of change of anode current di/dt does have some effect on the t_q of SCRs. Although the increase in t_q versus increasing di/dt was nominal for the SCRs illustrated, the percentage change for the fast SCRs was fairly high (about 30–40%).

REVERSE CURRENT MAGNITUDE (I_{RM})

The reverse current is actually due to the stored charge clearing out of the SCR's junctions when a negative voltage is applied to the SCR anode. I_{RM} is very closely related to the di/dt rate; an increasing di/dt rate causing an increase of I_{RM} and a decreasing di/dt rate causing a lower I_{RM} .

Parameter Changed	Device	Columns	1st (μs)	2nd (μs)
I_{GT} Increase	2N6508	AI	68	68
	2N6399	AG	48	48
	2N6240	AI	44.8	41.4
	C106F	HI	27	27
Decrease R_{GK} 1 k to 100 ohms	2N6508	AH	68	65
	2N6399	AG	48	45
	2N6240	GI	41.4	32.7
Increase R_{GK} 1 k to ∞	2N6508	EF	60	64
	2N6399	DF	32	35.5
	2N6240	CH	26.2	37.2
V_{DX}	C106F	DC	26	26
	2N6240	BC	26.2	26
	MCR100-6	FG	14.4	14.4
	2N5064	DG	31	31.7
	2N5061	DE	20.2	19.8
Decrease dv/dt Rate	2N6508	EH	65	60
	C106F	HJ	29	27
	2N6240	DF	30	27.7
Increase I_{TM}	2N6508	EG	60	64
	2N6399	DE	32	33
	C106F	EH	26	27
	2N6240	DC	26.2	27.7
		DE	27.7	28.6
		CE	26.2	28.6
	MCR100-6	CF	13.5	14.4
	2N5064	CD	30.7	31
	2N5061	BE	19.1	20.7

Table 5.2. The Effects of Changing Parameters on t_q

By using different series inductors and changing the negative anode turn-off voltage, it is possible to keep the di/dt rate constant while changing I_{RM} . It was found that I_{RM} has little or no effect on t_q when it is the only variable changed (see Table 5.1 C106F, Columns F and G, for example).

REVERSE ANODE VOLTAGE (V_{RM})

Reverse anode voltage has a strong effect on the I_{RM} magnitude and the di/dt rate, but when V_{RM} alone is varied, with I_{RM} and di/dt held constant, little or no change in t_q time was noticed. V_{RM} must always be within the reverse voltage of the device.

Device	Gate Bias		Conditions		+ V ₁	RI	dv/dt (V/ μ s)
	0V	- 5 V	- V ₂ = -10 V, I _F = 3 A		50 V	1 k/50	2.5/50
	t _q ¹	t _q ²	Diode DI	dv/dt (V/ μ s)	Remarks		
2N6508	40 μ s	30 μ s	Slow MR502	2.5	Slow diode faster than fast diode, (lower t _q)		
2N6240	16 μ s	9 μ s	Slow	2.5	Slow diode faster. 2.5 V/ μ s faster than 50 V/ μ s		
2N6399	30 μ s	25 μ s	Slow	2.5	Tested slow diode only		
C106F	13 μ s	8 μ s	Slow	2.5	Tested slow diode only		

Table 5.3 The Effects of Gate Bias on t_q

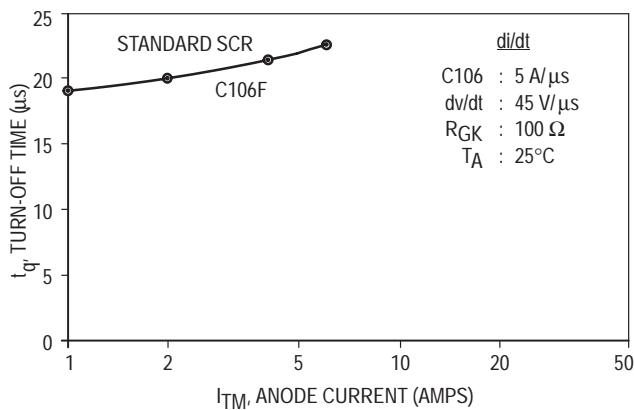


Figure 5.8. Standard SCR Turn-Off Time t_q as a Function of Anode Current I_{TM}

REAPPLIED dv/dt RATE

Varying the reappplied dv/dt rate across the range of dv/dt's commonly encountered can vary the t_q of a given SCR by more than 10%. The effect of the dv/dt rate on t_q is due to the Anode-Gate capacitance. The dv/dt applied at the SCR anode injects current into the gate through this capacitance ($i_{GT} = C \, dv/dt$). As the dv/dt rate increased, the gate current also increases and can trigger the SCR on. To complicate matters, this injected current also adds to the current due to leakage or stored charge left in the junctions just after turn-off.

The stored charge remaining in the center junction is the main reason for long t_q times and, for the most part, the charge is removed by the recombination process. If the reappplied dv/dt rate is high, more charge is injected into this junction and prevents it from returning to the blocking state, as soon as if it were a slow dv/dt rate. The higher the dv/dt rate, the longer the t_q times will be.

MAGNITUDE LIMIT OF REAPPLIED dv/dt (V_{DX})

Changing the magnitude limit of the reappplied dv/dt voltage has little or no effect on a given SCR's t_q time when the maximum applied voltage is well below the voltage breakdown of the SCR. The t_q times will lengthen if the SCR is being used near its voltage breakdown, since the leakage present near breakdown is higher than at lower voltage levels. The leakage will lengthen the time it takes for the charge to be swept out of the SCR's center junction, thus lengthening the time it takes for this junction to return to the blocking state.

GATE CATHODE RESISTANCE (R_{GK})

In general, the lower the R_{GK} is, the shorter the t_q time will be for a given SCR. This is because low R_{GK} aids in the removal of stored charge in the SCR's junctions. An approximate 15% change in the t_q time is seen by changing R_{GK} from 100 ohms to 1000 ohms for the DUTs.

GATE DRIVE MAGNITUDE (I_{GT})

Changing the gate drive magnitude has little effect on a SCR's t_q time unless it is grossly overdriven or underdriven. When it is overdriven, there is an unnecessary large amount of charge in SCR's junction. When underdriven, it is possible that only a small portion of the chip at the gate region turns on. If the anode current is not large enough to spread the small turned on region, there is a high current and charge density in this region that consequently lengthens the t_q time.

FORWARD CURRENT DURATION

Forward current duration had no measurable effect on t_q time when varied from 100 μ s to 300 μ s, which were the limits of the ON Semiconductor t_q Tester. Longer I_{TM} durations heat up the SCR which causes temperature effects; very short I_{TM} durations affect the t_q time due to the lack of time for the charges in the SCR's junctions to reach equilibrium, but these effects were not seen in the range tested.

REVERSE GATE BIAS VOLTAGE

As in transistor operation, reverse biasing the gate of the SCR decreases the turn-off time, due to the rapid “sweeping out” of the stored charge. The reduction in t_q for standard SCRs is quite pronounced, approaching perhaps 50% in some cases; for fast SCRs, only nominal improvement might result. Table 5.3 shows this effect on six SCRs where the gate bias was set for 0 V and -5 V, respectively (the 1 k gate resistor of the DUT was either grounded or returned to -5 V). Due to the internal, monolithic resistor of most SCRs, the actual reverse bias voltage between the gate–cathode is less than the reverse bias supply.

CHARACTERIZING SCRs FOR CROWBAR APPLICATIONS

The use of a crowbar to protect sensitive loads from power supply overvoltage is quite common and, at the first glance, the design of these crowbars seems like a straightforward, relatively simple task. The crowbar SCR is selected so as to handle the overvoltage condition and a fuse is chosen at 125 to 250% of the supply's rated full-load line current. However, upon further investigation, other questions and problems are encountered.

How much overvoltage and for how long (energy) can the load take this overvoltage? Will the crowbar respond too slowly and thus not protect the load or too fast resulting in false, nuisance triggering? How much energy can the crowbar thyristor (SCR) take and will it survive until the fuse opens or the circuit breaker opens? How fast will the fuse open, and at what energy level? Can the fuse adequately differentiate between normal current levels — including surge currents — and crowbar short circuit conditions?

It is the attempt of this section to answer these questions — to characterize the load, crowbar, and fuse and thus to match their characteristics to each other.

The type of regulator of most concern is the low voltage, series pass regulator where the filter capacitors to be crowbarred, due to 60 Hz operation, are relatively large and the charge and energy stored correspondingly large. On the other hand, switching regulators operating at about 20 kHz require smaller capacitors and thus have lower crowbar constraints.

These regulators are quite often line-operated using a high voltage, two-transistor inverter, half bridge or full bridge, driving an output step-down transformer. If a transistor were to fail, the regulator-transformed power would be less and the output voltage would drop, not rise, as is the case for the linear series regulator with a shorted pass transistor. Thus, the need for overvoltage protection of these types of switching regulators is minimized.

This premise, however, does not consider the case of the lower power series switching regulator where a

shorted transistor would cause the output voltage to rise. Nor does it take into account overvoltage due to transients on the output bus or accidental power supply hookup. For these types of operations, the crowbar SCR should be considered.

HOW MUCH OVERVOLTAGE CAN THE LOAD TAKE?

Crowbar protection is most often needed when ICs are used, particularly those requiring a critical supply voltage such as TTL or expensive LSI memories and MPUs.

If the load is 5 V TTL, the maximum specified continuous voltage is 7 V. (CMOS, with its wide power supply range of 3 to 18 V, is quite immune to most overvoltage conditions.) But, can the TTL sustain 8 V or 10 V or 15 V and, if so, for how long and for how many power cycles? Safe Operating Area (SOA) of the TTL must be known. Unfortunately, this information is not readily available and has to be generated.

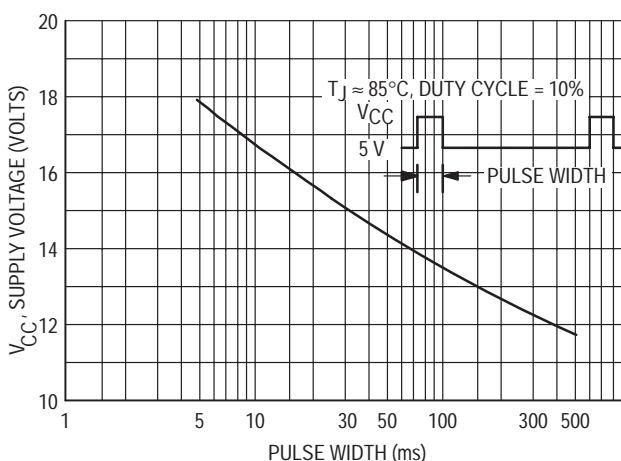
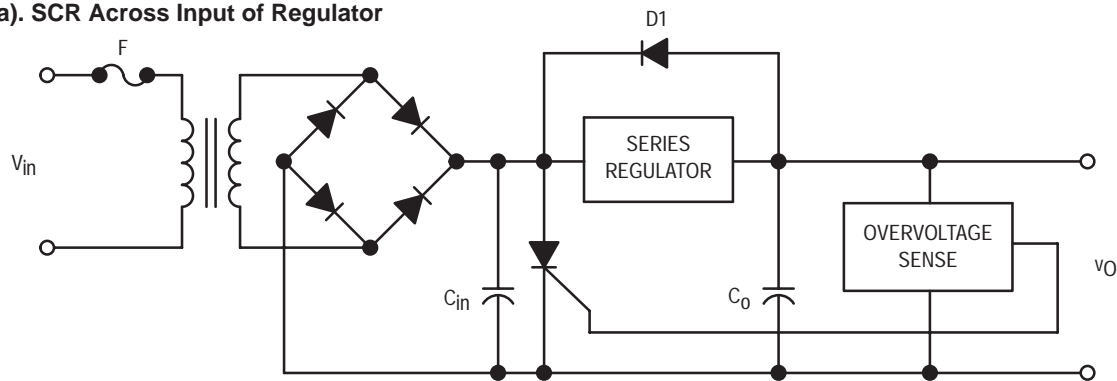


Figure 5.9. Pulsed Supply Voltage versus Pulse Width

Using the test circuit illustrated in Appendix III, a quasi-SOA curve for a typical TTL gate was generated (Figure 5.9). Knowing the overvoltage–time limit, the crowbar and fuse energy ratings can be determined.

The two possible configurations are illustrated in Figure 5.10, the first case shows the crowbar SCR across the input of the regulator and the second, across the output. For both configurations, the overvoltage comparator senses the load voltage at the remote load terminals, particularly when the I_R drop of the supply leads can be appreciable. As long as the output voltage is less than that of the comparator reference, the crowbar SCR will be in an off state and draw no supply current. When an over-voltage condition occurs, the comparator will produce a gate trigger to the SCR, firing it, and thus clamping the regulator input, as in the first case — to the SCRs on-state drop of about 1 to 1.5 V, thereby protecting the load.

(a). SCR Across Input of Regulator



(b). SCR Across Output of Regulator

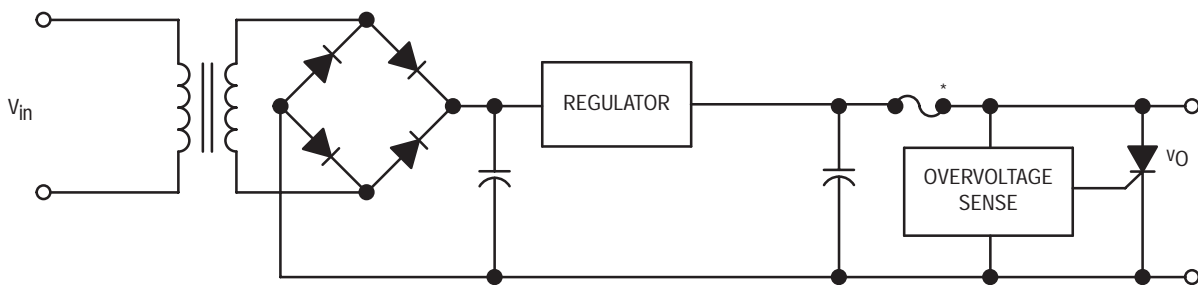


Figure 5.10. Typical Crowbar Configurations

Placing the crowbar across the input filter capacitors, although effectively clamping the output, has several disadvantages.

1. There is a stress placed on the input rectifiers during the crowbarring short circuit time before the line fuse opens, particularly under repeated operation.
2. Under low line conditions, the minimum short circuit current can be of the same magnitude as the maximum primary line current at high line, high load, making the proper fuse selection a difficult choice.
3. The capacitive energy to be crowbarred (input and output capacitor through rectifier D1) can be high.

When the SCR crowbar and the fuse are placed in the dc load circuit, the above problems are minimized. If crowbarring occurs due to an external transient on the line and the regulator's current limiting is working properly, the SCR only has to crowbar the generally smaller output filter capacitor and sustain the limited regulator current.

If the series pass devices were to fail (short), even with current limiting or foldback disabled, the crowbarred energy would generally be less than of the previous case. This is due to the higher impedance of the shorted regulator (due to emitter sharing and current sensing resistors) relative to that of rectifier D1.

Fuse selection is much easier as a fault will now give a greater percentage increase in dc load current than when measuring transformer primary or secondary rms current. The disadvantage, however, of placing the fuse in the dc load is that there is no protection for the input rectifier, capacitor, and transformer, if one of these components were to fail (short). Secondly, the one fuse must protect not only the load and regulator, but also have adequate clearing time to protect the SCR, a situation which is not always readily accomplished. The input circuitry can be protected with the addition of a primary fuse or a circuit breaker.

HOW MUCH ENERGY HAS TO BE CROWBARRED?

This is dictated by the power supply filter capacitors, which are a function of output current. A survey of several linear power supply manufacturers showed the output filter capacitor size to be from about 100 to 400 microfarads per ampere with about 200 $\mu\text{F}/\text{A}$ being typical. A 30 A regulator might therefore have a 6000 μF output filter capacitor.

Additionally, the usually much larger input filter capacitor will have to be dumped if the regulator were to short, although that energy to be dissipated will be dependent on the total resistance in the circuit between that capacitor and the SCR crowbar.

The charge to be crowbarred would be

$$Q = CV = I_T,$$

the energy,

$$E = 1/2 CV^2$$

and the peak surge current

$$i_{pk} = \frac{V_C}{R_T}$$

When the SCR crowbars the capacitor, the current waveform will be similar to that of Figure 5.11, with the peak surge current, i_{pk} , being a function of the total impedance in the circuit (Figure 5.12) and will thus be limited by the Equivalent Series Resistance (ESR) and inductance (ESL) of the capacitor plus the dynamic impedance of the SCR, any external current limiting resistance, (and inductance) of the interconnecting wires and circuit board conductors.

The ESR of computer grade capacitors, depending on the capacitor size and working voltage, might vary from 10 to 1000 milliohms ($m\Omega$). Those used in this study were in the 25 to 50 $m\Omega$ range.

The dynamic impedance of the SCR (the slope of the on-state voltage, on-state current curve), at high currents, might be in the 10 to 20 $m\Omega$ range. As an example, from the on-state characteristics of the MCR70, 35 A rms SCR, the dynamic impedance is

$$r_d = \frac{\Delta V_F}{\Delta I_F} = \frac{(4.5 - 3.4)V}{(300 - 200)A} = \frac{1.1 V}{100 A} \cong 11 m\Omega.$$

The interconnecting wire might offer an additional 5 $m\Omega$ (#20 solid copper wire $\cong 20 m\Omega/ft$) so that the total circuit resistance, without additional current limiting, might be in the 40 to 70 $m\Omega$ range. The circuit inductance was considered low enough to ignore so far as i_{pk} is concerned for this exercise, being in hundreds of nano-henry range (ESL $\cong 3 nH$, L wire $\cong 500 nH/ft$). However, di/dt will be affected by the inductance.

HOW MUCH ENERGY CAN THE CROWBAR SCR SUSTAIN?

There are several factors which contribute to possible SCR failures or degradation — the peak surge current, di/dt , and a measure of the device's energy capability, I^2t .

If the peak current and/or duration of the surge is large, destruction of the device due to excessive dissipation can occur. Obviously, the i_{pk} can be reduced by inserting additional impedance in the crowbar path, at an increase in dump time. However, this time, which is a measure of how long the overvoltage is present, should be within the SOA of the load.

The energy stored in the capacitor being a constant for a particular voltage would suggest that the I^2t integral for any limiting resistance is also a constant. In reality, this is not the case as the thermal response of the device must be taken into consideration. It has been shown that the dissipation capability of a device varies as to the \sqrt{t} for the first tens of milliseconds of the thermal response and, in effect, the measure of a device's energy capability would be closer to $i^2\sqrt{t}$. This effect is subsequently illustrated in the empirically derived i_{pk} versus time derating curves being a non-linear function. However, for comparison with fuses, which are rated in I^2t , the linear time base, "t," will be used.

The di/dt of the current surge pulse is also a critical parameter and should not exceed the device's ratings (typically about 200 A/ μs for 50 A or less SCRs). The magnitude of di/dt that the SCR can sustain is controlled by the device construction and, to some extent, the gate drive conditions. When the SCR gate region is driven on, conduction across the junction starts in a small region and progressively propagates across the total junction. Anode current will initially be concentrated in this small conducting area, causing high current densities which can degrade and ultimately destroy the device. To minimize this di/dt effect, the gate should be turned on hard and fast such that the area turned on is initially maximized. This can be accomplished with a gate current pulse approaching five times the maximum specified continuous gate current, I_{gt} , and with a fast rise time ($< 1 \mu s$). The gate current pulse width should be greater than the propagation time; a figure of 10 μs minimum should satisfy most SCRs with average current ratings under 50 A or so.

The wiring inductance alone is generally large enough to limit the di/dt . Since most SCRs are good for over 100 A/ μs , this effect is not too large a problem. However, if the di/dt is found excessive, it can be reduced by placing an inductance in the loop; but, again, this increases the circuit's response time to an overvoltage and the trade-off should be considered.

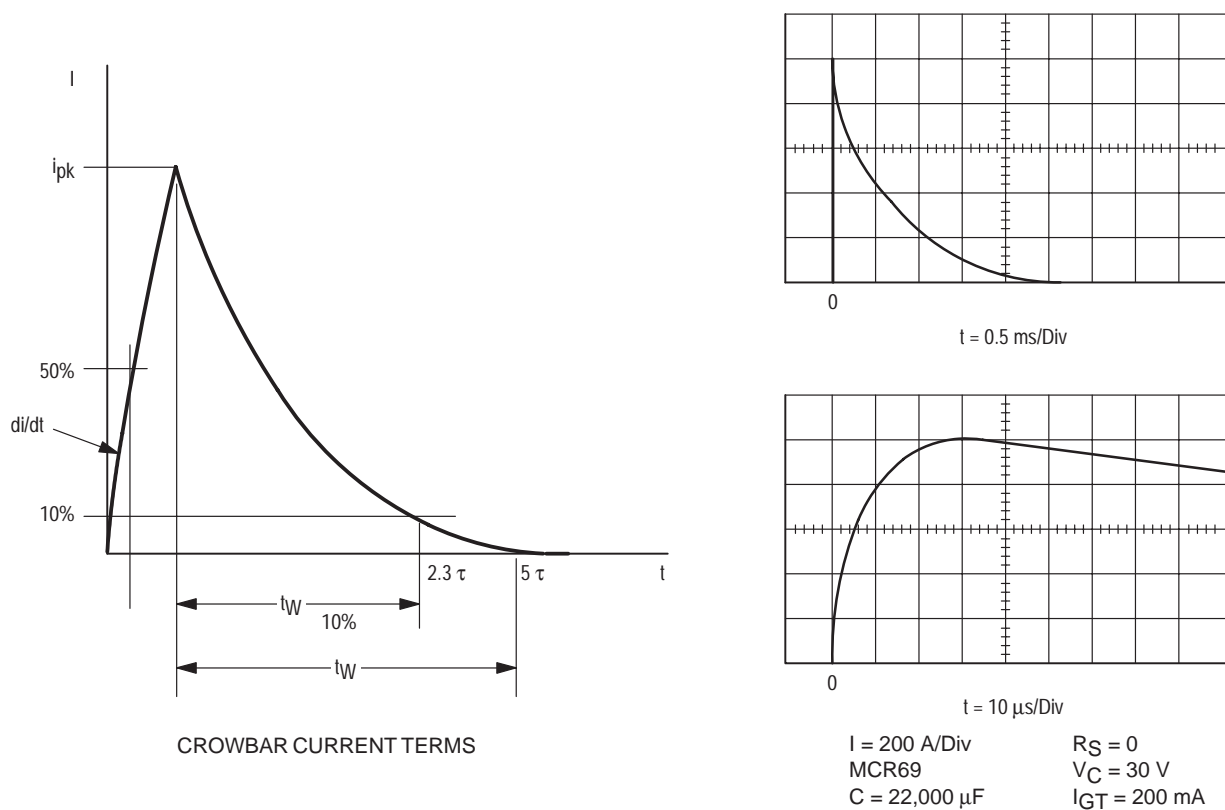


Figure 5.11. Typical SCR Crowbar Waveform

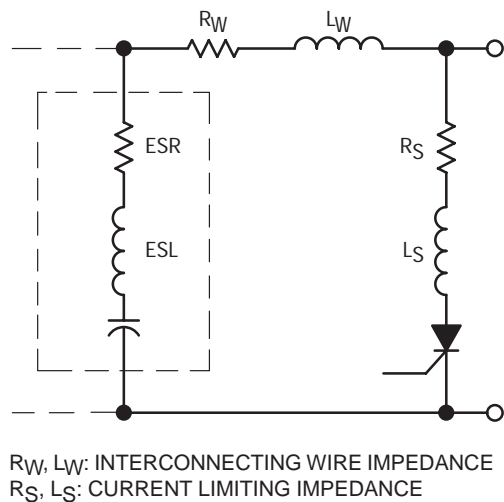


Figure 5.12. Circuit Elements Affecting SCR Surge Current

Since many SCR applications are for 60 Hz line operation, the specified peak non-repetitive surge current I_{TSM} and circuit fusing I^2t are based on 1/2 cycle (8.3 ms) conditions. For some SCRs, a derating curve based on up to 60 or 100 cycles of operation is also published. This rating, however, does not relate to crowbar applications. To fully evaluate a crowbar system, the SCR must be characterized with the capacitor dump exponential surge current pulse.

A simple test circuit for deriving this pulse is shown in Figure 5.13, whereby a capacitor is charged through a limiting resistor to the supply voltage, V , and then the charge is dumped by the SCR device under test (DUT). The SCR gate pulse can be varied in magnitude, pulse width, and rise time to produce the various I_{GT} conditions. An estimate of the crowbar energy capability of the DUT is determined by first dumping the capacitor charged to low voltage and then progressively increasing the voltage until the DUT fails. This is repeated for several devices to establish an average and minimum value of the failure points cluster.

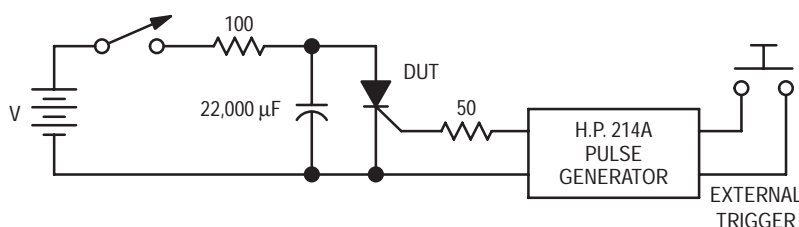


Figure 5.13

This procedure was used to test several different SCRs of which the following Table 5.4 describes several of the pertinent energy specifications and also the measured crowbar surge current at the point of device failure.

This one-shot destruct test was run with a gate current of five $I_{GT}(\text{MAX})$ and a 22,000 μF capacitor whose ESR produced the exponentially decaying current pulse about 1.5 ms wide at its 10% point. Based on an appropriate derating, ten devices of each line were then successfully tested under the following conditions.

Device	V_C	i_{pk}	t
2N6397	12 V	250 A	1.5 ms
2N6507	30 V	800 A	1.5 ms

To determine the effect of gate drive on the SCRs, three devices from each line were characterized at non-destruct levels using three different capacitors (200, 6,000, and 22,000 μF), three different capacitor voltages (10, 20, and 30 V), and three different gate drives ($I_{GT}(\text{MAX})$, 5 $I_{GT}(\text{MAX})$, and a ramp $I_{GT}(\text{MAX})$ with a di/dt of

about 1 mA/ μs). Due to its energy limitations, the MCR68 was tested with only 10 V across the larger capacitors.

The slow ramp, I_{GT} , was used to simulate overvoltage sense applications where the gate trigger rise time can be slow such as with a coupling zener diode.

No difference in SCR current characteristics were noted with the different gate current drive conditions; the peak currents were a function of capacitor voltage and circuit impedance, the fall times related to RTC, and the rise times, t_r , and di/dt , were more circuit dependent (wiring inductance) and less device dependent (SCR turn-on time, t_{on}). Since the wiring inductance limits, t_r , the effect of various I_{GT} s was masked, resulting in virtually identical waveforms.

The derated surge current, derived from a single (or low number) pulse test, does not truly reflect what a power supply crowbar SCR might have to see over the life of the supply. Life testing over many cycles have to be performed; thus, the circuit described in Appendix IV was developed. This life test fixture can simultaneously test ten SCRs under various crowbar energy and gate drive conditions.

Table 5.4. Specified and Measured Current Characteristics of Three SCRs

Device	Case	Maximum Specified Values					Measured Crowbar Surge Current i_{pk}		
		$I_{T(rms)}$ (A)	$I_{T(AV)}$ (A)	I_{TSM}^* (A)	I^2t (A^2s)	$I_{GT}(\text{Max})$ (mA)	Min (A)	Max (A)	Ave (A)
2N6397	TO-220	12	8	100	40	30	380	750	480
2N6507	TO-220	25	16	300	375	40	1050	1250	1100

* I_{TSM} = Peak Non-Repetitive Surge Current, 1/2 cycle sine wave, 8.3 ms.

Each of the illustrated SCRs of Figure 5.14(a) were tested with as many as four limiting resistors (0, 50, 100, and 240 $m\Omega$) and run for 1000 cycles at a nominal energy level. If no failures occurred, the peak current was progressively increased until a failure(s) resulted. Then the current was reduced by 10% and ten new devices were tested for 2000 cycles (about six hours at 350 cycles/hour). If this test

proved successful, the data was further derated by 20% and plotted as shown on log-log paper with a slope of $-1/4$. This theoretical slope, due to the $I^2\sqrt{t}$ one-dimensional heat-flow relationship (see Appendix VI), closely follows the empirical results. Of particular interest is that although the peak current increases with decreasing time, as expected, the I^2t actually decreases.

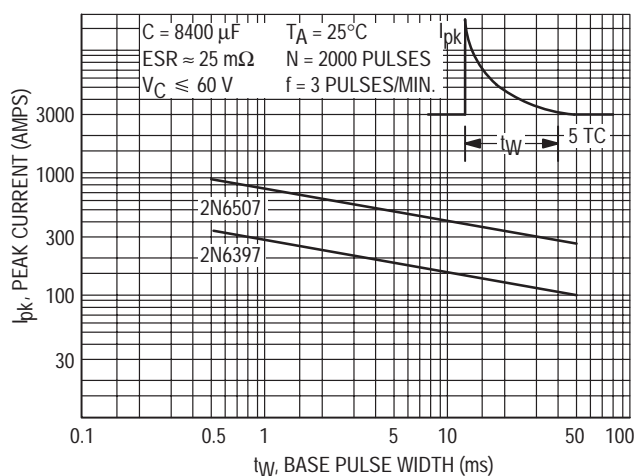


Figure 5.14(a). Peak Surge Current versus Pulse Width

Figure 5.14(b) shows the effect of elevated ambient temperature on the peak current capability of the illustrated SCRs.

FUSE CHARACTERISTICS

SCRs, like rectifiers, are generally rated in terms of average forward current, $I_T(AV)$, due to their half-wave operation. Additionally, an rms forward current, $I_T(rms)$, a peak forward surge current, I_{TSM} , and a circuit-fusing energy limit, I^2t , may be shown. However, these specifications, which are based one-half cycle 60 Hz operation, are not related to the crowbar current pulse and some means must be established to define their relationship. Also, fuses which must ultimately match the SCR and the load, are rated in rms currents.

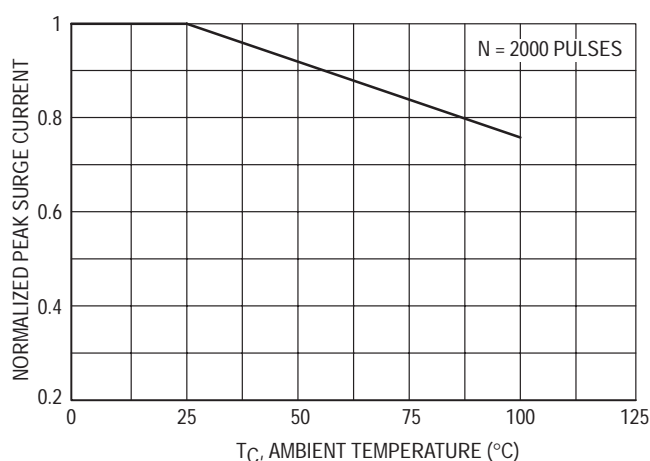
The crowbar energy curves are based on an exponentially decaying surge current waveform. This can be converted* to I_{rms} by the equation.

$$I_{rms} = 0.316 i_{pk}$$

which now allows relating the SCR to the fuse.

*See Appendix V

The logic load has its own overvoltage SOA as a function of time (Figure 5.9). The crowbar SCR must clamp the overvoltage within a specified time, and still be within its own energy rating; thus, the series-limiting resistance, R_S , in the crowbar path must satisfy both the load and SCR energy limitations. The overvoltage response time is set by the total limitations. The overvoltage response time is set by the total limiting resistance and dumped capacitor(s) time constant. Since the SOA of the TTL used in this exercise was derived by a rectangular overvoltage pulse (in effect, over-energy), the energy equivalent of the real-world exponentially falling voltage waveform must be made. An approximation can be made by using an equivalent rectangular pulse of 0.7 times the peak power and 0.7 times the base time.



(b). Peak Surge Current versus Ambient Temperature

Once an overvoltage is detected and the crowbar is enabled, in addition to sustaining the peak current, the SCR must handle the regulator short-circuit current for the time it takes to open the fuse.

Thus, all three elements are tied together — the load can take just so much overvoltage (over-energy) and the crowbar SCR must repeatedly sustain for the life of the equipment an rms equivalent current pulse that lasts for the fuse response time.

It would seem that the matching of the fuse to the SCR would be straightforward — simply ensure that the fuse rms current rating never exceed the SCR rms current rating (Figure 5.15), but still be sufficient to handle steady-state and normal overload currents. The more exact relationship would involve the energy dissipated in the system $\int I^2 R dt$, which on a comparative basis, can be reduced to I^2t . Thus, the “let-through” I^2t of the fuse should not exceed I^2t capability of the SCR under all operating conditions. These conditions are many, consisting of “available fault current,” power factor of the load, supply voltage, supply frequency, ambient temperature, and various fuse factors affecting the I^2t .

There has been much detailed information published on fuse characteristics and, rather than repeat the text which would take many pages, the reader is referred to those sources. Instead, the fuse basics will be defined and an example of matching the fuse to the SCR will be shown.

In addition to interrupting high current, the fuse should limit the current, thermal energy, and overvoltage due to the high current. Figure 5.16 illustrates the condition of the fuse at the moment the over-current starts. The peak let-through current can be assumed triangular in shape for a first-order approximation, lasting for the clearing time of the fuse. This time consists of the melting or pre-arcing time and the arcing time. The melting time is an inverse function of over-current and, at the time that the fuse element is opened, an arc will be formed causing the peak arc voltage. This arc voltage is both fuse and circuit dependent and under certain conditions can exceed the

peak line voltage, a condition the user should ensure does not overstress the electronics.

The available short-circuit current is the maximum current the circuit is capable of delivering and is generally limited by the input transformer copper loss and reactance when the crowbar SCR is placed at the input to the regulator or the regulator current limiting when placed at the output. For a fuse to safely protect the circuit, it should limit the peak let-through current and clear the fault in a short time, usually less than 10 ms.

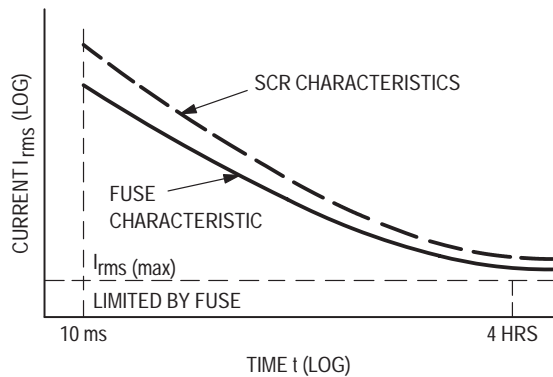


Figure 5.15. Time-Current Characteristic Curves of a Crowbar SCR and a Fuse

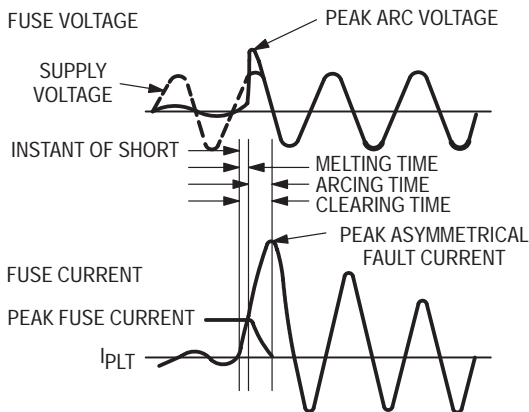


Figure 5.16. Typical Fuse Timing Waveforms During Short Circuit

Fuse manufacturers publish several curves for characterizing their products. The current-time plot, which describes current versus melting time (minimum time being 10 ms), is used in general industrial applications, but is not adequate for protecting semiconductors where the clearing time must be in the subcycle range. Where protection is required for normal multicycle overloads, this curve is useful.

Two other useful curves, the total clearing I^2t characteristic and the peak let-through current I_{PLT} characteristic, are illustrated in Figures 5.17 and 5.18 respectively. Some vendors also show total clearing time curves (overlayed on Figure 5.17 as dotted lines) which then allows direct comparison with the SCR energy limits. When this clearing time information is not shown, then the designer should determine the I_{PLT} and I^2t from the respective curves and then solve for the clearing time from the approximate equation relating these two parameters. Assuming a triangular waveform for I_{PLT} , the total clearing time, t_c , would then approximately be

$$t_c \approx \frac{3 I^2 t}{I_{PLT}^2}$$

Once t_c of the fuse is known, the comparison with the SCR can readily be made. As long as the I^2t of the fuse is less than the I^2t of the SCR, the SCR is protected. It should be pointed out that these calculations are predicated on a known value of available fault current. By inspection of Figure 5.18, it can be seen that I_{PLT} can vary greatly with available fault current, which could have a marked effect on the degree of protection. Also, the illustrated curves are for particular operating conditions; the curves will vary somewhat with applied voltage and frequency, initial loading, load power factor, and ambient temperature. Therefore, the reader is referred to the manufacturer's data sheet in those cases where extrapolation will be required for other operating conditions. The final proof is obtained by testing the fuse in the actual circuit under worst-case conditions.

CROWBAR EXAMPLE

To illustrate the proper matching of the crowbar SCR to the load and the fuse, consider the following example. A 50 A TTL load, powered by a 60 A current limited series regulator, has to be protected from transients on the supply bus by crowbarring the regulator output. The output filter capacitor of 10,000 μ F (200 μ F/A) contributes most of the energy to be crowbarred (the input capacitor is current limited by the regulator). The transients can reach 18 V for periods 100 ms.

Referring to Figure 5.9, it is seen that this transient exceeds the empirically derived SOA. To ensure safe operation, the overvoltage transient must be crowbarred within 5 ms. Since the TTL SOA is based on a rectangular power pulse even though plotted in terms of voltage, the equivalent crowbarred energy pulse should also be derived. Thus, the exponentially decaying voltage waveform should be multiplied by the exponentially decaying current to result in an energy waveform proportional to e^{-2x} . The rectangular equivalent will have to be determined and then compared with the TTL SOA. However, for simplicity, by using the crowbarred exponential waveform, a conservative rating will result.

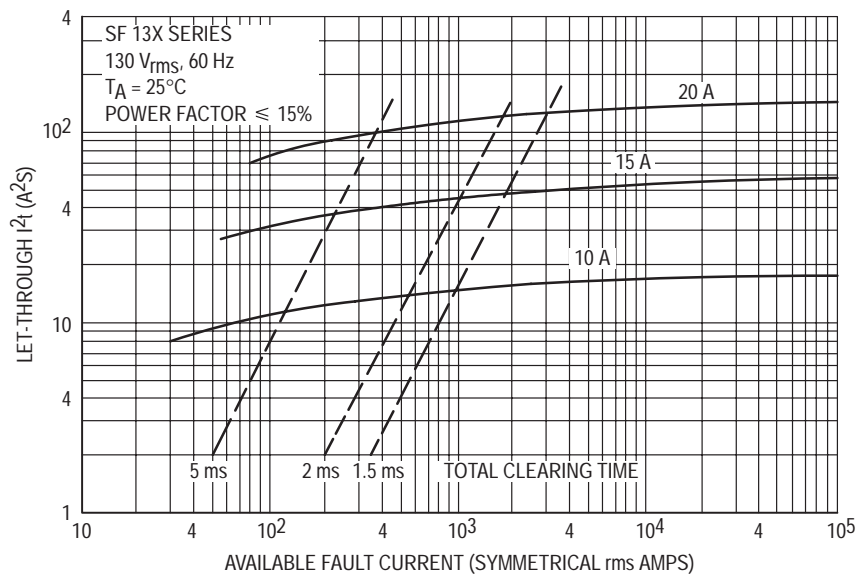


Figure 5.17. Maximum Clearing I^2t Characteristics for 10 to 20 A Fuses

To protect the SCR, a fuse must be chosen that will open before the SCR's I^2t is exceeded, the current being the regulator limiting current which will also be the available fault current to the fuse.

The fuse could be eliminated by using a 60 A SCR, but the cost versus convenience trade-off of not replacing the fuse is not warranted for this example. A second fuse or circuit breaker will protect the rectifiers and regulator for internal faults (shorts), but its selection, which is based on the respective energy limits of those components, is not part of this exercise.

If a crowbar discharge time of 3 ms were chosen, it would not only be within the rectangular pulsed SOA, but also be well within the derived equivalent rectangular model of the exponential waveform. It would also require about 1.3 time constants for the overvoltage to decay from 18 V to 5 V; thus, the RC time constant would be 3 ms/1.3 or 2.3 ms.

The limiting resistance, R_S would simply be

$$R_S = \frac{2.3 \text{ ms}}{10,000 \text{ } \mu\text{F}} = 0.23 \text{ } \Omega \cong 0.2 \text{ } \Omega$$

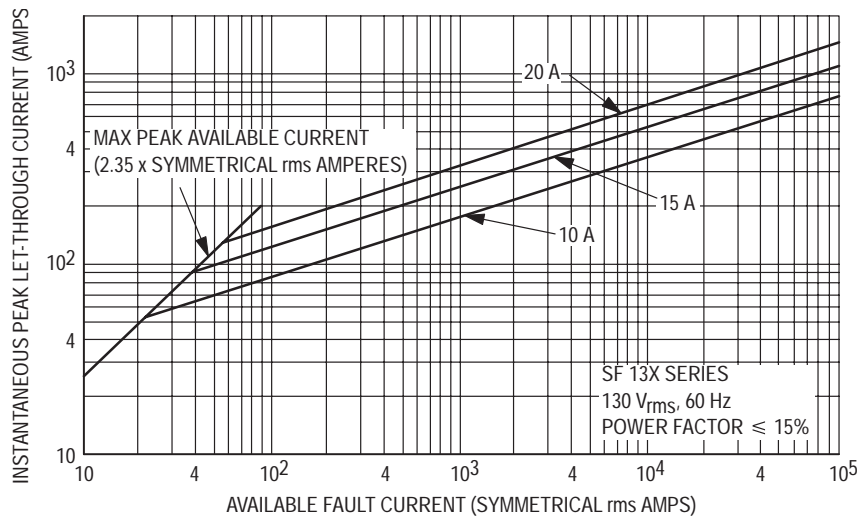


Figure 5.18. Peak Let-Through Current versus Fault Current for 10 to 20 A Fuses

Since the capacitor quickly charges up to the over-voltages V_{CC1} of 18 V, the peak capacitor discharge current would be

$$I_{pk} = \frac{V_{CC1}}{R_S} = \frac{18 \text{ V}}{0.2 \text{ } \Omega} = 90 \text{ A}$$

The rms current equivalent for this exponentially decaying pulse would be

$$I_{rms} = 0.316 I_{pk} = 0.316(90) = 28.4 \text{ A rms}$$

Now referring to the SCR peak current energy curves (Figure 5.14), it is seen that the MCR68 can sustain 210 A peak for a base time of 3 ms. This 12 A SCR must also sustain the 60 A regulator limited current for the time required to open the fuse. The MCR68 has a specified peak forward surge current rating of 100 A (1/2 cycle, sine wave, 60 Hz, non-repetitive) and a circuit fusing rating of 40 A²s.

The non-repetitive rating implies that the device can sustain 100 occurrences of this 1/2 cycle surge over the life of the device; the SCR crowbar surge current curves were based on 2000 cycles.

For the 3 ms time frame, the $I_1^2 t_1$ for the exponential waveform is

$$I_1^2 t_1 = (28.4 \text{ A})^2 (3 \text{ ms}) = 2.4 \text{ A}^2 \text{s}$$

Assuming that the fuse will open within 6 ms, the approximate energy that the SCR must sustain would be 60 A for an additional 3 ms. By superposition, this would amount to

$$I_2^2 t_2 = (60 \text{ A})^2 (6 \text{ ms}) = 21.6 \text{ A}^2 \text{s}$$

which, when added to the exponential energy, would result in 24 A²s.

The MCR68 has a 40 A²s rating based on a 1/2 cycle of 8.3 ms. Due to the one-dimensional heat flow in the device, the energy capability is not linearly related to time, but varies as to the \sqrt{t} . Therefore, with a 6 ms 1/2-cycle sine wave, the 40 A²t rating would now decrease to approximately (see Appendix VI for derivation).

$$\begin{aligned} I_2^2 t_2 &= I_1^2 t_1 \left(\frac{t_2}{t_1} \right)^{1/2} \\ &= 40 \text{ A}^2 \text{s} \left(\frac{6 \text{ ms}}{8.3 \text{ ms}} \right)^{1/2} \\ &= 34 \text{ A}^2 \text{s} \end{aligned}$$

Although the 1/2 cycle extrapolated rating is greater than the actual crowbar energy, it is only characterized for 100 cycles of operation.

To ensure 2000 cycles of operation, at a somewhat higher cost, the 25 A MCR69 could be chosen. Its exponential peak current capability, at 3 ms, is about 560 A and has a specified I_{TSM} of 300 A for 8.3 ms. The

$I^2 t$ rating is not specified, but can be calculated from the equation

$$I^2 t = \frac{(I_{TSM})^2}{2} t = \frac{(300 \text{ A})^2}{2} (8.3 \text{ ms}) = 375 \text{ A}^2 \text{s}$$

Extrapolating to 6 ms results in about 318 A²s, an $I^2 t$ rating much greater than the circuit 24 A²s value.

The circuit designer can then make the cost/performance trade-offs.

All of these ratings are predicated on the fuse operating within 6 ms.

With an available fault current of 60 A, Figure 5.17 shows that a 10 A (SF13X series) fuse will have a let-through $I^2 t$ of about 10 A²s and a total clearing time of about 6 ms, satisfying the SCR requirements, that is,

$$\begin{aligned} I^2 t_{\text{fuse}} &< I^2 t_{\text{SCR}} \\ t_c &\leq 6 \text{ ms} \end{aligned}$$

Figure 5.18 illustrates that for the same conditions, instantaneous peak let-through current of about 70 A would result. For fuse manufacturers that don't show the clearing time information, the approximate time can be calculated from the triangular model, as follows

$$t_c = \frac{3 I^2 t}{I_{PLT}^2} = \frac{3(10)}{(70)^2} = 6.1 \text{ ms}$$

The fuse is now matched to the SCR which is matched to the logic load. Other types of loads can be similarly matched, if the load energy characteristics are known.

CHARACTERIZING SWITCHES AS LINE-TYPE MODULATORS

In the past, hydrogen thyatrons have been used extensively as discharge switches for line type modulators. In general, such devices have been highly satisfactory from an electrical performance standpoint, but they have some major drawbacks including relatively large size and weight, low efficiency (due to filament power requirements), and short life expectancy compared with semiconductor devices, now can be eliminated through the use of silicon controlled rectifiers.

A line type modulator is a modulator whose output-pulse characteristics are determined by a lumped-constant transmission line (pulse forming network) and by the proper match of the line impedance (PFN) to the load impedance.

A switch for this type modulator should only initiate conduction and should have no effect on pulse characteristics. This is in contrast to a hard switch modulator where output pulse characteristics are determined by the "hard" relationship of grid (base) control of conduction through a vacuum tube (transistor) switch.

Referring to the schematic (Figure 5.25), when the power supply is first turned on, no charge exists in the PFN, and energy is transferred from the power supply to the PFN via the resonant circuit comprising the charging choke and PFN capacitors. At the time that the voltage

across the PFN capacitors reaches twice the power supply voltage, current through the charging choke tries to reverse and the power supply is disconnected due to the back biased impedance of the hold-off diode. If we assume this diode to be perfect, the energy remains stored in the PFN until the discharge switch is triggered to its on state. When this occurs, assuming that the pulse transformer has been designed to match the load impedance to the PFN impedance, all energy stored in the PFN reactance will be transferred to the load if we neglect switch losses. Upon completion of the transfer of energy the switch must return to its off condition before allowing transfer of energy once again from the power supply to the PFN storage element.

OPTIMUM SWITCH CHARACTERISTICS

FORWARD BREAKOVER VOLTAGE

Device manufacturers normally apply the variable-amplitude output of a half-wave rectifier across the SCR. Thus, forward voltage is applied to the device for only a half cycle and the rated voltage is applied only as an ac peak. While this produces a satisfactory rating for ac applications, it does not hold for dc.

An estimated 90% of devices tested for minimum breakover voltage (V_{BO}) in a dc circuit will not meet the data sheet performance specifications. A switch designed for the pulse modulator application should therefore specify a minimum continuous forward breakover voltage at rated maximum leakage current for maximum device temperatures.

THE OFF SWITCH

The maximum forward leakage current of the SCR must be limited to a low value at maximum device temperature. During the period of device nonconduction it is desired that the switch offer an off impedance in the range of megohms to hundreds of megohms. This is required for two reasons: (1) to prevent diminishing the efficiency of recharge by an effective shunt path across the PFN, and (2) to prevent the bleeding off of PFN charge during the interpulse period. This second factor is especially important in the design of radar transponders wherein the period between interrogations is variable. Change of the PFN voltage during the interpulse period could result in frequency shift, pulse instabilities, and loss of power from the transmitter being modulated.

THE ON SWITCH

At present, SCR design is more limited in the achievable maximum forward sustaining voltage than in the current that the device will conduct. For this reason modulators utilizing SCRs can be operated at lower impedance levels than comparable thyatron circuits of yesterday. It is not uncommon for the characteristic impedance of the pulse forming network to be in the order

of 5 to 10 ohms or less. Operating the SCR at higher current to switch the same equivalent pulse power as a thyatron requires the SCR on impedance to be much lower so that the I^2R loss is a reasonable value, in order to maintain circuit efficiency. Low switch loss, moreover, is mandatory because internal power dissipation can be directly translated into junction-temperature-rise and associated leakage current increase which, if excessive, could result in thermal runaway.

TURN-ON TIME

In radar circuits the *pulse-power* handling capability of an SCR, rather than the normally specified *average-power* capability, is of primary importance.

For short pulses at high PRFs the major portion of semiconductor dissipation occurs during the initial turn-on during the time that the anode rises from its forward leakage value to its maximum value. It is necessary, therefore, that turn-on time be as short as possible to prevent excessive power dissipation.

The function of radar is to provide distance information measured as a function of time. It is important, therefore, that any delay introduced by a component be fixed in relation to some variable parameter such as signal strength or temperature. For radar pulse modulator applications, a minimal delay variation versus temperature is required and any such variation must be repetitive from SCR to SCR, in production lots, so that adequate circuit compensation may be provided.

PULSE GATE CURRENT TO FIRE

The time of delay, the time of rise, and the delay variation versus temperature associated with SCR turn-on are functions of the gate triggering current available and the trigger pulse duration. In order to predict pulse circuit operation of the SCR, the pulse gate current required to turn the device on when switching the low-impedance modulator should be specified and the limits of turn-on-time variation for the specified pulse trigger current and collector load should be given at the high and low operating temperature extremes.

RECOVERY TIME

After the cessation of forward conducting current in the on device, a time of SCR circuit isolation must be provided to allow the semiconductor to return to its off state. Recovery time cannot be given as an independent parameter of device operation, but must include factors as determined by the external circuit, such as: (1) pulse current and rate of decay; (2) availability of an inverse voltage immediately following pulse-current conduction; (3) level of base bias following pulse current conduction; (4) rate of rise of reapplied positive voltage and its amplitude in relation to SCR breakover voltage; and (5) maximum circuit ambient temperature.

In the reverse direction the controlled rectifier behaves like a conventional silicon diode. Under worst circuit conditions, if an inverse voltage is generated through the existence of a load short circuit, the current available will be limited only by the impedance of the pulse forming network and SCR inverse characteristics. The reverse current is able to sweep out some of the carriers from the SCR junctions. Intentional design of the load impedance to something less than the network impedance allows development of an inverse voltage across the SCR immediately after pulse conduction, enhancing switch turn-off time. Careful use of a fast clamp diode in series with a fast zener diode, the two in shunt across the SCR, allows application of a safe value of circuit-inverse-voltage without preventing the initial useful reverse current. Availability of a negative base-bias following pulse current conduction provides a similar enhancement of switch turn-off time.

If removal of carriers from the SCR junction enables a faster switch recovery time, then, conversely, operation of the SCR at high temperatures with large forward currents and with slow rate of current decay all increase device recovery time.

HOLDING CURRENT

One of the anomalies that exist in the design of a pulse SCR is the requirement for a high holding current. This need can be determined by examining the isolation component that disconnects the power supply from the discharge circuit during the time that PFN energy is being transferred to the transmitter and during the recovery time of the discharge switch. An inductance resonating with the PFN capacitance at twice the time of recharge is normally used for power supply isolation. Resonant charging restricts the initial flow of current from the power supply, thereby maximizing the time at which power supply current flow will exceed the holding current of the SCR. If the PFN recharge current from the power supply exceeds the holding current of the SCR before it has recovered, the SCR will again conduct without the application of a trigger pulse. As a result continuous conduction occurs from the power supply through the low impedance path of the charging choke and on switch. This lock-on condition can completely disable the equipment employing the SCR switch.

The charging current passed by the inductance is given as (the PFN inductance is considered negligible):

$$i_c(t) = \frac{E_{bb} - V_n(0)}{\sqrt{L_c/C_n}} \left[\frac{\cos \frac{T_r - 2t}{2\sqrt{L_c C_n}}}{\sin \frac{T_r}{2\sqrt{L_c C_n}}} \right]$$

Where

E_{bb} = power supply voltage

$V_n(0)$ = 0 volts if the PFN employs a clamp diode or is matched to the load

T_r = time of resonant recharge and is usually equal to $\frac{1}{PRF}$

L_c = value of charging inductance

C_n = value of total PFN capacity

For a given radar pulse modulator design, the values of power supply voltage, time of resonant recharge, charging choke inductance, and PFN capacitance are established. If the time (t) represents the recovery time of the SCR being used as the discharge switch, i_c then represents the minimum value of holding current required by the SCR to prevent power supply lock-on. Conversely, if the modulator design is about an existing SCR where holding current, recovery time, and forward breakover voltage are known, the charge parameters can be derived by rewriting the above formula as follows:

$$i_H = \frac{V_{BO} - V_n(0)}{\sqrt{L_c/C_n}} \left[\frac{\cos \frac{T_r - 2(\text{recovery time})}{2\sqrt{L_c C_n}}}{\sin \frac{T_r}{2\sqrt{L_c C_n}}} \right]$$

The designer may find that for the chosen SCR the desired characteristics of modulator pulse width and pulse repetition frequency are not obtainable.

One means of increasing the effective holding current of an SCR is for the semiconductor to exhibit some turn-off gain characteristic for the residual current flow at the end of the modulator pulse. The circuit designer then can provide turn-off base current, making the SCR more effective as a pulse circuit element.

THE SCR AS A UNIDIRECTIONAL SWITCH

When triggered to its on state, the SCR, like the hydrogen thyatron, is capable of conducting current in one direction. A load short circuit could result in an inverse voltage across the SCR due to the reflection of voltage from the pulse forming network. The circuit designer may wish to provide an intentional load-to-PFN mismatch such that some inverse voltage is generated across the SCR to enhance its turn-off characteristics. Nevertheless, since the normal circuit application is unidirectional, the semiconductor device designer could take advantage of this fact in restricting the inverse-voltage rating that the SCR must withstand. The circuit designer, in turn, can accommodate this lack of peak-inverse-voltage rating by use of a suitable diode clamp across the PFN or across the SCR.

SCRs TESTS FOR PULSE CIRCUIT APPLICATION

The suitability for pulse circuit applications of SCRs not specifically characterized for such purposes can be determined from measurements carried out with relatively simple test circuits under controlled conditions. Applicable test circuits and procedures are outlined in the following section.

FORWARD BLOCKING VOLTAGE AND LEAKAGE CURRENT

Mount the SCRs to a heat sink and connect the units to be tested as shown in Figure 5.21. Place the assembly in an oven and stabilize at maximum SCR rated temperature. Turn on the power supply and raise the voltage to rated V_{BO} . Allow units to remain with the voltage applied for minimum of four hours. At the end of the temperature soak, determine if any units exhibit thermal runaway by checking for blown fuses (without removing the power). Reject any units which have blown circuit fuses. The forward leakage current, I_{LF} , of the remaining units may be calculated after measuring the voltage V_L , across resistor R2. Any units with a leakage current greater than manufacturer's rating should be rejected.

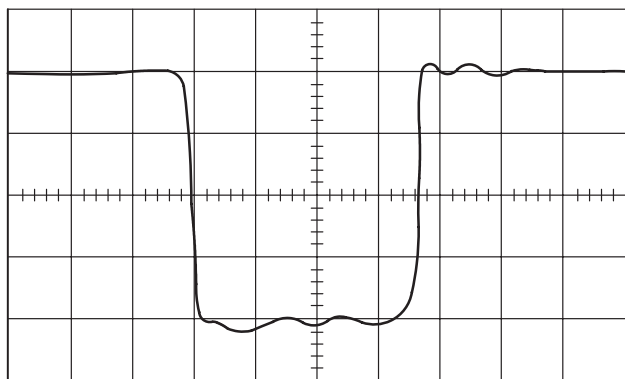


Figure 5.20. Vertical Set to 4 cm, Horizontal 0.2 μ s/cm. Detected RF Magnetron Pulse

TURN-ON TIME, VARIATION AND ON IMPEDANCE

This circuit assumes that the pulse gate current required to switch a given modulator load current is specified by the manufacturer or that the designer is able to specify the operating conditions. Typical operating values might be:

Time of trigger pulse $t = 1 \mu$ s

Pulse gate current $I_G = 200$ mA

Forward blocking voltage $V_{BO} = 400$ V

Load current $I_{Load} = 30$ A

To measure turn-on time using a Tektronix 545 oscilloscope (or equivalent) with a dual trace type CA plug-in, connect probes of Channels A and B to Test Points A and B. Place the Mode selector switch in the Added Algebraically position and the Channel B Polarity switch in the Inverted position. Adjust the HR212A pulse generator to give a positive pulse 1 μ s wide (100 pps) as viewed at Test Point A. Adjust the amplitude of the "added" voltage across the 100-ohm base resistor for the specified pulse gate current (200 mA in this example).

Switch the Mode selector knob to the alternate position. Connect Channel A to Test Point D. Leave the oscilloscope probe, Channel B, at Test Point B, thereby displaying the input trigger waveform. Measure the time between the 50 percent voltage amplitudes of the two waveforms. This is the Turn-On Time ($t_D + t_R$).

To measure turn-on time versus temperature, place the device to be tested on a suitable heat sink and place the assembly in a temperature chamber. Stabilize the chamber at minimum rated (cold) temperature. Repeat the above measurements. Raise the chamber temperature to maximum rated (hot) temperature and stabilize. Repeat the measurements above.

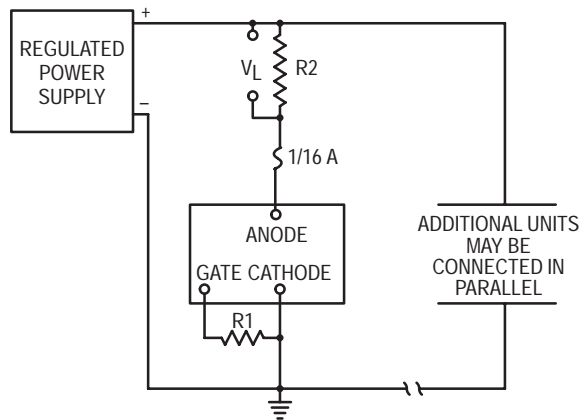


Figure 5.21. Test Setup for SCR Forward Blocking Voltage and Leakage Current Measurements

RESISTOR R1 IS USED ONLY IF MANUFACTURER CALLS FOR BIAS RESISTOR BETWEEN GATE AND CATHODE. RESISTOR R2 CAN HAVE ANY SMALL VALUE WHICH, WHEN MULTIPLIED BY MAXIMUM ALLOWABLE LEAKAGE CURRENT, WILL PROVIDE A CONVENIENT READING OF VOLTAGE V_L .

To measure the turn-on impedance for the specified current load, the on impedance can be measured as an SCR forward voltage drop. The point in time of measurement shall be half the output pulse width. For a 1 μ s output pulse, the measurement procedure would be:

Connect the oscilloscope probe, Channel B, to Point D shown in Figure 5.22. Use the oscilloscope controls Time/CM and Multiplier to a setting of 0.5 μ s per centimeter or faster. With the Amplitude Control set to view 100 volts per centimeter (to prevent amplifier overloading) measure the amplitude of the voltage drop, V_F , across the SCR 0.5 μ s after the PFN voltage waveform has dropped to half amplitude. It may be necessary to check ground reference several times during this test to provide the needed accuracy of measurement.

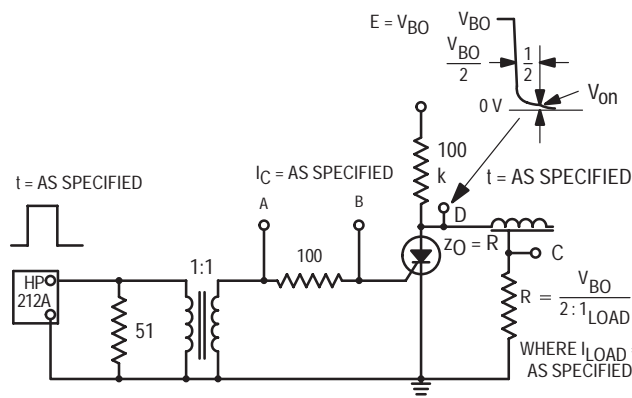


Figure 5.22. Suggested Test Circuit for SCR "On" Measurements

HOLDING CURRENT

The SCR holding current can be measured with or without a gate turn-off current, according to the position of switch S2. The ON Semiconductor Trigger Pulse Generator is a transistor circuit capable of generating a 1.5 μ s turn-on pulse followed by a variable-duration turn-off pulse. Measurements should be made at the maximum expected temperature of operation. Resistor R1 should be chosen to allow an initial magnitude of current flow at the device pulse current rating.

To measure holding current, connect the SCRs under test as illustrated in Figure 5.23. Place SCRs in oven and stabilize at maximum expected operating temperature. View the waveform across R1 by connecting the oscilloscope probe (Tektronix 2465) Channel A to Point A, and Channel B to Point B. Place the Mode Selector switch in the Added Algebraically position. Place the Polarity switch of Channel B in the Inverted position. Adjust both Volts/CM switches to the same scale factor, making sure that each Variable knob is in its Calibrated position. Adjust pulse generator for a positive pulse, 1 μ s wide, and 1,000 pps pulse repetition frequency. Adjust power supply voltage to rated V_{BO} . Adjust input pulse amplitude until unit fully triggers. Measure amplitude of voltage drop across R1, $V(A - B)$, and calculate holding current in mA from the equation

$$mA = \frac{V(A - B)}{R1} + \frac{V_{BO}}{100 \text{ k } \Omega}$$

Any unit which turns on but does not turn off has a holding current of less than

$$\frac{V_{BO} \text{ V}}{100 \text{ k } \Omega}$$

The approximate voltage setting to view the amplitude of the holding current will be 10 or 20 volts per centimeter. The approximate sweep speed will be 2 to 5 μ s per centimeter. These settings will, of course, vary, depending upon the holding current of the unit under test.

SCR recovery time is greatly dependent upon the circuit in which the device is used. However, any test of SCR recovery time should suffice to compare devices of various manufacturers, as long as the test procedure is standardized. Further evaluation of the selected devices could be made in an actual modulator circuit tester wherein techniques conducive to SCR turn-off are used. The circuit setup shown in Figures 5.24 and 5.25 can be employed for such tests. A slight load to PFN mismatch is called for to generate an inverse voltage across the SCR at the termination of the output pulse. An SCR gate turn-off pulse is used. The recharge component is a charging choke, providing optimized conditions of reapplied voltage to the PFN (and across the SCR). Adequate heat sinking of the SCR should be provided.

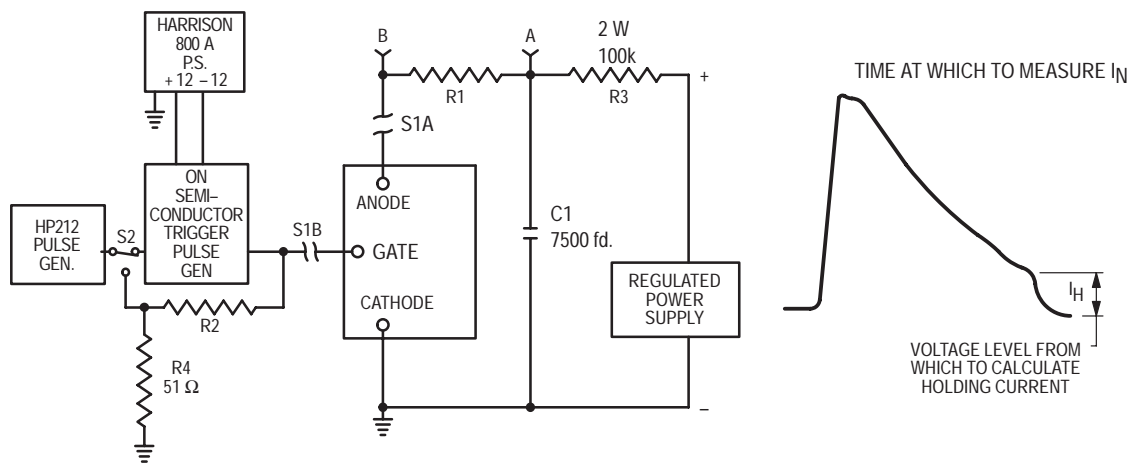


Figure 5.23. Test Setup for Measuring Holding Current

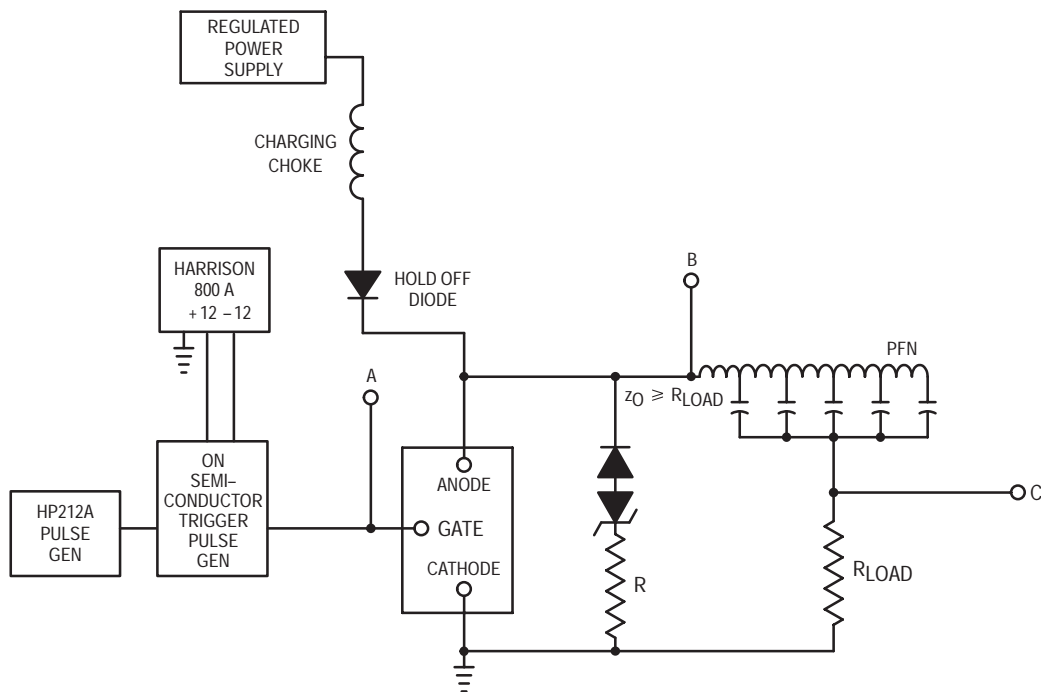


Figure 5.24. Modulator Circuit for SCR Tests

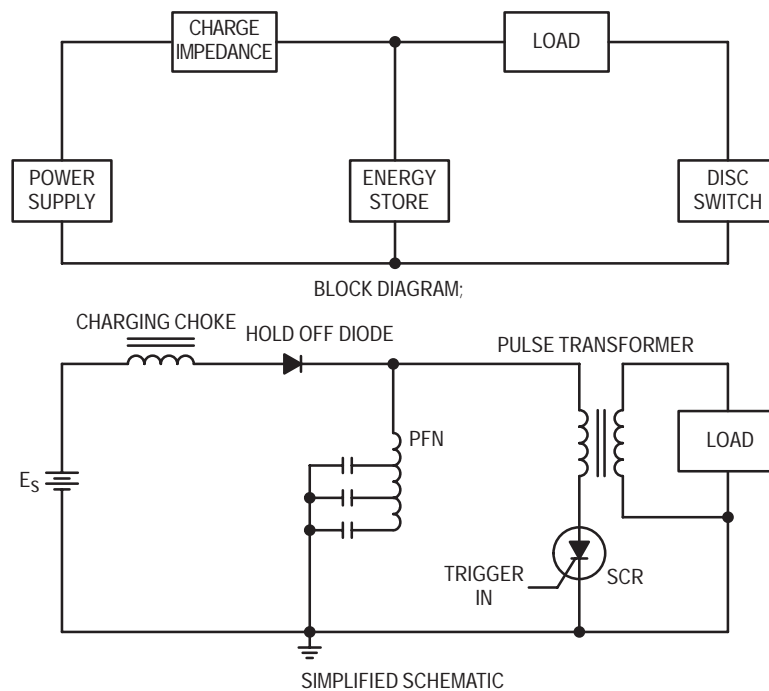


Figure 5.25. Radar Modulator, Resonant Line Type

PARALLEL CONNECTED SCRs

When an application requires current capability in excess of a single economical SCR, it can be worthwhile to consider paralleling two or more devices. To help determine if two or more SCRs in parallel are more cost effective than one high current SCR, some of the advantages and disadvantages are listed for parallel devices.

Advantages

1. Less expensive to purchase
2. Less expensive to mount
3. Less expensive to replace, in case of failure
4. Ease of mounting
5. Ease of isolation from sink

Disadvantages

1. Increased SCR count
2. Selected or matched devices
3. Increased component count
4. Greater R & D effort

There are several factors to keep in mind in paralleling and many are pertinent for single SCR operations as well.

GATE DRIVE

The required gate current (I_{GT}) amplitude can vary greatly and can depend upon SCR type and load being switched. As a general rule for parallel SCRs, I_{GT} should

be at least two or three times the $I_{GT}(\text{MAX})$ specification on the data sheet and ideally close to, but never exceeding, the maximum specified gate power dissipation or peak current. Adequate gate current is necessary for rapid turn-on of all the parallel SCRs and to ensure simultaneous turn-on without excessive current crowding across any of the individual die. The rise time of the gate drive pulse should be fast, ideally ≤ 100 ns. Each gate should be driven from a good current source and through its own resistor, even if transformer drive is used. Gate pulse width requirements vary but should be of sufficient width to ensure simultaneous turn-on and last well beyond the turn-on delay of the slowest device, as well as beyond the time required for latching of all devices. Ideally, gate current would flow for the entire conduction period to ensure latching under all operating conditions.

With low voltage switching, which includes conduction angles near 180° and near zero degrees, the gate drive requirements can be more critical and special emphasis may be required of gate pulse amplitude and width.

PARAMETER MATCHING

For reliable current sharing with parallel SCRs, there are certain device parameters that should be matched or held within close tolerances. The degree of matching required varies and can be affected by type of load (resistive, inductive, incandescent lamp or phase controlled loads) being switched.

The most common device parameters that can effect current sharing are:

1. t_d — turn-on delay time
2. t_r — turn-on rise time of anode current
3. $V_A(\text{MIN})$ — minimum anode voltage at which device will turn on
4. Static on-state voltage and current
5. I_L — Latching current

The four parameters shown in Table 5.6 were measured with a curve tracer and are:

I_L , latching current; V_{TM} , on-state voltage; I_{GT} and V_{GT} , minimum gate current and voltage for turn on. Of the four parameters, I_L and V_{TM} can greatly affect current sharing.

The latching current of each SCR is important at turn-on to ensure each device turns on and will stay on for the entire conduction period. On-state voltage determines how well the SCRs share current when cathode ballasting is not used.

Table 5.5 gives turn-on delay time (t_d) and turn-on rise time (t_r) of the anode-cathode voltage and the minimum forward anode voltage for turn-on. These parameters were measured in the circuits shown in Figures 5.28 and 5.29. One SCR at a time was used in the circuit shown in Figure 5.28.

Turn-on delay on twenty-five SCRs was measured (only ten are shown in Table 5.5) and they could be from one or more production lots. The variation in t_d was slight and ranged from 35 to 44 ns but could vary considerably on other production lots and this possible variation in t_d would have to be considered in a parallel application.

Waveforms for minimum anode voltage for turn-on are shown in Figure 5.26. The trailing edge of the gate current pulse is phase delayed (R_3) so that the SCR is not turned on. The width of the gate current pulse is now increased (R_5) until the SCR turns on and the forward anode voltage switches to the on-state at about 0.73 V. This is the minimum voltage at which this SCR will turn on with the circuit conditions shown in Figure 5.28.

For dynamic turn-on current sharing, t_d , t_r and $V_A(\text{MIN})$ are very important. As an example, with a high wattage incandescent lamp load, it is very important that the inrush current of the cold filament be equally shared by the parallel SCRs. The minimum anode voltage at which a device turns on is also very important. If one of the parallel devices turns on before the other devices and its on-state voltage is lower than the required minimum anode voltage for turn-on of the unfired devices, they therefore cannot turn on. This would overload the device which

turned on, probably causing failure from over-current and excessive junction temperature.

Table 5.5. MCR12D Turn-On Delay, Rise Time and Minimum Forward Anode Voltage For Turn-On

Device	Turn-On Delay and Rise Time Off-State Voltage = 8 V Peak $R_L = 10 \text{ Ohms}$, $I_A \approx 6.5 \text{ A Peak}$ $I_G = 100 \text{ mA}$ (PW = 100 μs) Conduction Angle 90 Degrees		Minimum Anode Voltage For Turn-On Off-State Voltage = 4 V Peak $R_L = 0.5 \text{ Ohm}$ $I_A = 5 \text{ A}$ $I_G = 100 \text{ mA}$
	$t_d(\text{ns})$	$t_r(\mu\text{s})$	(Volts)
1	35	0.80	0.70
2	38	0.95	0.81
3	45	1	0.75
4	44	1	0.75
5	44	0.90	0.75
6	43	0.85	0.75
7	38	1.30	0.75
8	38	1.25	0.70
9	38	1	0.75
10	37	0.82	0.70

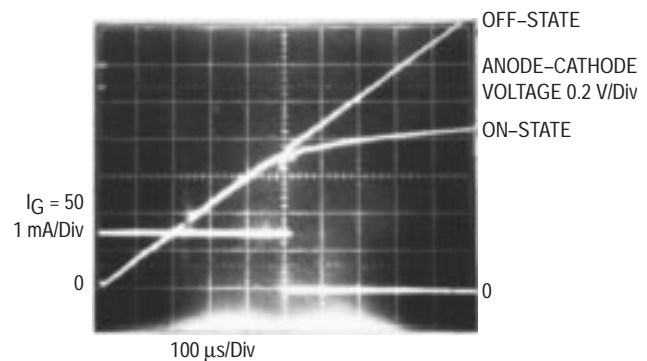


Figure 5.26. Minimum Anode Voltage For Turn-On
Off-State Voltage = 4 V Peak, $R_L = 0.5 \text{ Ohm}$,
 $I_A \approx 5 \text{ A}$, $I_G = 75 \text{ mA}$

Turn-off time — t_q is important in higher frequency applications which require the SCR to recover from the forward conduction period and be able to block the next cycle of forward voltage. Thus, t_q matching for high frequency operation can be as important as t_d , t_r and $V_A(\text{MIN})$ matching for equal turn-on current sharing.

Due to the variable in t_q measurement, no further attempt will be made here to discuss this parameter and the reader is referred to Application Note AN914.

The need for on-state matching of current and voltage is important, especially in unforced current sharing circuits.

UNFORCED CURRENT SHARING

When operating parallel SCRs without forced current sharing, such as without cathode ballasting using resistors or inductors, it is very important that the device parameters be closely matched. This includes t_d , t_r , minimum forward anode voltage for turn-on and on-state voltage matching. The degree of matching determines the success of the circuit.

In circuits without ballasting, it is especially important that physical layout, mounting of devices and resistance paths be identical for good current sharing, even with on-state matched devices.

Figure 5.27 shows how anode current can vary on devices closely matched for on-state voltage (1, 3 and 4) and a mismatched device (2). Without resistance ballasting, the matched devices share peak current within one ampere and device 2 is passing only nine amps, seven amps lower than device 1. Table 5.6 shows the degree of match or mismatch of V_{TM} of the four SCRs.

With unforced current sharing ($R_K = 0$), there was a greater tendency for one device (1) to turn-on, preventing the others from turning on when low anode switching voltage (≤ 10 V rms) was tried. Table 5.5 shows that the minimum anode voltage for turn-on is from 7 to 14% lower for device 1 than on 2, 3 and 4. Also, device 1 turn-on delay is 35 ns versus 38, 45 and 44 ns for devices 2, 3 and 4.

The tendency for device 1 to turn on, preventing the other three from turning on, is most probably due to its lower minimum anode voltage requirement and shorter turn on delay. The remedy would be closer matching of the minimum anode voltage for turn-on and driving the gates hard (but less than the gate power specifications) and increasing the width of the gate current pulse.

FORCED CURRENT SHARING

Cathode ballast elements can be used to help ensure good static on-state current sharing. Either inductors or resistors can be used and each has advantages and disadvantages. This section discusses resistive ballasting, but it should be kept in mind that the inductor method is usually better suited for the higher current levels. Although they are more expensive and difficult to design, there is less power loss with inductor ballasting as well as other benefits.

The degree of peak current sharing is shown in Figure 5.27 for four parallel MCR12D SCRs using cathode resistor ballasting with an inductive anode load. With devices 1, 3 and 4, on-state voltage is matched within 10 mV at an anode current of 15 A (See Table 5.6) and are within 1A of each other in Figure 5.27, with cathode resistance (R_K) equal to zero. As R_K increases, the current sharing becomes even closer. The unmatched device 2, with a V_{TM} of 1.41 V (Table 5.6), is not carrying

its share of current (Figure 5.29) with R_K equal zero. As R_K increases, device 2 takes a greater share of the total current and with R_K around 0.25 ohm, the four SCRs are sharing peak current quite well. The value of R_K depends on how close the on-state voltage is matched on the SCRs and the degree of current sharing desired, as well as the permissible power dissipation in R_K .

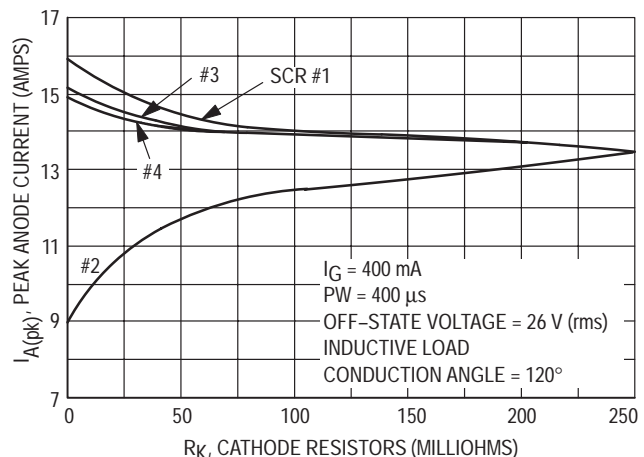


Figure 5.27. Effects Of Cathode Resistor On Anode Current Sharing

Table 5.6. MCR12D Parameters Measured On Curve Tracer, $T_C = 25^\circ\text{C}$

Device #	I_L , Latching Current $V_D = 12$ Vdc $I_G = 100$ mA	V_{TM} , On-State Voltage $I_A = 15$ A $PW = 300$ μ s	Minimum Gate Current & Voltage for Turn-On $V_D = 12$ Vdc, $R_L = 140$ Ω	
			I_{GT}	V_{GT}
1	13 mA	1.25 V	5.6 mA	0.615 V
2	27	1.41	8.8	0.679
3	28	1.26	12	0.658
4	23	1.26	9.6	0.649
5	23	1.28	9.4	0.659
6	23	1.26	9.6	0.645
7	18	1.25	7.1	0.690
8	19	1.25	7	0.687
9	19	1.25	8.4	0.694
10	16	1.25	6.9	0.679

LINE SYNCHRONIZED DRIVE CIRCUIT

Gate drive for phase control of the four parallel SCRs is accomplished with one complementary MOS hex gate, MC14572, and two bipolar transistors (Figure 5.28). This adjustable line-synchronized driver permits SCR conduction from near zero to 180 degrees. A Schmitt trigger clocks a delay monostable multivibrator that is followed by a pulse-width monostable multivibrator.

Line synchronization is achieved through the half-wave section of the secondary winding of the full-wave, center-tapped transformer (A). This winding also supplies power to the circuit through rectifiers D₁ and D₂.

The full-wave signal is clipped by diode D₅, referenced to a +15 volt supply, so that the input limit of the CMOS chip is not exceeded. The waveform is then shaped by the Schmitt trigger, which is composed of inverters U_{1-a} and U_{1-b}. A fast switching output signal B results.

The positive-going edge of this pulse is differentiated by the capacitive-resistive network of C₁ and R₂ and

triggers the delay multivibrator that is composed of U_{1-c} and U_{1-d}. As a result, the normally high output is switched low. The trailing edge of this pulse (C) then triggers the following multivibrator, which is composed of NAND gate U_{1-e} and inverter U_{1-f}. The positive going output pulse (waveform D) of this multivibrator, whose width is set by potentiometer R₆, turns on transistors Q₁ and Q₂, which drives the gates of the four SCRs. Transistor Q₂ supplies about 400 mA drive current to each gate through 100 ohm resistors and has a rise time of ≤ 100 ns.

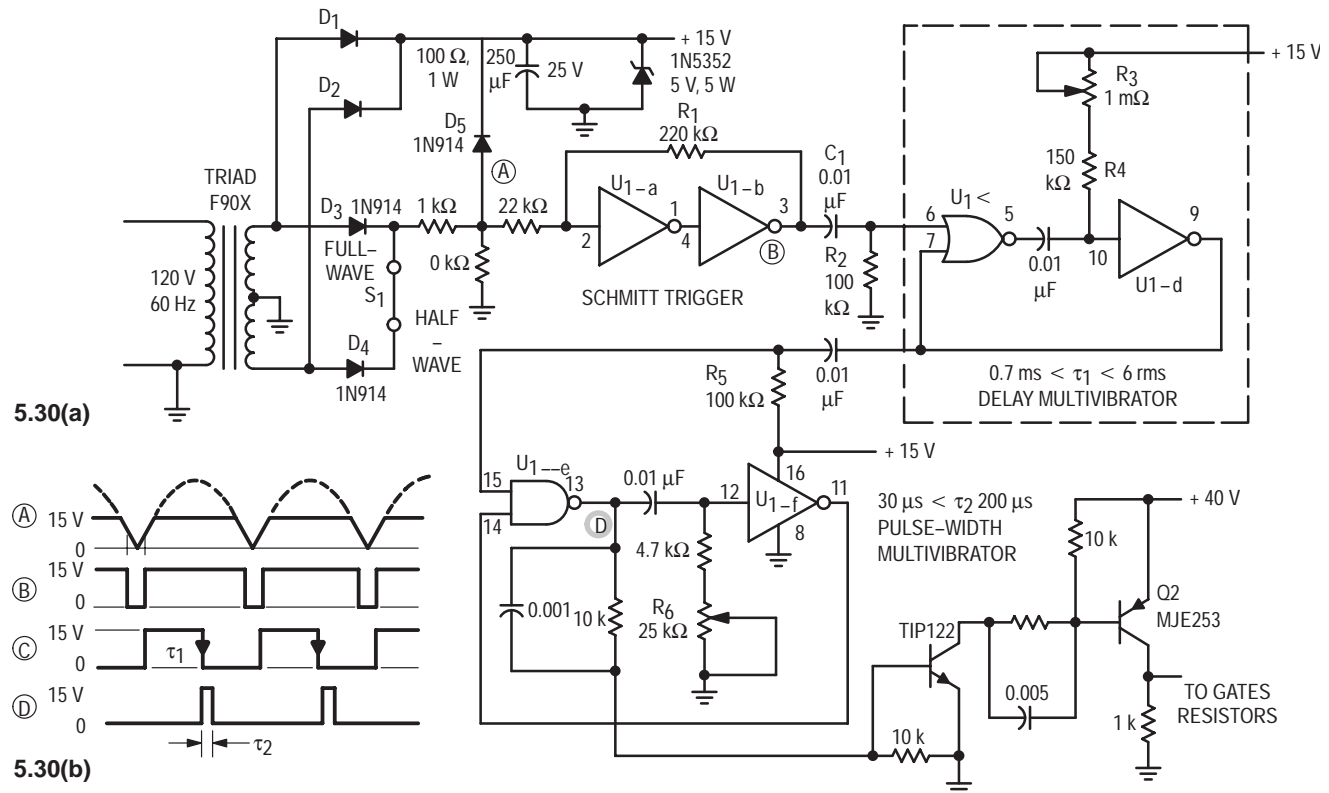


Figure 5.28. Line-Synchronized Gate Driver

PARALLEL SCR CIRCUIT

The four SCRs are MCR12Ds, housed in the TO-220 package, rated at 12 A rms, 50 V and are shown schematically in Figure 5.29. Due to line power limitations, it was decided to use a voltage step down transformer and not try working directly from the 120 V line. Also, line isolation was desirable in an experiment of this type.

The step down transformer ratings were 120 V rms primary, 26 V rms secondary, rated at 100 A, and was used with a variable transformer for anode voltage adjustment.

The inductive load consisted of four filter chokes in parallel (Stancor #C-2688 with each rated at 10 mH, 12.5 Adc and 0.11 ohm).

For good current sharing with parallel SCRs, symmetry in layout and mounting is of primary importance. The four SCRs were mounted on a natural finish aluminum heat sink and torqued to specification which is 8 inch pounds. Cathode leads and wiring were identical, and when used, the cathode resistors R_K were matched within 1%. An RC snubber network (R₇ and C₂) was connected across the anodes-cathodes to slow down the rate-of-rise of the off-state voltage, preventing unwanted turn-on.

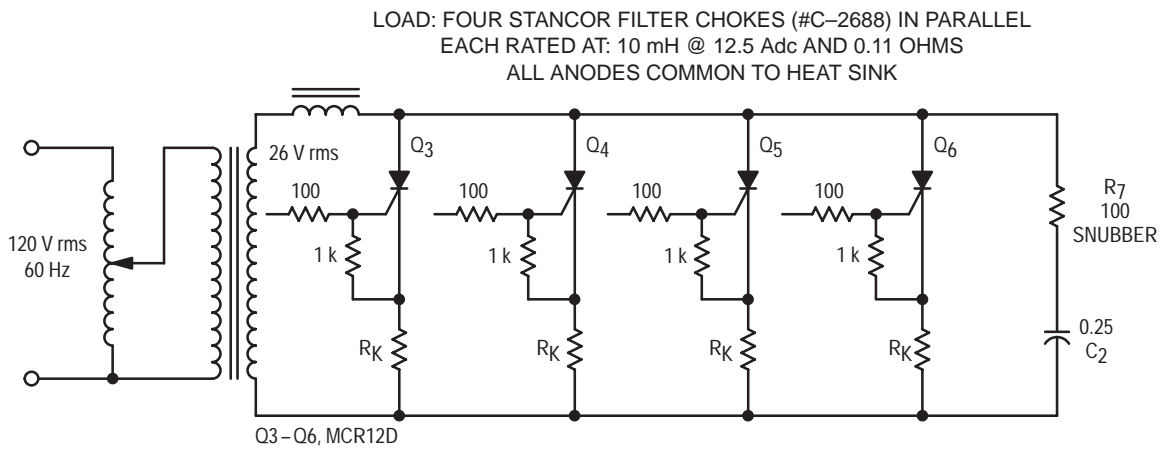


Figure 5.29. Parallel Thyristors

CHARACTERIZING RFI SUPPRESSION IN THYRISTOR CIRCUITS

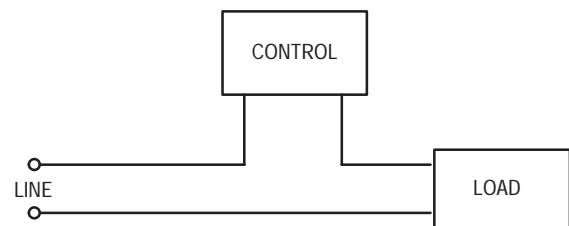
In order to understand the measures for suppression of EMI, characteristics of the interference must be explored first. To have interference at all, we must have a transmitter, or creator of interference, and a receiver, a device affected by the interference. Neither the transmitter nor the receiver need be related in any way to those circuits commonly referred to as radio-frequency circuits. Common transmitters are opening and closing of a switch or relay contacts, electric motors with commutators, all forms of electric arcs, and electronic circuits with rapidly changing voltages and currents. Receivers are generally electronic circuits, both low and high impedance which are sensitive to pulse or high frequency energy. Often the very circuits creating the interference are sensitive to similar interference from other circuits nearby or on the same power line.

EMI can generally be separated into two categories — radiated and conducted. Radiated interference travels by way of electro-magnetic waves just as desirable RF energy does. Conducted interference travels on power, communications, or control wires. Although this separation and nomenclature might seem to indicate two neat little packages, independently controllable, such is not the case. The two are very often interdependent such that in some cases control of one form may completely eliminate the other. In any case, both interference forms must be considered when interference elimination steps are taken.

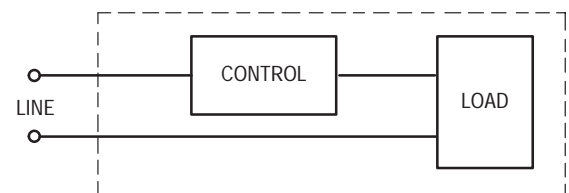
Phase control circuits using thyristors (SCRs, triacs, etc.) for controlling motor speed or resistive lighting and heating loads are particularly offensive in creating interference. They can completely obliterate most stations on any AM radio nearby and will play havoc with another control on the same power line. These controls are generally connected in one of the two ways shown in the block diagrams of Figure 5.30.

A common example of the connection of 5.30(a) is the wall mounted light dimmer controlling a ceiling mounted lamp. A motorized appliance with a built-in control such as a food mixer is an example of the connection shown in 5.30(b).

Figure 5.30(a) may be re-drawn as shown in Figure 5.31, illustrating the complete circuit for RF energy. The switch in the control box represents the thyristor, shown in its blocking state. In phase control operation, this switch is open at the beginning of each half cycle of the power line alternations. After a delay determined by the remainder of the control circuitry, the switch is closed and remains that way until the instantaneous current drops to zero. This switch is the source from which the RF energy flows down the power lines and through the various capacitors to ground.



(a). Separately Mounted Control



(b). Control and Load in the Same Enclosure

Figure 5.30. Block Diagram of Control Connections

If the load is passive, such as a lamp or a motor which does not generate interference, it may be considered as an impedance bypassed with the wire-to-wire capacitance of its leads. If it is another RF energy source, however, such as a motor with a commutator, it must be treated separately to reduce interference from that source. The power supply may be considered as dc since the interference pulse is extremely short (10 μ s) compared to the period of the power line frequency (16 ms for 60 Hz). The inductance associated with the power source comes from two separate phenomena. First is the leakage impedance of the supply transformer, and second is the self-inductance of the wires between the power line transformer and the load.

One of the most difficult parameters to pin down in the system is the effect of grounding. Most industrial and commercial wiring and many homes use a grounded conduit system which provides excellent shielding of radiated energy emanating from the wiring. However, a large number of homes are being wired with two to three wire insulated cable without conduit. In three-wire systems, one wire is grounded independently of the power system even though one of the power lines is already grounded. The capacitances to ground shown in Figure 5.31 will be greatly affected by the type of grounding used. Of course, in any home appliance, filtering must be provided suitable for all three different systems.

Before the switch in the control is closed, the system is in a steady-state condition with the upper line of the power line at the system voltage and the bottom line and the load at ground potential. When the switch is closed, the upper line potential instantaneously falls due to the line and source inductance, then it rises back to its original value as the line inductance is charged. While the upper line is rising, the line from the control to the load also rises in potential. The effect of both of these lines increasing in potential together causes an electrostatic field change which radiates energy. In addition, any other loads connected across the power lines at point A, for example, would be affected by a temporary loss of voltage created by the closing of the switch and by the line and source inductance. This is a form of conducted interference.

A second form of radiated interference is inductive coupling in which the power line and ground form a one-turn primary of an air core transformer. In this mode, an unbalanced transient current flows down the power lines with the difference current flowing to ground through the various capacitive paths available. The secondary is the radio antenna or the circuit being affected. This type of interference is a problem only when

the receiver is within about one wavelength of the transmitter at the offending frequency.

Radiated interference from the control circuit proper is of little consequence due to several factors. The lead lengths in general are so short compared to the wavelengths in question that they make extremely poor antenna. In addition, most of these control circuits are mounted in metal enclosures which provide shielding for radiated energy generated within the control circuitry.

A steel box will absorb radiated energy at 150 kHz such that any signal inside the box is reduced 12.9 dB per mil of thickness of the box. In other words, a 1/16 inch thick steel box will attenuate radiated interference by over 800 dB! A similar aluminum box will attenuate 1 dB per mil or 62.5 dB total. Thus, even in an aluminum box, the control circuitry will radiate very little energy.

Both forms of radiated interference which are a problem are a result of conducted interference on the power lines which is in turn caused by a rapid rise in current. Thus, if this current rise is slowed, all forms of interference will be reduced.

RFI SOLUTIONS

Since the switch in Figure 5.31, when it closes, provides a very low impedance path, a capacitor in parallel with it will show little benefit in slowing down the rise of current. The capacitor will be charged to a voltage determined by the circuit constants and the phase angle of the line voltage just before the switch closes. When the switch closes, the capacitor will discharge quickly, its current limited only by its own resistance and the resistance of the switch. However, a series inductor will slow down the current rise in the load and thus reduce the voltage transient on all lines. A capacitor connected as shown in Figure 5.32 will also help slow down the current rise since the inductor will now limit the current out of the capacitor. Thus, the capacitor voltage will drop slowly and correspondingly the load voltage will increase slowly.

Although this circuit will be effective in many cases, the filter is unbalanced, providing an RF current path through the capacitances to ground. It has, therefore, been found advantageous to divide the inductor into two parts and to put half in each line to the control. Figure 5.33 illustrates this circuit showing the polarity marks of two coils which are wound on the same core.

A capacitor at point A will help reduce interference further. This circuit is particularly effective when used with the connection of Figure 5.30(b) where the load is not always on the grounded side of the power line. In this case, the two halves of the inductor would be located in the power line leads, between the controlled circuit and the power source.

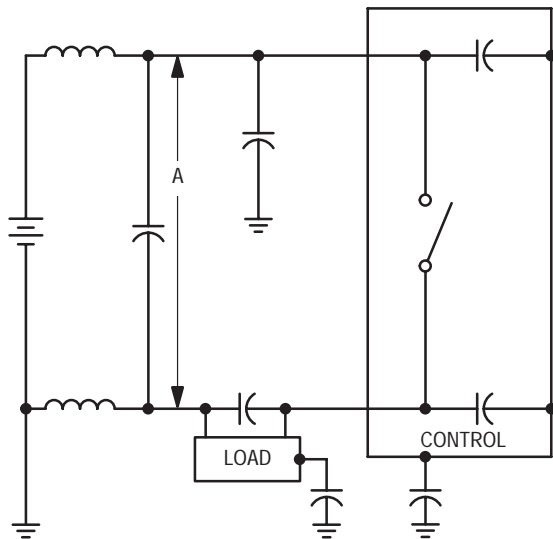


Figure 5.31. RF Circuit for Figure 5.30(a)

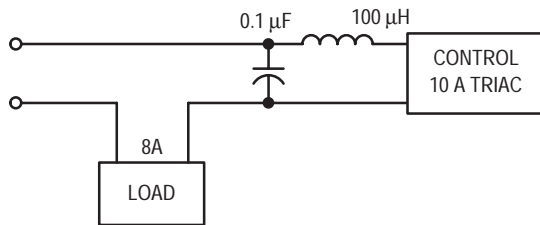


Figure 5.32. One Possible EMI Reduction Circuit

Where the control circuit is sensitive to fast rising line transients, a capacitor at point B will do much to eliminate this problem. The capacitor must charge through the impedance of the inductor, thus limiting the rate of voltage change (dv/dt) applied to the thyristor while it is in the blocking state.

DESIGN CRITERIA

Design equations for the split inductor have been developed based on parameters which should be known before attempting a design. The most difficult to determine is t_r , the minimum allowable current rise time which will not cause objectionable interference. The value of this parameter must be determined empirically in each situation if complete interference reduction is needed. ON Semiconductor has conducted extensive tests using an AM radio as a receiver and a 600 Watt thyristor lamp dimmer as a transmitter. A rate of about 0.35 Amp per μs seems to be effective in eliminating objectionable interference as well as materially reducing false triggering of the thyristor due

to line transients. The value of t_r may be calculated by dividing the peak current anticipated by the allowable rate of current rise.

Ferrite core inductors have proved to be the most practical physical configuration. Most ferrites are effective; those with highest permeability and saturation flux density are preferred. Those specifically designed as high frequency types are not necessarily desirable.

Laminated iron cores may also be used; however, they require a capacitor at point A in Figure 5.33 to be at all effective. At these switching speeds, the iron requires considerable current in the windings before any flux change can take place. We have found currents rising to half their peak value in less than one μs before the inductance begins to slow down the rise. The capacitor supplies this current for the short period without dropping in voltage, thus eliminating the pulse on the power line.

Once a core material has been selected, wire size is the next decision in the design problems. Due to the small number of turns involved (generally a single layer) smaller sizes than normally used in transformers may be chosen safely. Generally, 500 to 800 circular mills per ampere is acceptable, depending on the enclosure of the filter and the maximum ambient temperature expected.

An idea of the size of the core needed may be determined from the equation:

$$(1) A_c A_w = \frac{26 A_{wire} E_{rms} t_r}{B_{MAX}}$$

where:

A_c = the effective cross-sectional area of the core in in^2

A_w = available core window area in in^2

A_{wire} = wire cross section in circular mils

B_{MAX} = core saturation flux density in gauss

t_r = allowable current rise time in seconds

E_{rms} = line voltage

(A factor of 3 has been included in this equation to allow for winding space factor.) Once a tentative core selection has been made, the number of turns required may be found from the equation:

$$(2) N = \frac{11 E_{rms} t_r \times 10^6}{B_{MAX} A_c}$$

where:

N = the total number of turns on the core

The next step is to check how well the required number of turns will fit onto the core. If the fit is satisfactory, the core design is complete; if not, some trade-offs will have to be made.

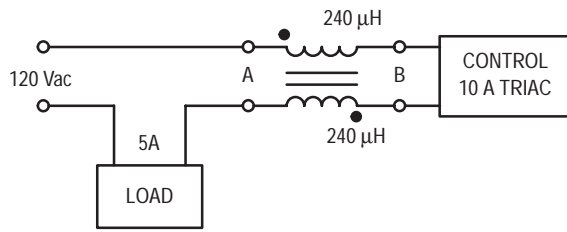


Figure 5.33. Split Inductor Circuit

In most cases, the inductor as designed at this point will have far too much inductance. It will support the entire peak line voltage for the time selected as t_r and will then saturate quickly, giving much too fast a current rise. The required inductance should be calculated from the allowable rise time and load resistance, making the rise time equal to two time constants. Thus:

$$(3) \quad \frac{2L}{R} = t_r \quad \text{or} \quad L = \frac{R t_r}{2}$$

Paper or other insulating material should be inserted between the core halves to obtain the required inductance by the equation:

$$(4) \quad l_g = \frac{3.19 N^2 A_c \times 10^{-8}}{L} - \frac{l_c}{\mu}$$

where:

l_g = total length of air gap in inches

μ = effective ac permeability of the core material at the power line frequency

l_c = effective magnetic path length of the core in inches

A_c = effective cross sectional area of the core in square inches

L = inductance in henries

DESIGN EXAMPLE

Consider a 600 watt, 120 Volt lamp dimmer using an ON Semiconductor 2N6348A triac. Line current is $\frac{600}{120} = 5$ amperes. #16 wire will provide about 516 circular mils per ampere.

For core material, type 3C5 of Ferroxcube Corporation of America, Saugerties, New York, has a high B_{max} and μ . The company specifies $B_{MAX} = 3800$ gauss and $\mu = 1900$ for material.

As was previously mentioned, a current rise rate of about 0.35 ampere per μs has been found to be acceptable for interference problems with ac-dc radios in most wiring situations. With 5 amperes rms, 7 amperes peak,

$$t_r = \frac{7}{0.35} = 20 \mu s$$

Then the equation (1):

$$A_c A_w = \frac{26 \times 2580 \times 120 \times 20 \times 10^{-6}}{3800 \text{ gauss}} = 0.044$$

Core part number 1F30 of the same company in a U-1 configuration has an $A_c A_w$ product of 0.0386, which should be close enough.

$$N = \frac{10.93 \times 120 \times 20 \times 10^{-6} \times 10^6}{3800 \times 0.137} = 42 \text{ turns}$$

Two coils of 21 turns each should be wound on either one or two legs and be connected as shown in Figure 5.33.

The required inductance of the coil is found from equation (3).

$$L = \frac{R t_r}{2} = \frac{E_{rated}}{I_{rated}} \times \frac{t_r}{2} = \frac{120}{5} \times \frac{20}{2} \times 10^{-6} = 240 \times 10^{-6}$$

$$L = 240 \mu H$$

To obtain this inductance, the air gap should be

$$l_g = \frac{3.19 \times 42^2 \times 0.137 \times 10^{-8}}{240 \times 10^{-6}} - \frac{3.33}{1900} = 0.0321 - 0.00175$$

$$l_g = 0.03035$$

Thus, 15 mils of insulating material in each leg will provide the necessary inductance.

If a problem still exists with false triggering of the thyristor due to conducted interference, a capacitor at point B in Figure 5.33 will probably remedy the situation.