File Number **1894**

IRFF430, IRFF431, IRFF432, IRFF433

N-Channel Enhancement-Mode Power Field-Effect Transistors

2.25A and 2.75A, 450V - 500V
$r_{DS(on)}$ = 1.5Ω and 2.0Ω

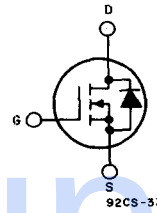
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRFF430, IRFF431, IRFF432 and IRFF433 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

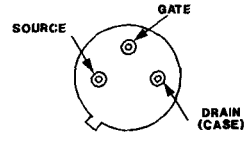
The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-205AF

Absolute Maximum Ratings

	Parameter	IRFF430	IRFF431	IRFF432	IRFF433	Units
V_{DS}	Drain – Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 20 kΩ)①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	2.75	2.75	2.25	2.25	A
I_{DM}	Pulsed Drain Current ③	11	11	9.0	9.0	A
V_{GS}	Gate – Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		11	11	9.0	9.0	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

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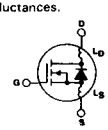
Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRFF430 IRFF432	500	–	–	V	V_{GS} = 0V
		IRFF431 IRFF433	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate – Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate – Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF430 IRFF431	2.75	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFF432 IRFF433	2.25	–	–	A	
$R_{DS(on)}$	Static Drain – Source On-State Resistance ②	IRFF430 IRFF431	–	1.3	1.5	Ω	V_{GS} = 10V, I_D = 1.5A
		IRFF432 IRFF433	–	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	30	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 225V, I_D = 1.5A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	22	30	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	17	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	11	17	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

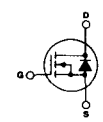


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	5.0	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF430 IRFF431	–	–	2.75	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF432 IRFF433	–	–	2.25	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF430 IRFF431	–	–	11	A	
		IRFF432 IRFF433	–	–	9.0	A	
V_{SD}	Diode Forward Voltage ②	IRFF430 IRFF431	–	–	1.4	V	T_C = 25°C, I_S = 2.75A, V_{GS} = 0V
		IRFF432 IRFF433	–	–	1.3	V	T_C = 25°C, I_S = 2.25A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	T_J = 150°C, I_F = 2.75A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.6	–	μC	T_J = 150°C, I_F = 2.75A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

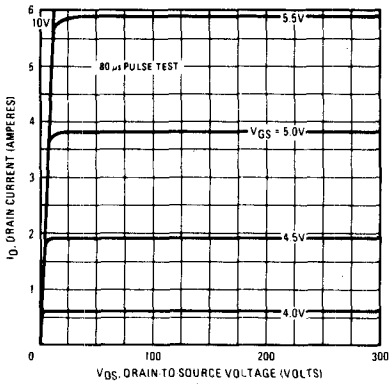


Fig. 1 - Typical output characteristics.

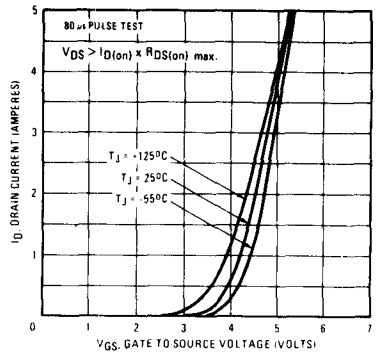


Fig. 2 - Typical transfer characteristics.

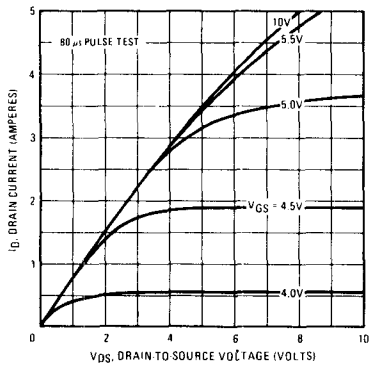


Fig. 3 - Typical saturation characteristics.

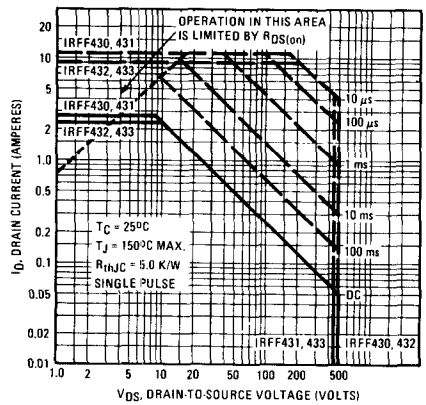


Fig. 4 - Maximum safe operating area.

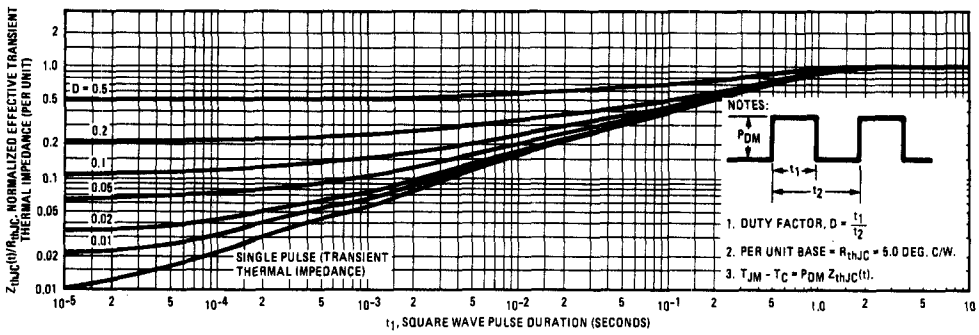


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

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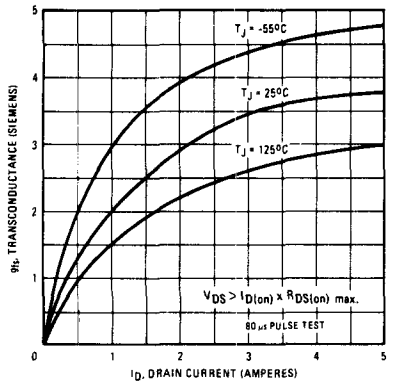

Fig. 6 - Typical transconductance vs. drain current.

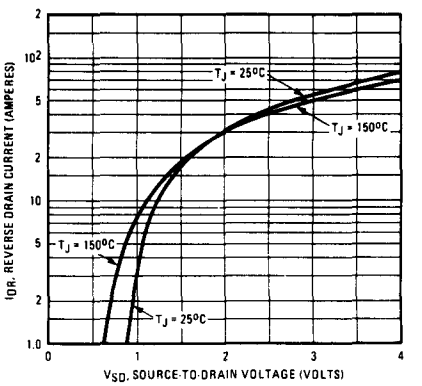

Fig. 7 - Typical source-drain diode forward voltage.

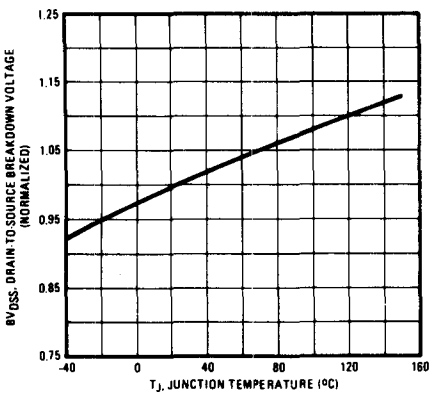

Fig. 8 - Breakdown voltage vs. temperature.

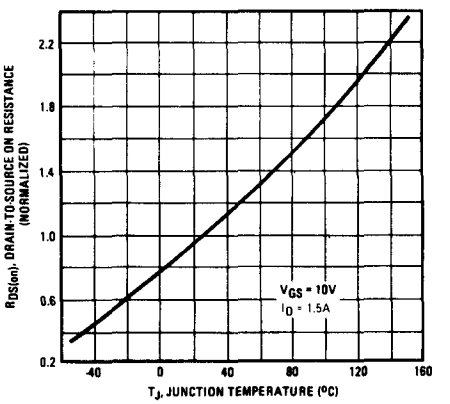

Fig. 9 - Normalized on-resistance vs. temperature.

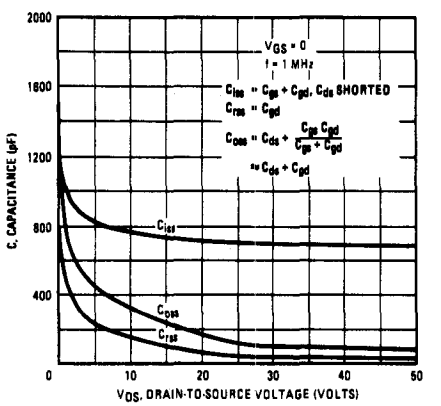

Fig. 10 - Typical capacitance vs. drain-to-source voltage.

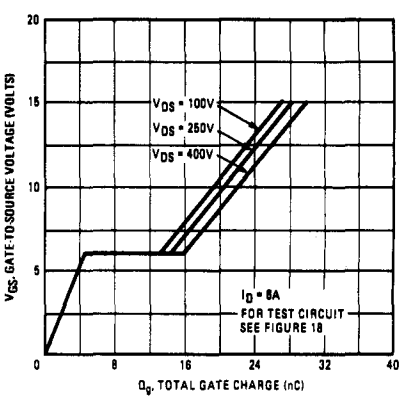

Fig. 11 - Typical gate charge vs. gate-to-source voltage.

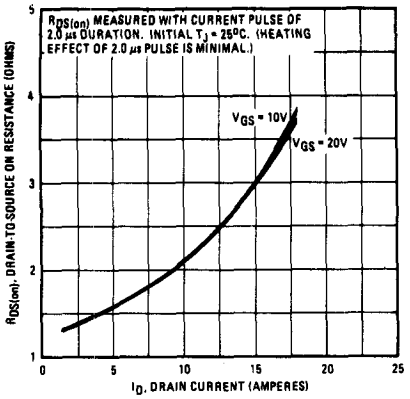

Fig. 12 - Typical on-resistance vs. drain current.

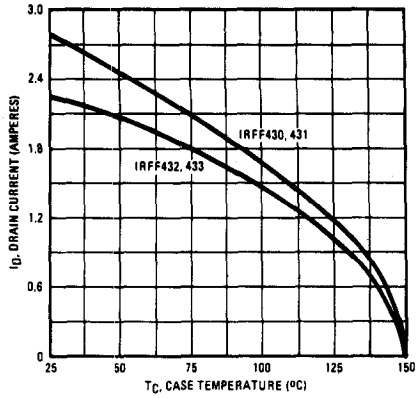

Fig. 13 - Maximum drain current vs. case temperature.

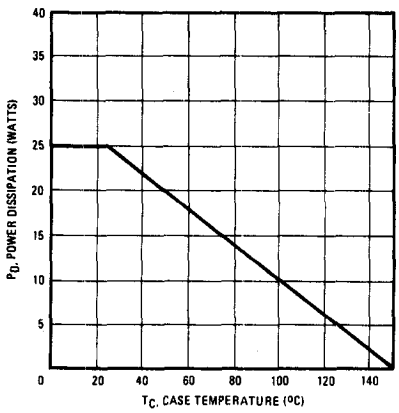

Fig. 14 - Power vs. temperature derating curve.

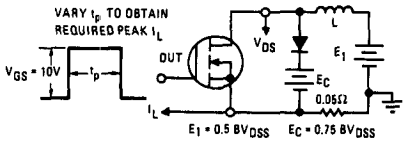

Fig. 15 - Clamped inductive test circuit.

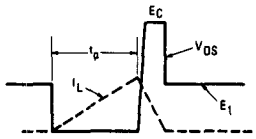

Fig. 16 - Clamped inductive waveforms.

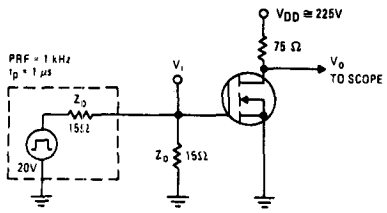

Fig. 17 - Switching time test circuit.

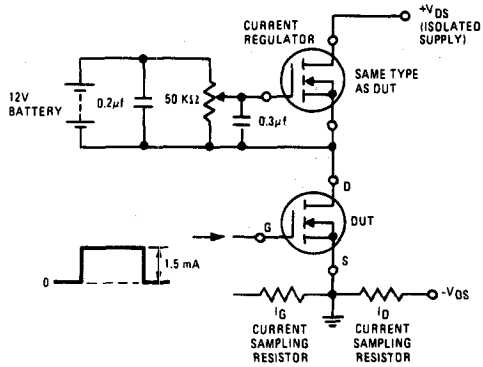

Fig. 18 - Gate charge test circuit.