

PIC18F1220/1320 Rev. D0 Silicon/Data Sheet Errata

The PIC18F1220/1320 Rev. D0 parts you have received conform functionally to the Device Data Sheet (DS39605F), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the PIC18F1220/1320 silicon.

The following silicon errata apply only to PIC18F1220/1320 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F1220	0000 0111 111	0 0111
PIC18F1320	0000 0111 110	0 0111

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: Core (DAW Instruction)

The DAW instruction may improperly clear the Carry bit (STATUS<0>) when executed.

Work around

Test the Carry bit state before executing the DAW instruction. If the Carry bit is set, increment the next higher byte to be added, using an instruction such as INCF SZ (this instruction does not affect any Status flags and will not overflow a BCD nibble). After the DAW instruction has been executed, process the Carry bit normally (see Example 1).

EXAMPLE 1: PROCESSING THE CARRY BIT DURING BCD ADDITIONS

```

MOVLW 0x80      ; .80 (BCD)
ADDLW 0x80      ; .80 (BCD)

BTFSC STATUS, C ; test C
INCF SZ byte2   ; inc next higher LSB
DAW
BTFSC STATUS, C ; test C
INCF SZ byte2   ; inc next higher LSB

This is repeated for each DAW instruction.

```

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: EUSART

The auto-baud measurement may not determine the correct baud rate if the ABDEN bit is set while the RB4/RX pin is low.

Work around

If the wake-up function is being used (WUE is set), wait for the RB4/RX pin to go high following a Break signal before setting the ABDEN bit.

If the wake-up function is not being used, ensure that RB4/RX is Idle (high between bytes) before setting the ABDEN bit.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Reset

It has been observed that in certain Reset conditions, including power-up, the first GOTO instruction at address 0x0000 may not be executed. This occurrence is rare and affects very few applications.

To determine if your system is affected, test a statistically significant number of applications across the operating temperature, voltage and frequency ranges of the application. Affected systems will repeatably fail normal testing. Systems not affected will continue to not be affected over time.

Work around

Insert a NOP instruction at address 0x0000.

Date Codes that pertain to this issue:

All engineering and production devices.

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4. Module: Oscillator (INTOSC)

The Least Significant bit of the OSCTUNE register, TUN0 (OSCTUNE<0>), is not implemented. As a result, incrementing or decrementing the OSCTUNE register will not have the expected single-step change on the frequency of INTOSC.

This is expected to be a permanent design change for the device.

Work around

For incremental changes to OSCTUNE, copy its contents to WREG, increment or decrement WREG twice, then write WREG back to OSCTUNE. This has the effect of incrementing or decrementing TUN<5:1> while maintaining TUN0 clear (the smallest possible adjustment in this silicon revision).

It is also possible to decrement OSCTUNE directly. Each direct decrement decreases the value of OSCTUNE by two (TUN0 remains clear). If incremental change is not required, OSCTUNE can also be written to directly with any value.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: Oscillator (INTRC)

The 31 kHz internal RC oscillator source (INTRC) has been configured as a separate, fixed frequency source that is calibrated at the factory. Its output is no longer tunable using the OSCTUNE register. The INTOSC source remains tunable using OSCTUNE, as previously described.

This is expected to be a permanent design change for the device.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

Clarifications/Corrections to the Data Sheet

In the PIC18F1220/1320 Device Data Sheet (DS39605F), the following clarifications and corrections should be noted:

1. Module: Timer3 (Special Event Trigger)

In **Section 14.0 “Timer3 Module”**, bit 6 of the T3CON register was incorrectly defined as unimplemented. The correct definition for T3CON<6> is T3CCP2 and is shown in **bold** below:

In all tables and references to the T3CON register throughout the document, T3CON<6> should always be interpreted as the control bit, T3CCP2, and not as an unimplemented bit position.

REGISTER 14-1: T3CON: TIMER3 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON
bit 7							bit 0

bit 6,3 **T3CCP2:T3CCP1:** Timer3 and Timer1 to CCP1 Enable bits
 1x = Timer3 is the clock source for compare/capture CCP module
 01 = **Reserved**
 00 = Timer1 is the clock source for compare/capture CCP module

2. Module: Data EEPROM

In Table 22-1 on page 254 of the Device Data Sheet, the typical value for parameter D122, Data EEPROM Erase/Write Cycle Time (TDEW) has changed. The new value is 5.5 ms and is shown in **bold** below.

TABLE 22-1: MEMORY PROGRAMMING REQUIREMENTS

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D122	TDEW	Erase/Write Cycle Time	—	5.5	—	ms	

3. Module: Oscillator Configurations

The INTOSC clock source has been modified to reduce its start-up time, and to improve its frequency stability.

The IOFS bit (OSCCON<2>) will indicate the INTOSC has settled in approximately 128 μs.

The INTOSC clock frequency is adjusted using the TUN<5:1> bits (OSCTUNE<5:1>). The TUN0 bit (OSCTUNE<0>) is no longer effective in adjusting the INTOSC frequency, although it continues to be readable and writable.

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4. Module: Oscillator Configurations

The INTRC clock source has been modified to improve its frequency stability.

The OSCTUNE register no longer affects the INTRC frequency. Peripherals that use the INTRC clock source are also affected (WDT and FSCM).

5. Module: DC Characteristics

Modifications have been made that have changed the typical values for parameters, D022A (Brown-out Reset) and D022B (Low-Voltage Detect). The new values will change the ninth and last page of the table shown.

The new values are shown in bold text.

22.1 DC Characteristics: Power-Down and Supply Current PIC18F1220/1320 (Industrial) PIC18LF1220/1320 (Industrial) (Continued)

PIC18LF1220/1320 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial					
PIC18F1220/1320 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
Param No.	Device	Typ	Max	Units	Conditions		
Module Differential Currents (ΔI_{WDT}, ΔI_{BOR}, ΔI_{LVD}, ΔI_{OSCB}, ΔI_{AD})							
D022 (ΔI_{WDT})	Watchdog Timer	1.5	4.0	μA	-40°C	VDD = 2.0V	
		2.2	4.0	μA	$+25^{\circ}\text{C}$		
		3.1	5.0	μA	$+85^{\circ}\text{C}$		
		2.5	6.0	μA	-40°C	VDD = 3.0V	
		3.3	6.0	μA	$+25^{\circ}\text{C}$		
		4.7	7.0	μA	$+85^{\circ}\text{C}$		
		3.7	10.0	μA	-40°C	VDD = 5.0V	
		4.5	10.0	μA	$+25^{\circ}\text{C}$		
		6.1	13.0	μA	$+85^{\circ}\text{C}$		
D022A (ΔI_{BOR})	Brown-out Reset	35	50	μA	-40°C to $+85^{\circ}\text{C}$	VDD = 3.0V	
		42	60	μA		VDD = 5.0V	
		Extended Devices Only	46	65	μA	-40°C to $+125^{\circ}\text{C}$	
D022B (ΔI_{LVD})	Low-Voltage Detect	31	45	μA	-40°C to $+85^{\circ}\text{C}$	VDD = 2.0V	
		33	50	μA		VDD = 3.0V	
		42	60	μA		VDD = 5.0V	
	Extended Devices Only	46	65	μA	-40°C to $+125^{\circ}\text{C}$	VDD = 5.0V	
D025 (ΔI_{OSCB})	Timer1 Oscillator	1.7	3.5	μA	-40°C	VDD = 2.0V	32 kHz on Timer1 ⁽⁴⁾
		1.8	3.5	μA	$+25^{\circ}\text{C}$		
		2.1	4.5	μA	$+85^{\circ}\text{C}$		
		2.2	4.5	μA	-40°C	VDD = 3.0V	
		2.6	4.5	μA	$+25^{\circ}\text{C}$		
		2.8	5.5	μA	$+85^{\circ}\text{C}$		
		3.0	6.0	μA	-40°C	VDD = 5.0V	
		3.3	6.0	μA	$+25^{\circ}\text{C}$		
3.6	7.0	μA	$+85^{\circ}\text{C}$				
D026 (ΔI_{AD})	A/D Converter	1.0	3.0	μA	-40°C to $+85^{\circ}\text{C}$	VDD = 2.0V	A/D on, not converting
		1.0	4.0	μA	-40°C to $+85^{\circ}\text{C}$	VDD = 3.0V	
		2.0	10.0	μA	-40°C to $+85^{\circ}\text{C}$	VDD = 5.0V	
		1.0	8.0	μA	-40°C to $+125^{\circ}\text{C}$	VDD = 5.0V	

6. Module: DC Characteristics

The operating values for the SEC_RUN and SEC_IDLE modes are corrected, on the seventh and eighth pages of the nine-page table in **Section 22.2 “DC Characteristics: Power-Down and Supply Current”**.

The new values are shown in bold text.

22.2 DC Characteristics: Power-Down and Supply Current PIC18F1220/1320 (Industrial) PIC18LF1220/1320 (Industrial)

PIC18LF1220/1320 (Industrial)		Standard Operating Conditions (unless otherwise stated)						
		Operating temperature -40°C ≤ TA ≤ +85°C for industrial						
PIC18F1220/1320 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated)						
		Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended						
Param No.	Device	Typ	Max	Units	Conditions			
Supply Current (IDD)^(2,3)								
	All devices	3.2	4.1	mA	-40°C	VDD = 4.2 V	FOSC = 40 MHz (PRI_IDLE mode, EC oscillator)	
		3.2	4.1	mA	+25°C			
		3.3	4.1	mA	+85°C			
	All devices	4.0	5.1	mA	-40°C	VDD = 5.0V		
		4.1	5.1	mA	+25°C			
		4.1	5.1	mA	+85°C			
	PIC18LF1220/1320	9.2	15	μA	-10°C	VDD = 2.0V		FOSC = 32 kHz ⁽⁴⁾ (SEC_RUN mode, Timer1 as clock)
		9.6	15	μA	+25°C			
		12.7	18	μA	+70°C			
PIC18LF1220/1320	22	30	μA	-10°C	VDD = 3.0V			
	21	30	μA	+25°C				
	20	35	μA	+70°C				
All devices	50	80	μA	-10°C	VDD = 5.0V			
	45	80	μA	+25°C				
	45	80	μA	+70°C				

Legend: Shading of rows is to assist in readability of the table.

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
- The test conditions for all IDD measurements in active operation mode are:
 OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
 MCLR = VDD; WDT enabled/disabled as specified.
- 3:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{EXT}$ (mA) with REXT in kΩ.
- 4:** Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

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22.2 DC Characteristics: Power-Down and Supply Current PIC18F1220/1320 (Industrial) PIC18LF1220/1320 (Industrial) (Continued)

PIC18LF1220/1320 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
PIC18F1220/1320 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Device	Typ	Max	Units	Conditions	
Supply Current (I_{DD})^(2,3)						
	PIC18LF1220/1320	5.1	9	μA	-10°C	V _{DD} = 2.0V V _{DD} = 3.0V V _{DD} = 5.0V F _{OSC} = 32 kHz ⁽⁴⁾ (SEC_IDLE mode, Timer1 as clock)
		5.8	9	μA	$+25^{\circ}\text{C}$	
		7.9	11	μA	$+70^{\circ}\text{C}$	
	PIC18LF1220/1320	7.9	12	μA	-10°C	
		8.9	12	μA	$+25^{\circ}\text{C}$	
		10.5	14	μA	$+70^{\circ}\text{C}$	
	All devices	12.5	20	μA	-10°C	
		16.3	20	μA	$+25^{\circ}\text{C}$	
		18.4	25	μA	$+70^{\circ}\text{C}$	

Legend: Shading of rows is to assist in readability of the table.

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD};
MCLR = V_{DD}; WDT enabled/disabled as specified.
- 3:** For RC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in k Ω .
- 4:** Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to $+70^{\circ}\text{C}$. Extended temperature crystals are available at a much higher cost.

REVISION HISTORY

Rev A Document (08/2005)

First revision of this document. Includes silicon issues 1 (Core), 2 (EUSART), 3 (Reset) and 4 (Oscillator (INTOSC Source)), and Data Sheet Clarification issues 1 (Timer3 (Special Event Trigger)) and 2 (Data EEPROM).

Rev B Document (03/2006)

Removed previous silicon issue 4 and added new silicon issues 4 (Oscillator/INTOSC) and 5 (Oscillator/INTRC). Data Sheet Clarification issue 1 (CCP) clarified as Timer3/Special Event Trigger.

Rev C Document (07/2007)

Added data sheet clarification issues 3-4 (Oscillator Configurations) and 5 (DC Characteristics).

Rev D Document (02/2009)

Added data sheet clarification issue 6 (DC Characteristics).

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NOTES:

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02/04/09