



MOTOROLA
Semiconductors



REVERSE BLOCKING TRIODE THYRISTOR

... multi-purpose PNP silicon controlled rectifiers suited for industrial, consumer, and military applications. Offered in a choice of space-saving, economical packages for mounting versatility.

- Uniform Low-Level Noise-Immune Gate Triggering –
 $I_{GT} = 10 \text{ mA (Typ) @ } T_C = 25^\circ\text{C}$
- Low Forward "On" Voltage –
 $V_T = 1.0 \text{ V (Typ) @ } 5.0 \text{ Amp @ } 25^\circ\text{C}$
- High Surge-Current Capability –
 $I_{TSM} = 100 \text{ Amp Peak}$
- Shorted Emitter Construction

MAXIMUM RATINGS

(Apply over operating temperature range and for all case types unless otherwise noted)

Rating	Symbol	Value	Unit
*Peak Repetitive Forward and Reverse Blocking Voltage (1)	V_{DRM}	25	Volts
	or	50	
	V_{RRM}	100	
	2N4167, 83,	200	
	2N4168, 84,	300	
	2N4169, 85,	400	
	2N4170, 86,	500	
	2N4171, 87,	600	
2N4172, 88,			
2N4173, 89,			
2N4174, 90,			
Forward Current RMS	$I_T(\text{RMS})$	8.0	Amp
*Peak Forward Surge Current (One cycle, 60 Hz, $T_J = -40$ to $+100^\circ\text{C}$)	I_{TSM}	100	Amp
Circuit Fusing ($T_J = -40$ to $+100^\circ\text{C}$; $t \leq 8.3 \text{ ms}$)	I^2t	40	A^2s
*Peak Gate Power	P_{GM}	5.0	Watt
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
Peak Gate Voltage (2)	V_{GM}	10	Volts
*Operating Temperature Range	T_J	-40 to $+100$	$^\circ\text{C}$
*Storage Temperature Range	T_{stg}	-40 to $+150$	$^\circ\text{C}$
Stud Torque		15	in. lb.

THERMAL CHARACTERISTICS

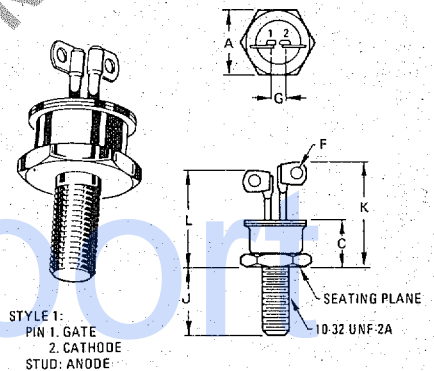
Characteristic	Symbol	Typ	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	2.5*	$^\circ\text{C/W}$
Thermal Resistance, Case to Ambient (See Fig. 11) 2N4183-98	$R_{\theta CA}$	50	—	$^\circ\text{C/W}$

- (1) Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage applied exceeds the rated blocking voltage.
 (2) Devices should not be operated with a positive bias applied to the gate concurrently with a negative potential applied to the anode.
 *Indicates JEDEC Registered Data

2N4167 thru 2N4174
2N4183 thru 2N4190

SILICON CONTROLLED RECTIFIERS

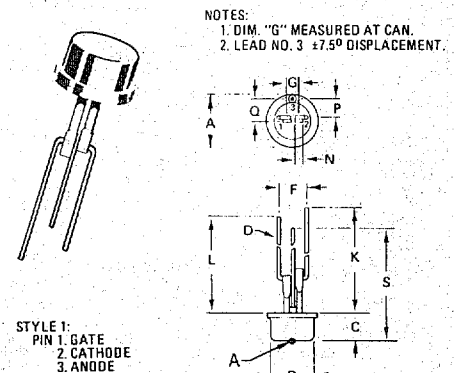
8-AMPERE RMS
25 thru 600 VOLTS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	11.10	—	0.437
C	—	7.87	—	0.310
F	—	1.78 TYP	—	0.070 TYP
G	2.29	2.79	0.090	0.110
J	10.72	11.48	0.422	0.452
K	—	16.76	—	0.660
L	—	15.49	—	0.610

NOTE:
1. DIM "G" MEASURED AT CAN.

2N4167-74
CASE 86-01



NOTES:
1. DIM. "G" MEASURED AT CAN.
2. LEAD NO. 3 $\pm 7.5^\circ$ DISPLACEMENT.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	10.92	—	0.430
B	—	8.89	—	0.350
C	—	5.97	—	0.235
D	0.76	0.86	0.030	0.034
F	4.83	5.33	0.190	0.210
G	2.29	2.79	0.090	0.110
K	33.53	—	1.320	—
L	31.50 TYP	—	1.240 TYP	—
N	1.65	1.91	0.065	0.075
P	3.43	3.68	0.135	0.145
Q	4.57	5.08	0.180	0.200
S	30.48	—	1.20	—

2N4183-90
CASE 87L-01

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current ($V_D = \text{Rated } V_{DRM}$ @ $T_J = 100^\circ\text{C}$, gate open)	I_{DRM}	—	—	2.0	mA
*Peak Reverse Blocking Current ($V_R = \text{Rated } V_{RRM}$ @ $T_J = 100^\circ\text{C}$, gate open)	I_{RRM}	—	—	2.0	mA
Gate Trigger Current (Continuous dc) (1) ($V_D = 7.0 \text{ Vdc}$, $R_L = 100 \Omega$) *($V_D = 7.0 \text{ Vdc}$, $R_L = 100 \Omega$, $T_C = -40^\circ\text{C}$)	I_{GT}	—	10	30 60	mA
Gate Trigger Voltage (Continuous dc) ($V_D = 7.0 \text{ Vdc}$, $R_L = 100 \Omega$) *($V_D = 7.0 \text{ Vdc}$, $R_L = 100 \Omega$, $T_C = -40^\circ\text{C}$) *($V_D = 7.0 \text{ Vdc}$, $R_L = 100 \Omega$, $T_J = 100^\circ\text{C}$)	V_{GT}	— 0.2	0.75	1.5 2.5	Volts
*Forward "On" Voltage (pulsed, 1.0 ms max, duty cycle $\leq 1\%$) ($I_{TM} = 15.7 \text{ A}$)	V_{TM}	—	1.4	2.0	Volts
Holding Current ($V_D = 7.0 \text{ Vdc}$, gate open) *($V_D = 7.0 \text{ Vdc}$, gate open, $T_C = -40^\circ\text{C}$)	I_H	—	10	30 60	mA
Turn-On Time ($t_d + t_r$) ($I_G = 20 \text{ mAdc}$, $I_F = 5.0 \text{ Adc}$, $V_D = \text{Rated } V_{DRM}$)	t_{on}	—	1.0	—	μs
Turn-Off Time ($I_F = 5.0 \text{ Adc}$, $I_R = 5.0 \text{ Adc}$) ($I_F = 5.0 \text{ Adc}$, $I_R = 5.0 \text{ Adc}$, $T_J = 100^\circ\text{C}$, $V_D = \text{Rated } V_{DRM}$) ($dv/dt = 30 \text{ V}/\mu\text{s}$)	t_{off}	—	15 25	—	μs
Forward Voltage Application Rate (Exponential) (Gate open, $T_J = 100^\circ\text{C}$, $V_D = \text{Rated } V_{DRM}$)	dv/dt	—	50	—	$\text{V}/\mu\text{s}$

(1) For optimum operation, i.e. faster turn-on, lower switching losses, best di/dt capability, recommended $I_{GT} = 200 \text{ mA}$ minimum.
* Indicates JEDEC Registered Data

TYPICAL TRIGGER CHARACTERISTICS

FIGURE 1 — PULSE CURRENT TRIGGERING

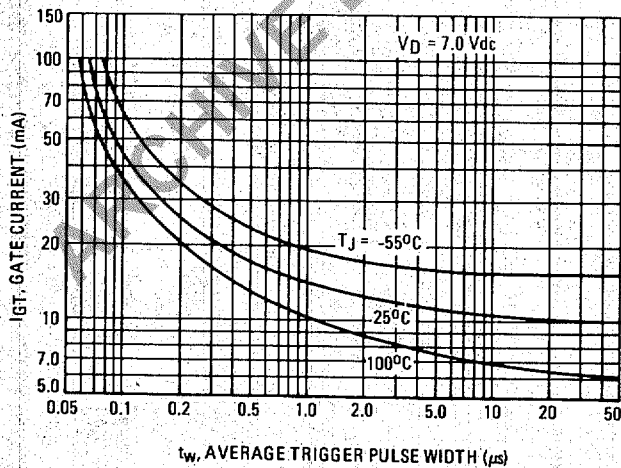
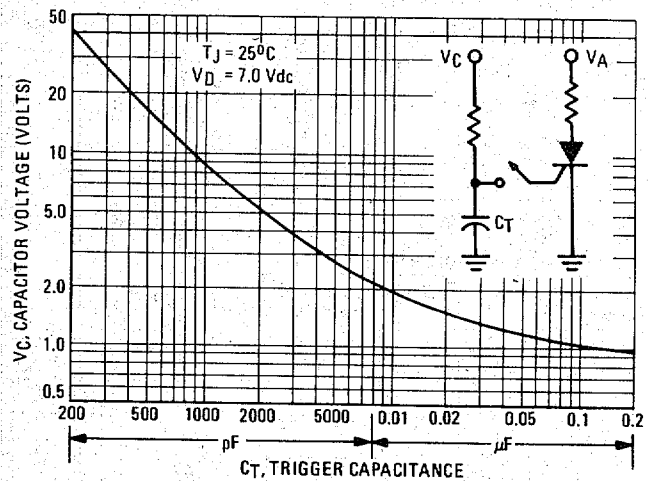


FIGURE 2 — CAPACITIVE DISCHARGE TRIGGERING



CURRENT DERATING

FIGURE 3 - MAXIMUM CASE TEMPERATURE

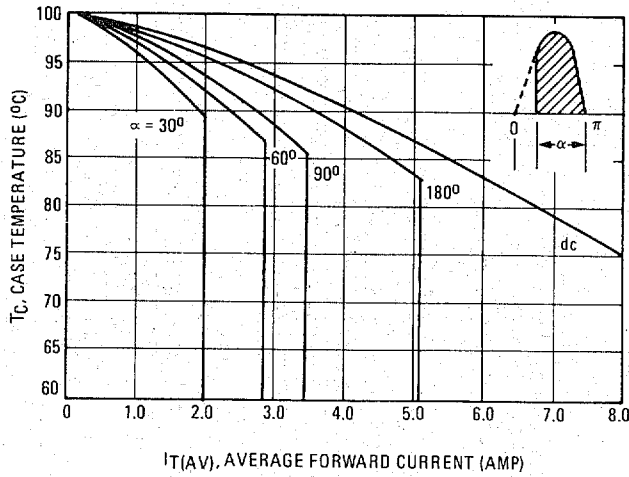


FIGURE 4 - MAXIMUM AMBIENT TEMPERATURE

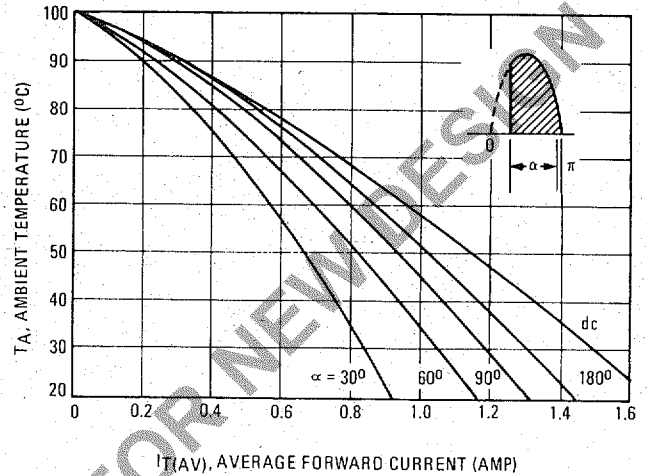


FIGURE 5 - POWER DISSIPATION

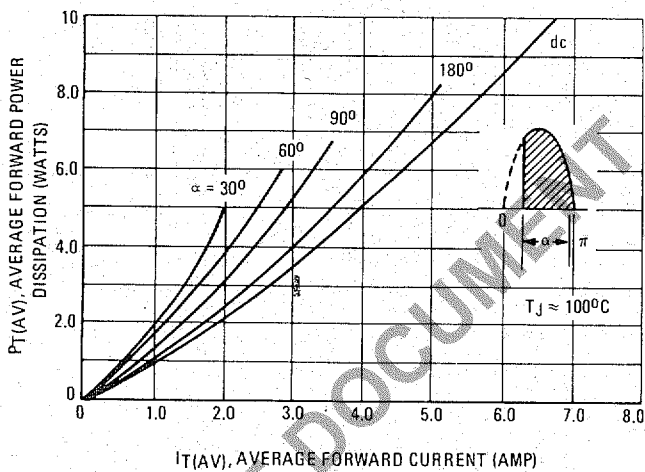


FIGURE 6 - MAXIMUM SURGE CAPABILITY

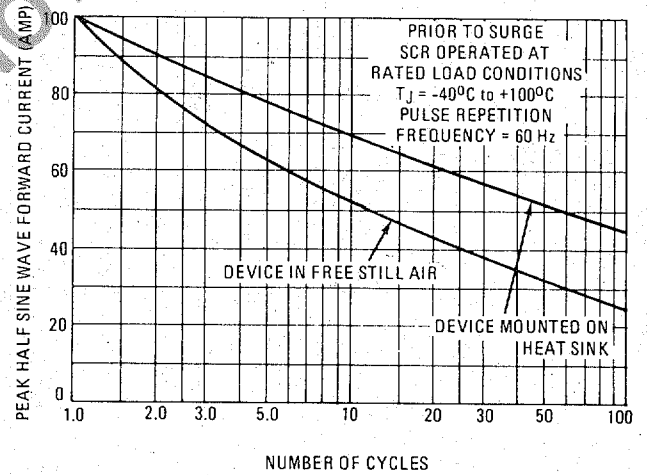


FIGURE 7 - THERMAL RESPONSE

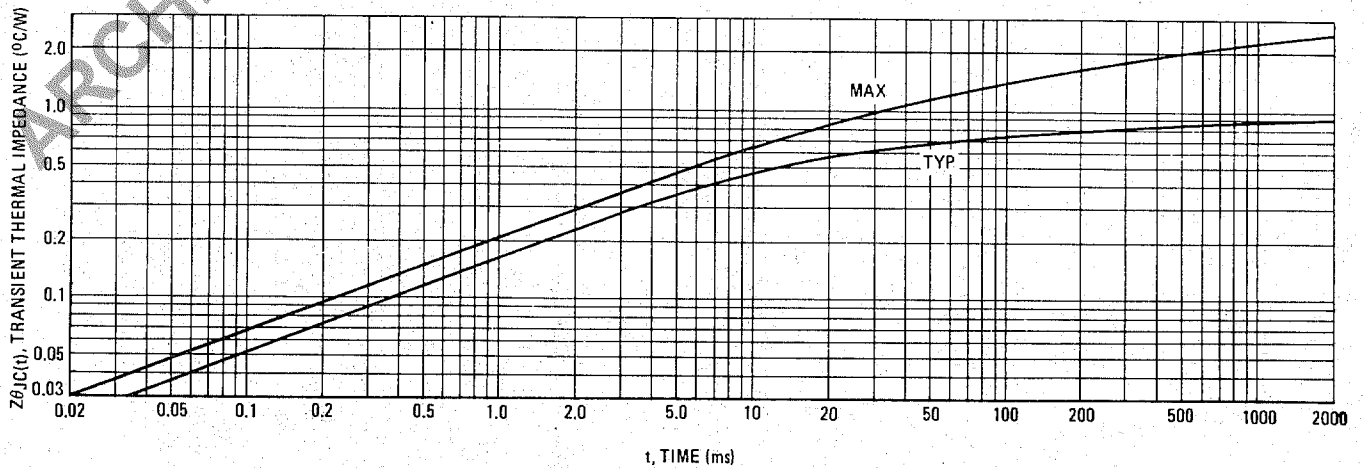


FIGURE 8 - FORWARD VOLTAGE

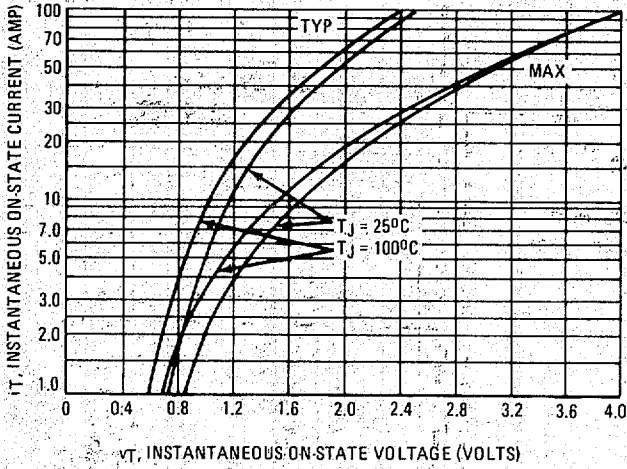


FIGURE 9 - HOLDING CURRENT

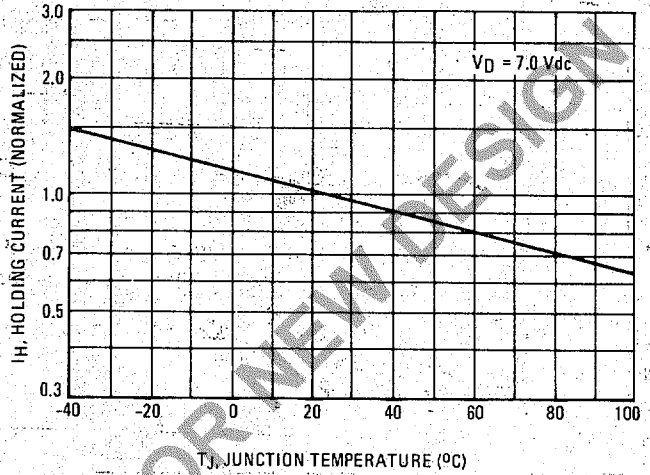


FIGURE 10 - TYPICAL THERMAL RESISTANCE OF PLATES

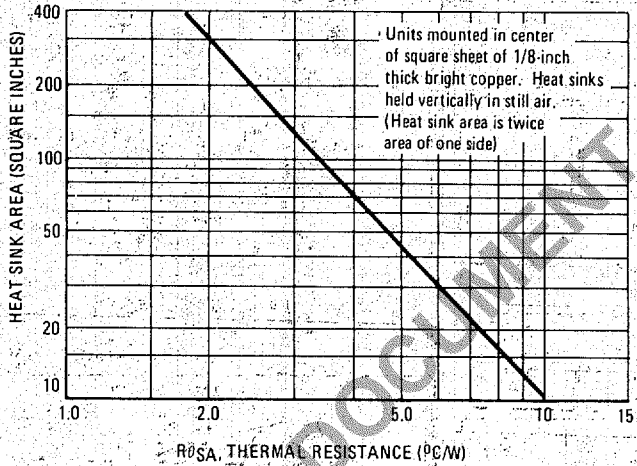


FIGURE 11 - CASE-TO-AMBIENT THERMAL RESISTANCE

