IRFP140R, IRFP141R, IRFP142R, IRFP143R

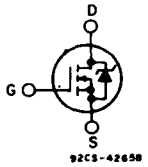
File Number **2086**

Avalanche Energy Rated N-Channel Power MOSFETs

27A and 24A, 60V-100V
$r_{DS}(on) = 0.085\Omega$ and 0.11Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

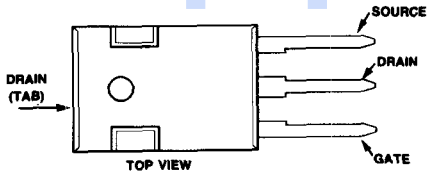


TERMINAL DIAGRAM

TERMINAL DESIGNATION

The IRFP140R, IRFP141R, IRFP142R and IRFP143R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.



JEDEC TO-247

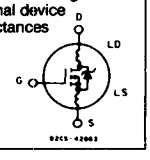
Absolute Maximum Ratings

Parameter		IRFP140R	IRFP141R	IRFP142R	IRFP143R	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20$ KΩ) ①	100	60	100	60	V
I_D @ $T_C = 25°C$	Continuous Drain Current	27	27	24	24	A
I_D @ $T_C = 100°C$	Continuous Drain Current	17	17	15	15	A
I_{DM}	Pulsed Drain Current ③	108	108	96	96	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	100				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFP140R IRFP142R	100	—	—	V	V_{GS} = 0V
		IRFP141R IRFP143R	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFP140R IRFP141R	27	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max}$, V_{GS} = 10V
		IRFP142R IRFP143R	24	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFP140R IRFP141R	—	0.07	0.085	Ω	V_{GS} = 10V, I_D = 15A
		IRFP142R IRFP143R	—	0.09	0.11	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	10	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, I_D = 15A
C_{iss}	Input Capacitance	ALL	—	1275	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	550	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	160	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	16	30	ns	$V_{DD} \simeq$ 30V, I_D = 15A, Z_o = 4.7Ω
t_r	Rise Time	ALL	—	27	60	ns	See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	38	80	ns	
t_f	Fall Time	ALL	—	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	38	60	nC	V_{GS} = 10V, I_D = 34A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	17	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	21	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFP140R IRFP141R	—	—	27	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFP142R IRFP143R	—	—	24	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFP140R IRFP141R	—	—	108	A	
		IRFP142R IRFP143R	—	—	96	A	
V_{SD}	Diode Forward Voltage ②	IRFP140R IRFP141R	—	—	2.5	V	T_C = 25°C, I_S = 27A, V_{GS} = 0V
		IRFP142R IRFP143R	—	—	2.3	V	T_C = 25°C, I_S = 24A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	500	—	ns	T_J = 150°C, I_F = 27A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.9	—	μC	T_J = 150°C, I_F = 27A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 10V, starting T_J = 25°C, L = 250μH, R_{gs} = 50Ω, I_{peak} = 27A. See figures 15, 16.

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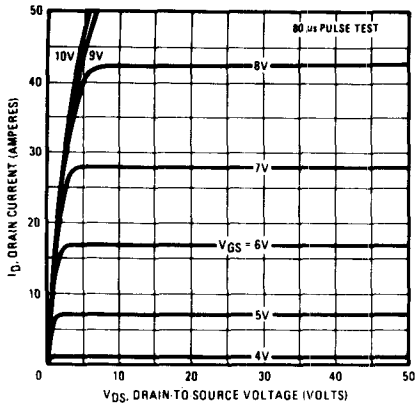

Fig. 1 - Typical output characteristics.

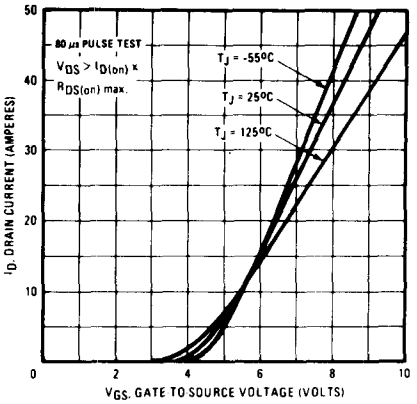

Fig. 2 - Typical transfer characteristics.

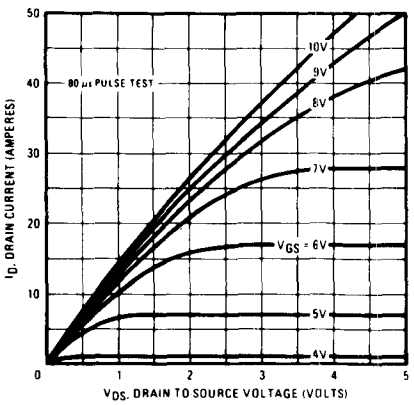

Fig. 3 - Typical saturation characteristics.

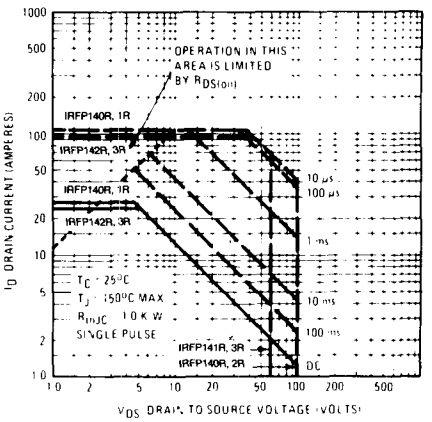

Fig. 4 - Maximum safe operating area.

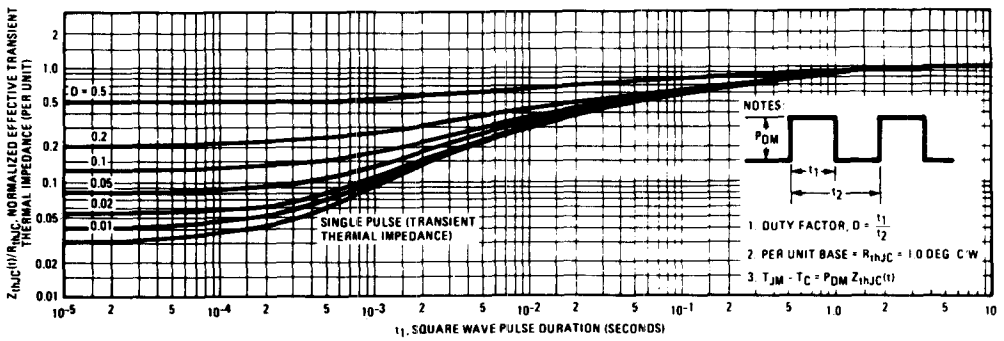

Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

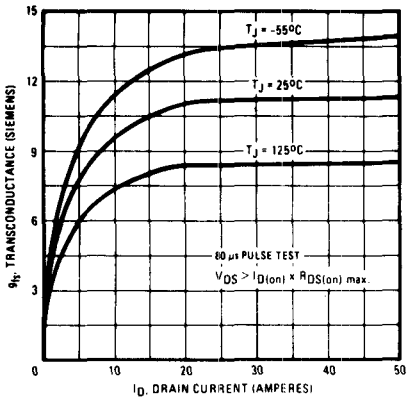

Fig. 6 - Typical transconductance vs. drain current.

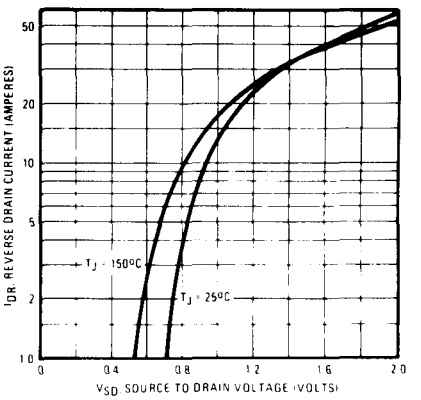

Fig. 7 - Typical source-drain diode forward voltage.

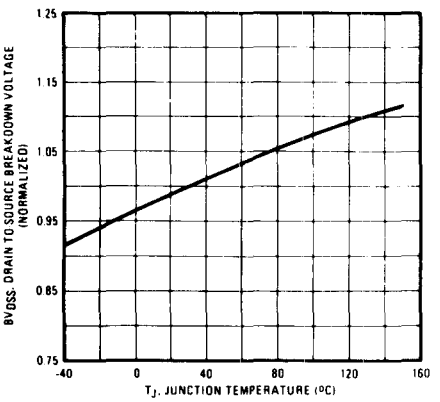

Fig. 8 - Breakdown voltage vs. temperature.

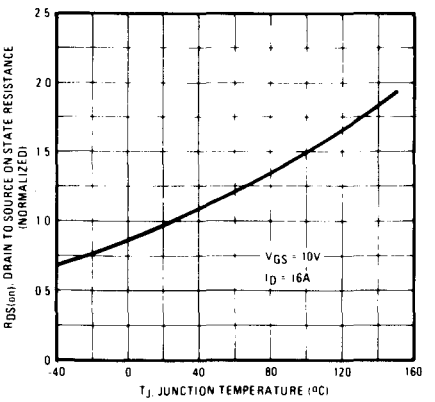

Fig. 9 - Normalized on-resistance vs. temperature.

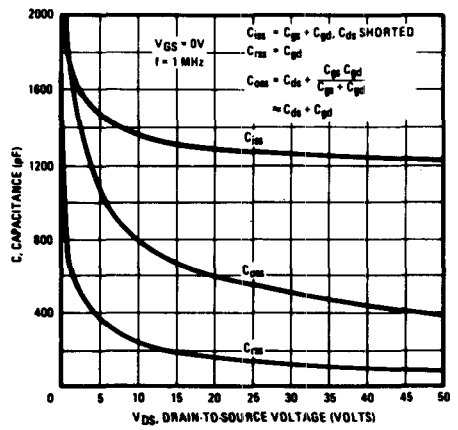

Fig. 10 - Typical capacitance vs. drain-to-source voltage.

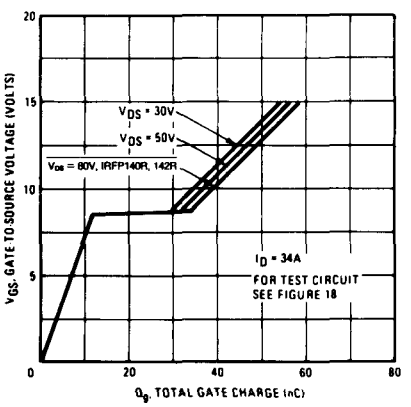

Fig. 11 - Typical gate charge vs. gate-to-source voltage.

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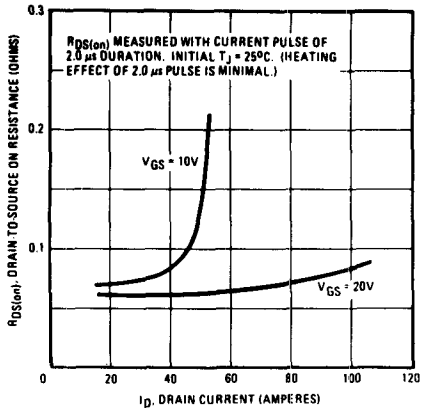

Fig. 12 - Typical on-resistance vs. drain current.

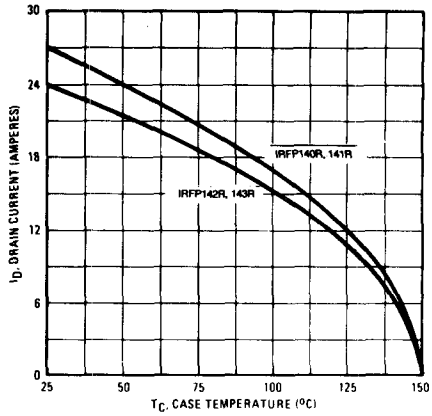

Fig. 13 - Maximum drain current vs. case temperature.

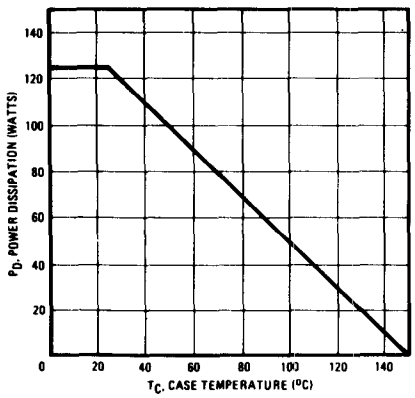

Fig. 14 - Power vs. temperature derating curve.

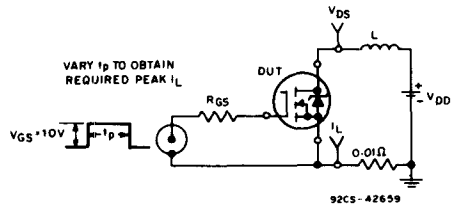

Fig. 15 - Unclamped energy test circuit.

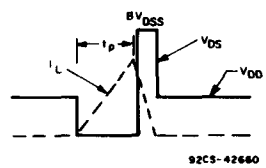

Fig. 16 - Unclamped energy waveforms.

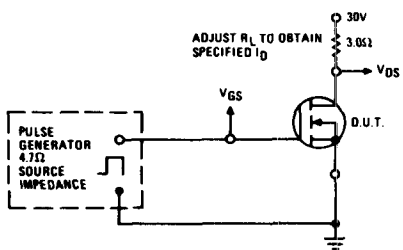

Fig. 17 - Switching time test circuit.

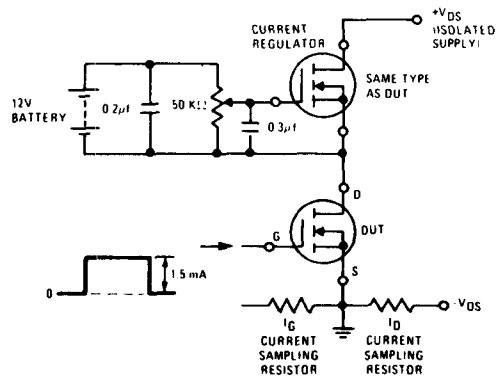

Fig. 18 - Gate charge test circuit.