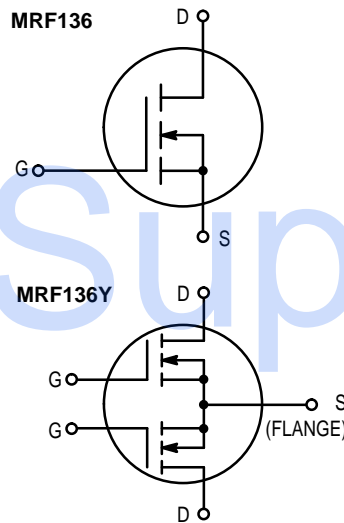


The RF MOSFET Line
RF Power
Field-Effect Transistors
N-Channel Enhancement-Mode MOSFETs

... designed for wideband large-signal amplifier and oscillator applications up to 400 MHz range, in either single ended or push-pull configuration.

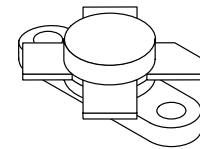
- Guaranteed 28 Volt, 150 MHz Performance

MRF136	MRF136Y
Output Power = 15 Watts	Output Power = 30 Watts
Narrowband Gain = 16 dB (Typ)	Broadband Gain = 14 dB (Typ)
Efficiency = 60% (Typical)	Efficiency = 54% (Typical)
- Small-Signal and Large-Signal Characterization
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Space Saving Package For Push-Pull Circuit Applications — MRF136Y
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques

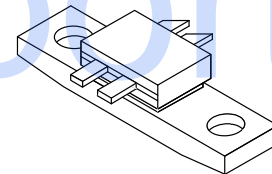


MRF136
MRF136Y

15 W, 30 W, to 400 MHz
N-CHANNEL
MOS BROADBAND
RF POWER FETs



CASE 211-07, STYLE 2
MRF136



CASE 319B-02, STYLE 1
MRF136Y

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		MRF136	MRF136Y	
Drain-Source Voltage	V_{DSS}	65	65	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	65	65	Vdc
Gate-Source Voltage	V_{GS}	±40		Vdc
Drain Current — Continuous	I_D	2.5	5.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	55 0.314	100 0.571	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150		°C
Operating Junction Temperature	T_J	200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
		MRF136	MRF136Y	
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.2	1.75	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS (1)

Drain–Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 5.0$ mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero–Gate Voltage Drain Current ($V_{DS} = 28$ V, $V_{GS} = 0$)	I_{DSS}	—	—	2.0	mAdc
Gate–Source Leakage Current ($V_{GS} = 40$ V, $V_{DS} = 0$)	I_{GSS}	—	—	1.0	μAdc

ON CHARACTERISTICS (1)

Gate Threshold Voltage ($V_{DS} = 10$ V, $I_D = 25$ mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance ($V_{DS} = 10$ V, $I_D = 250$ mA)	g_{fs}	250	400	—	mmhos

DYNAMIC CHARACTERISTICS (1)

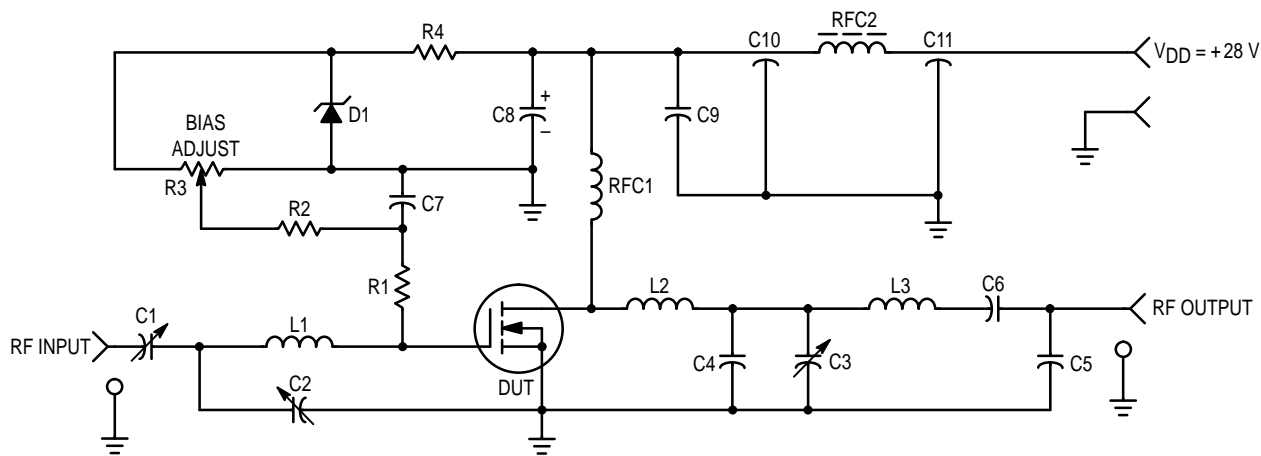
Input Capacitance ($V_{DS} = 28$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{iss}	—	24	—	pF
Output Capacitance ($V_{DS} = 28$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{oss}	—	27	—	pF
Reverse Transfer Capacitance ($V_{DS} = 28$ V, $V_{GS} = 0$, $f = 1.0$ MHz)	C_{rss}	—	5.5	—	pF

FUNCTIONAL CHARACTERISTICS (2)

Noise Figure ($V_{DS} = 28$ Vdc, $I_D = 500$ mA, $f = 150$ MHz)	MRF136	NF	—	1.0	—	dB
Common Source Power Gain (Figure 1) ($V_{DD} = 28$ Vdc, $P_{out} = 15$ W, $f = 150$ MHz, $I_{DQ} = 25$ mA)	MRF136	G_{ps}	13	16	—	dB
Common Source Power Gain (Figure 2) ($V_{DD} = 28$ Vdc, $P_{out} = 30$ W, $f = 150$ MHz, $I_{DQ} = 100$ mA)	MRF136Y	G_{ps}	12	14	—	dB
Drain Efficiency (Figure 1) ($V_{DD} = 28$ Vdc, $P_{out} = 15$ W, $f = 150$ MHz, $I_{DQ} = 25$ mA)	MRF136	η	50	60	—	%
Drain Efficiency (Figure 2) ($V_{DD} = 28$ Vdc, $P_{out} = 30$ W, $f = 150$ MHz, $I_{DQ} = 100$ mA)	MRF136Y	η	50	54	—	%
Electrical Ruggedness (Figure 1) ($V_{DD} = 28$ Vdc, $P_{out} = 15$ W, $f = 150$ MHz, $I_{DQ} = 25$ mA, VSWR 30:1 at all Phase Angles)	MRF136	ψ	No Degradation in Output Power			
Electrical Ruggedness (Figure 2) ($V_{DD} = 28$ Vdc, $P_{out} = 30$ W, $f = 150$ MHz, $I_{DQ} = 100$ mA, VSWR 30:1 at all Phase Angles)	MRF136Y	ψ	No Degradation in Output Power			

NOTES:

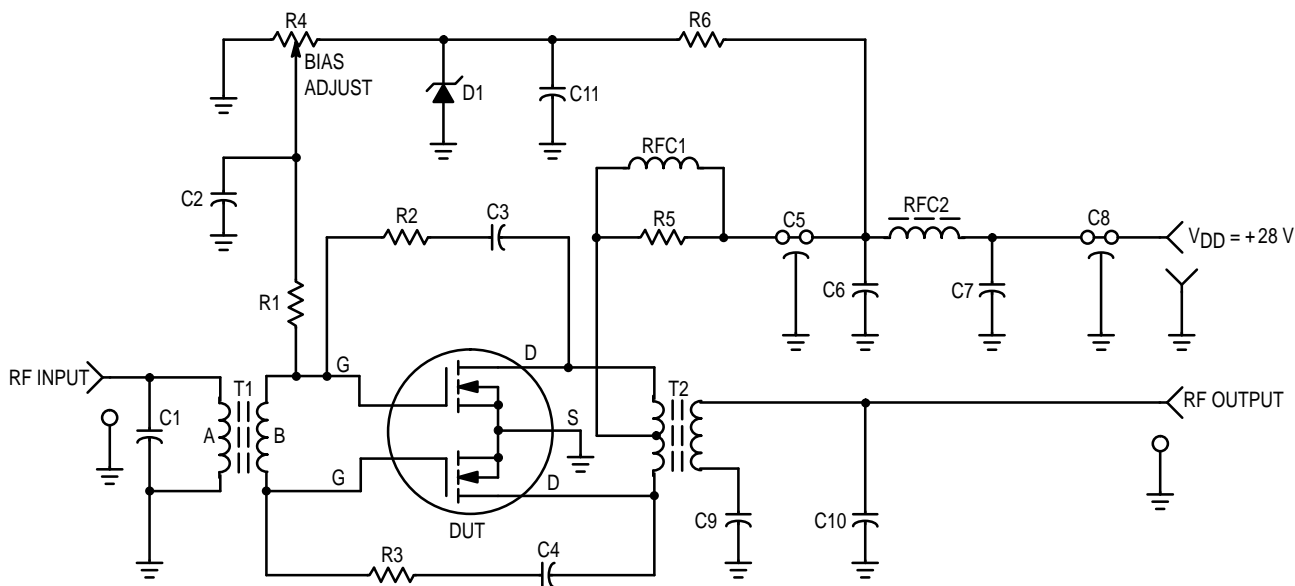
1. For MRF136Y, each side measured separately.
2. For MRF136Y measured in push–pull configuration.



- C1, C2 — Arco 406, 15–115 pF or Equivalent
- C3 — Arco 404, 8–60 pF or Equivalent
- C4 — 43 pF Mini-Unelco or Equivalent
- C5 — 24 pF Mini-Unelco or Equivalent
- C6 — 680 pF, 100 Mils Chip
- C7 — 0.01 μ F Ceramic
- C8 — 100 μ F, 40 V
- C9 — 0.1 μ F Ceramic
- C10, C11 — 680 pF Feedthru
- D1 — 1N5925A Motorola Zener

- L1 — 2 Turns, 0.29" ID, #18 AWG, 0.10" Long
- L2 — 2 Turns, 0.23" ID, #18 AWG, 0.10" Long
- L3 — 2-1/4 Turns, 0.29" ID, #18 AWG, 0.125" Long
- RFC1 — 20 Turns, 0.30" ID, #20 AWG Enamel Closewound
- RFC2 — Ferroxcube VK-200 — 19/4B
- R1 — 27 Ω , 1 W Thin Film
- R2 — 10 k Ω , 1/4 W
- R3 — 10 Turns, 10 k Ω
- R4 — 1.8 k Ω , 1/2 W
- Board Material — 0.062" G10, 1 oz. Cu Clad, Double Sided

Figure 1. 150 MHz Test Circuit (MRF136)



- C1 — 5.0 pF
- C2, C3, C4, C6, C7, C9, C11 — 0.1 μ F Ceramic
- C5, C8 — 680 pF Feedthru
- C10 — 15 pF
- D1 — 1N4740 Motorola Zener
- RFC1 — 17 Turns, #24 AWG Wound on R5
- RFC2 — Ferroxcube VK-200-19/4B or Equivalent
- R1 — 10 k Ω , 1/4 W
- R2, R3 — 560 Ω , 1/2 W
- R4 — 10 Turns, 10 k Ω

- R5 — 56 k Ω , 1 W
- R6 — 1.6 k Ω , 1/4 W
- T1 — Primary Winding — 3 Turns #28 Enameled Wire.
— Secondary Winding — 2 Turns #28 Enameled Wire.
Both windings wound through a Fair/Rite Balun 65 core.
Part #2865002402.
- T2 — 1:1 Transformer Wound Bifilar — 2 Turns Twisted Pair
#24 Enameled Wire through a Indiana General Balun Q1
core. Part #18006-1-Q1. Primary winding center tapped.
- Board Material — 0.062" G10, 1 oz. Cu Clad, Double Sided

Figure 2. 30–150 MHz Test Circuit (MRF136Y)

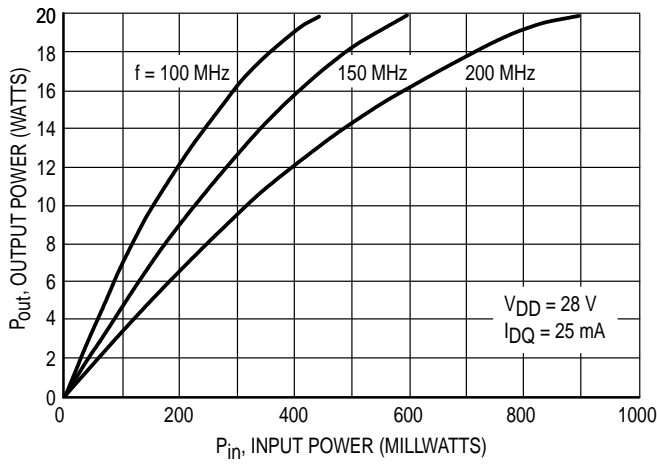


Figure 3. Output Power versus Input Power

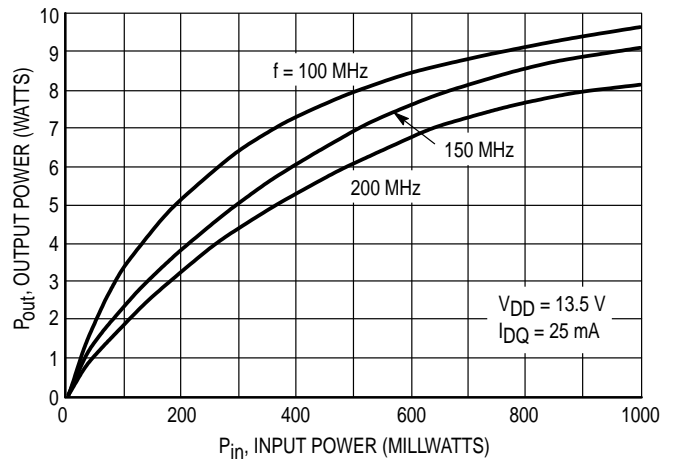


Figure 4. Output Power versus Input Power

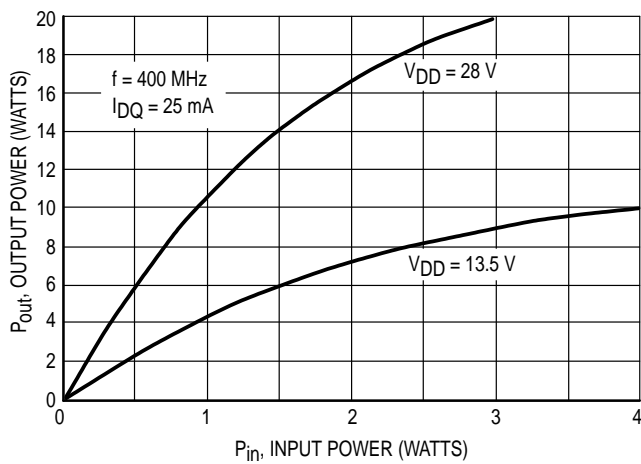


Figure 5. Output Power versus Input Power

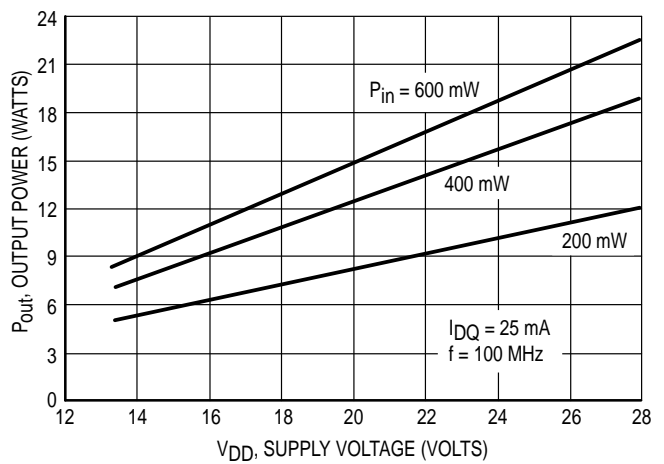


Figure 6. Output Power versus Supply Voltage

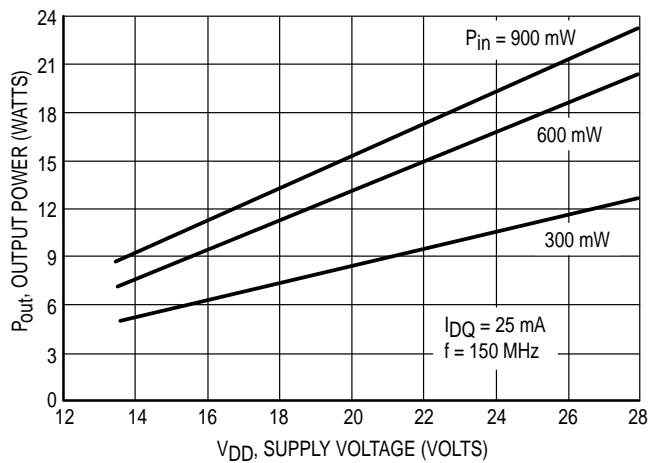


Figure 7. Output Power versus Supply Voltage

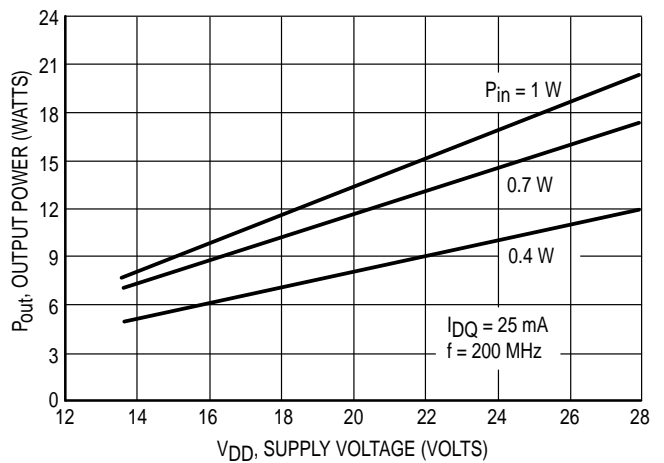
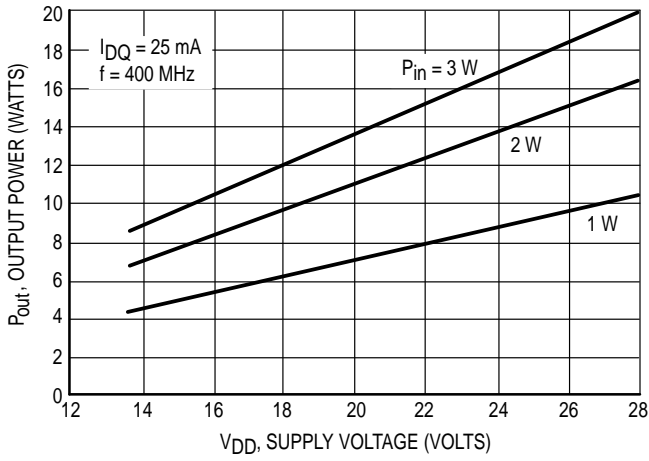
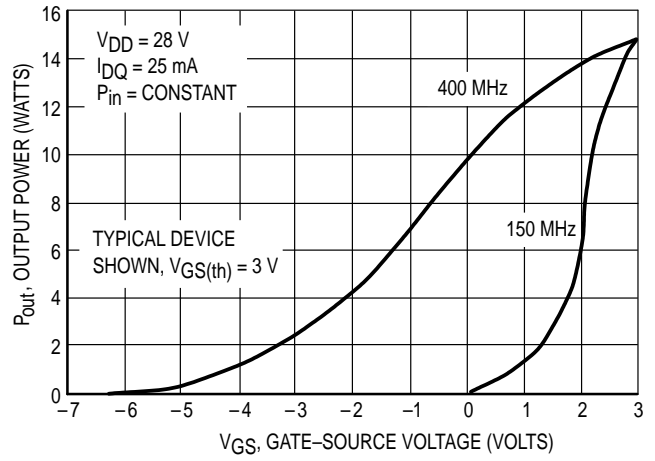


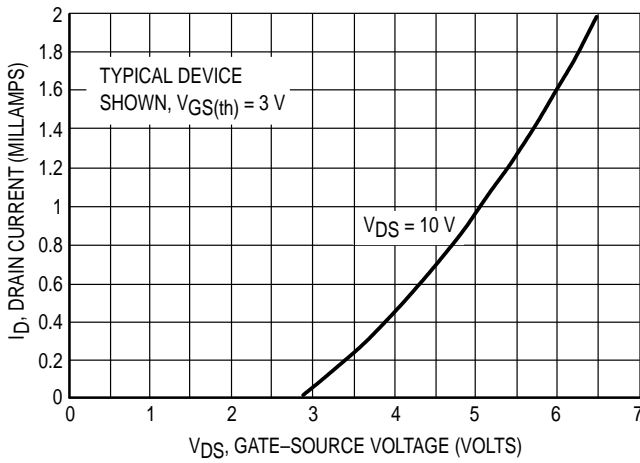
Figure 8. Output Power versus Supply Voltage



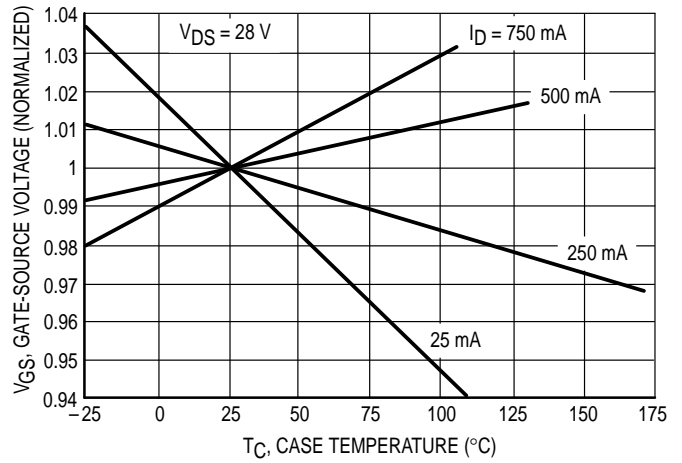
**Figure 9. Output Power versus Supply Voltage
MRF136**



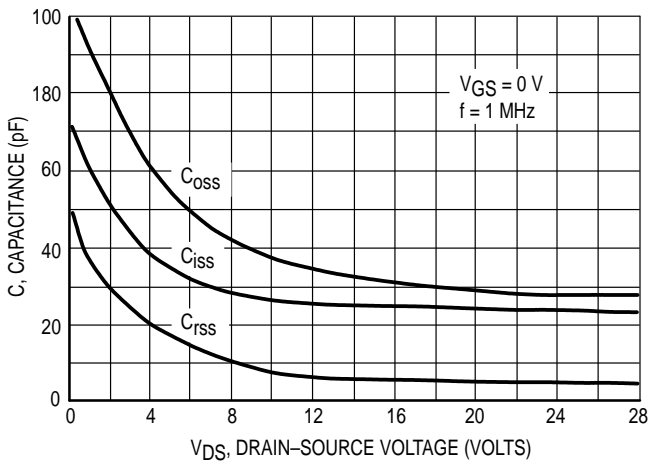
**Figure 10. Output Power versus Gate Voltage
MRF136**



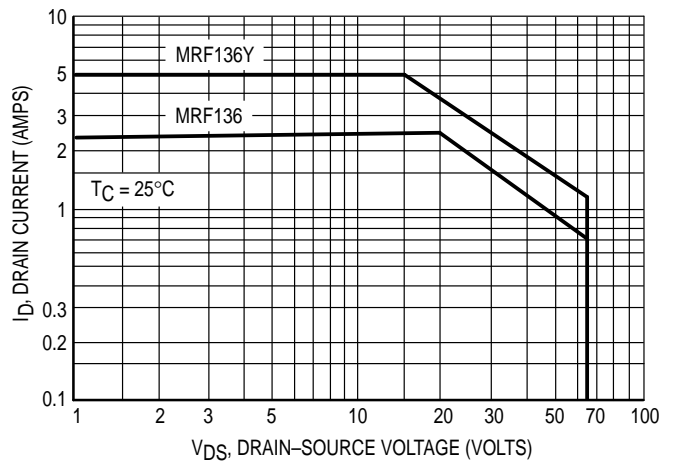
**Figure 11. Drain Current versus Gate Voltage
(Transfer Characteristics)*
MRF136/MRF136Y**



**Figure 12. Gate-Source Voltage versus
Case Temperature*
MRF136/MRF136Y**



**Figure 13. Capacitance versus Drain-Source Voltage*
MRF136/MRF136Y**



**Figure 14. DC Safe Operating Area
MRF136/MRF136Y**

*Data shown applies to MRF136 and each half of MRF136Y.

MRF136Y
TYPICAL PERFORMANCE IN BROADBAND TEST CIRCUIT
 (Refer to Figure 2)

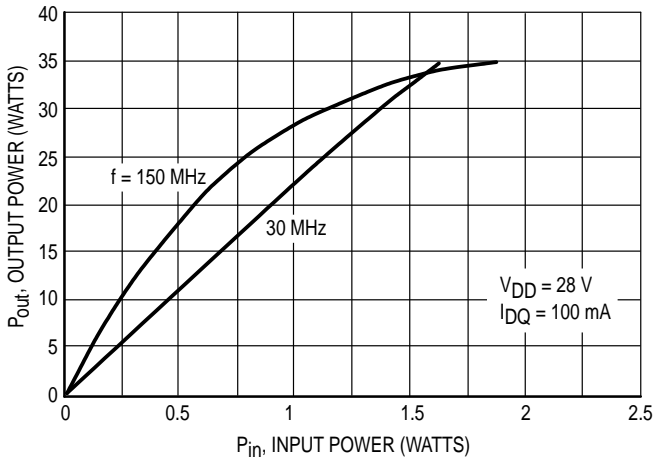


Figure 15. Output Power versus Input Power

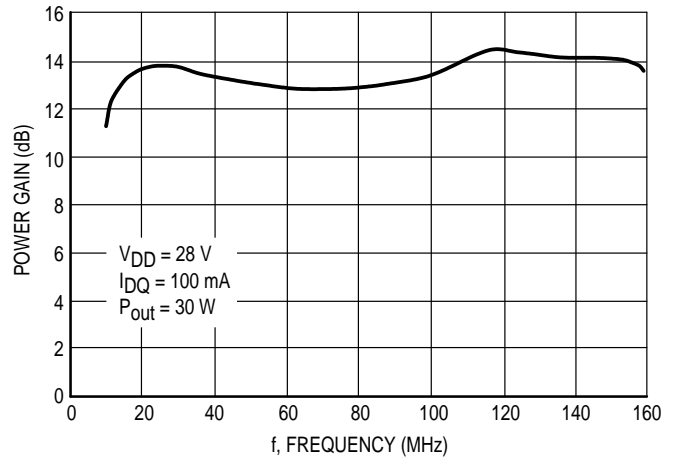


Figure 16. Power Gain versus Frequency

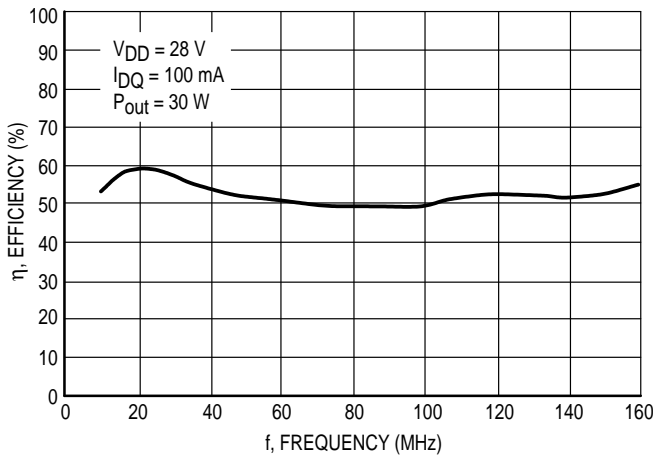


Figure 17. Drain Efficiency versus Frequency

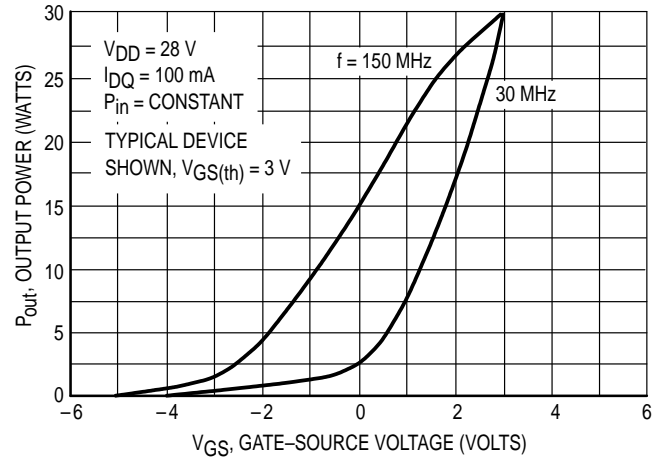


Figure 18. Output Power versus Gate Voltage

TYPICAL 400 MHz PERFORMANCE

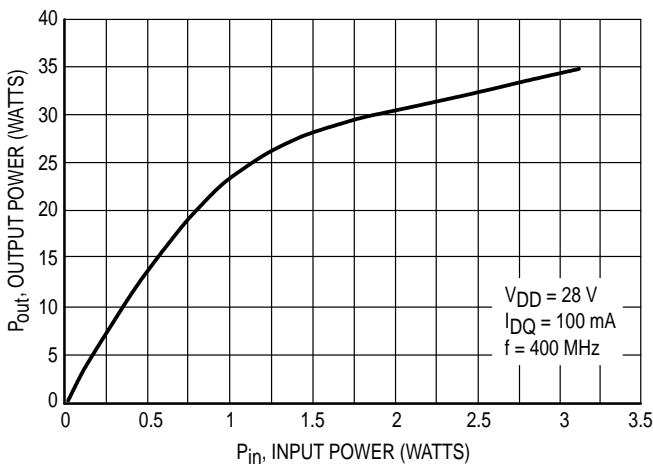


Figure 19. Output Power versus Input Power

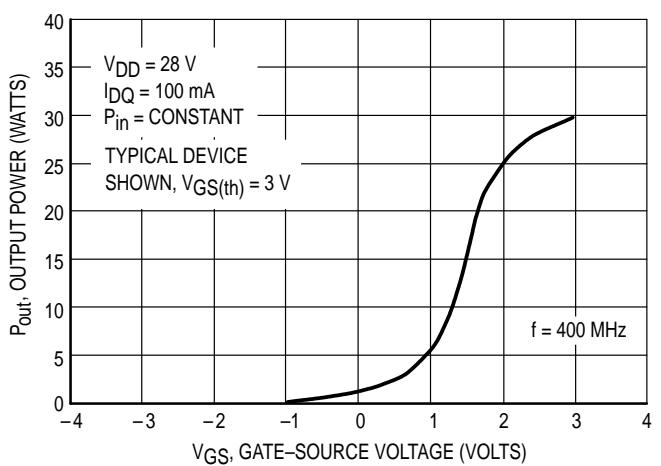


Figure 20. Output Power versus Gate Voltage

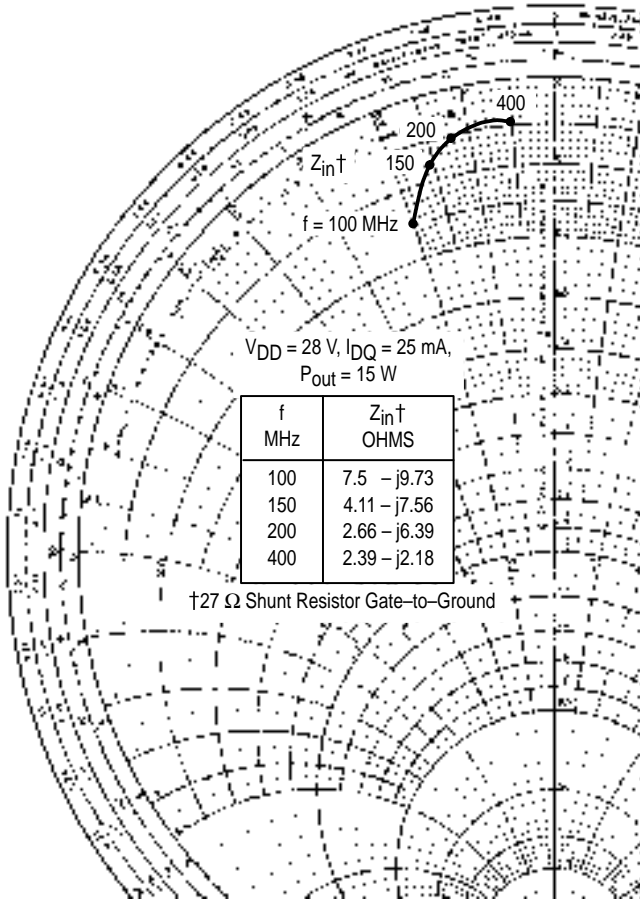


Figure 21. Large-Signal Series Equivalent Input Impedance, Z_{in}^\dagger
MRF136

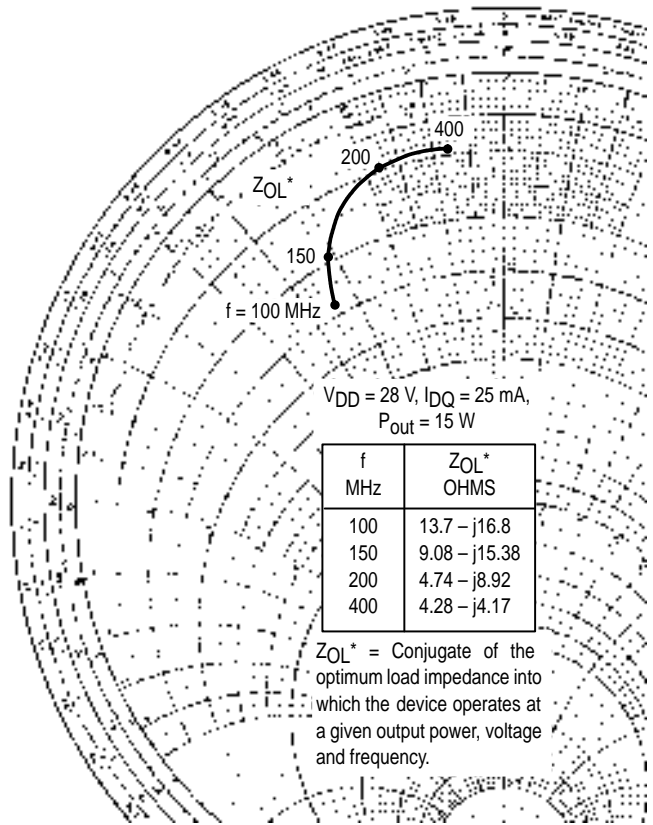


Figure 22. Large-Signal Series Equivalent Output Impedance, Z_{OL}^*
MRF136

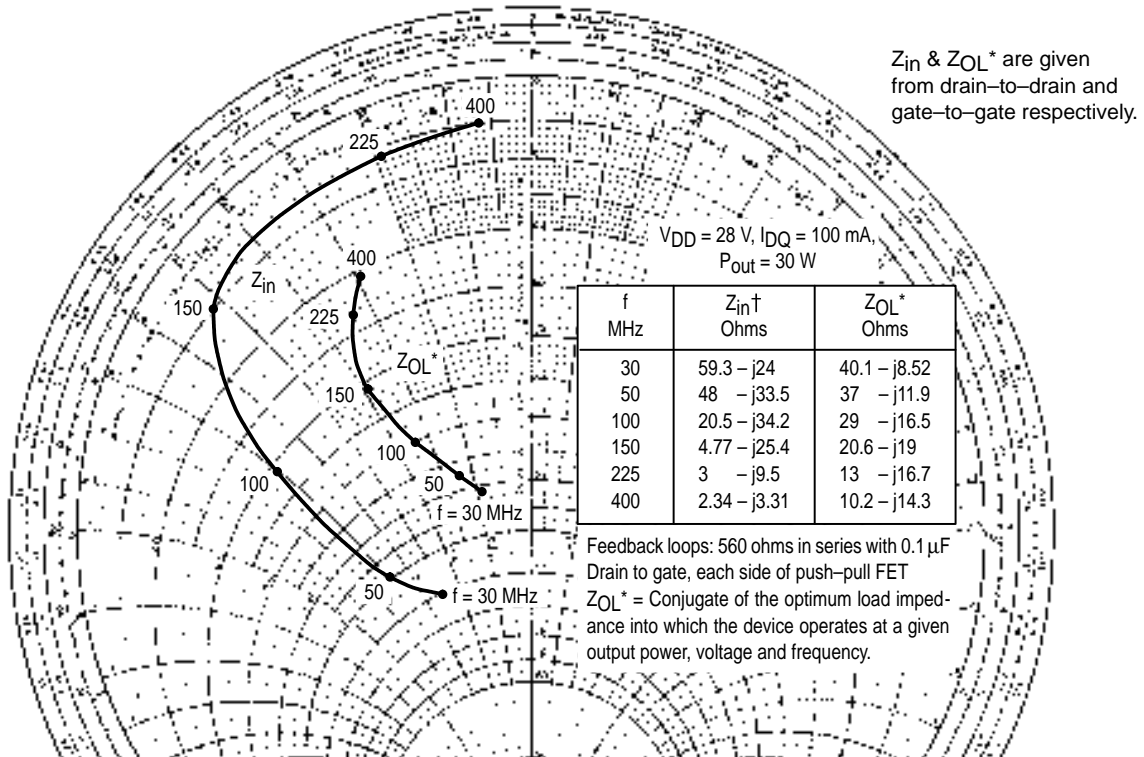


Figure 23. Input and Output Impedance
MRF136Y

MRF136

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	φ	S ₂₁	φ	S ₁₂	φ	S ₂₂	φ
2.0	0.988	-11	41.19	173	0.006	67	0.729	-12
5.0	0.970	-27	40.07	164	0.014	62	0.720	-31
10	0.923	-52	35.94	149	0.026	54	0.714	-58
20	0.837	-88	27.23	129	0.040	36	0.690	-96
30	0.784	-111	20.75	117	0.046	27	0.684	-118
40	0.751	-125	16.49	108	0.048	22	0.680	-131
50	0.733	-135	13.41	103	0.050	19	0.679	-139
60	0.720	-142	11.43	99	0.050	16	0.678	-145
70	0.709	-147	9.871	96	0.050	14	0.679	-149
80	0.707	-152	8.663	93	0.051	13	0.683	-153
90	0.706	-155	7.784	91	0.051	13	0.682	-155
100	0.708	-157	7.008	88	0.051	13	0.680	-157
110	0.711	-159	6.435	86	0.051	14	0.681	-158
120	0.714	-161	5.899	85	0.051	15	0.682	-159
130	0.717	-163	5.439	82	0.052	16	0.684	-160
140	0.720	-164	5.068	80	0.052	17	0.684	-161
150	0.723	-165	4.709	80	0.052	18	0.686	-161
160	0.727	-166	4.455	78	0.052	18	0.690	-161
170	0.732	-167	4.200	77	0.052	18	0.694	-162
180	0.735	-168	3.967	75	0.052	19	0.699	-162
190	0.738	-169	3.756	74	0.052	19	0.703	-163
200	0.740	-170	3.545	73	0.052	20	0.706	-163
225	0.746	-171	3.140	69	0.053	22	0.717	-163
250	0.742	-172	2.783	67	0.053	25	0.724	-163
275	0.744	-173	2.540	64	0.054	27	0.724	-163
300	0.751	-174	2.323	60	0.055	29	0.736	-163
325	0.757	-175	2.140	58	0.058	32	0.749	-163
350	0.760	-176	1.963	54	0.059	35	0.758	-163
375	0.762	-177	1.838	52	0.062	38	0.768	-163
400	0.774	-179	1.696	50	0.065	41	0.783	-163
425	0.775	-179	1.590	48	0.068	43	0.793	-163
450	0.781	+179	1.493	46	0.071	46	0.805	-163
475	0.787	+177	1.415	43	0.074	47	0.813	-164
500	0.792	+176	1.332	40	0.079	48	0.825	-164
525	0.797	+175	1.259	38	0.083	50	0.831	-164
550	0.801	+175	1.185	37	0.088	51	0.843	-164
575	0.810	+174	1.145	36	0.094	52	0.855	-164
600	0.816	+173	1.091	34	0.101	52	0.869	-165
625	0.818	+171	1.041	32	0.106	53	0.871	-165
650	0.825	+170	0.994	30	0.112	53	0.884	-165
675	0.834	+169	0.962	29	0.119	53	0.890	-165
700	0.837	+168	0.922	27	0.127	53	0.906	-166
725	0.836	+167	0.879	25	0.133	52	0.909	-167
750	0.841	+166	0.838	25	0.140	53	0.917	-167
775	0.844	+165	0.824	24	0.148	52	0.933	-167
800	0.846	+163	0.785	21	0.154	50	0.941	-168

Table 1. Common Source Scattering Parameters
V_{DS} = 28 V, I_D = 0.5 A

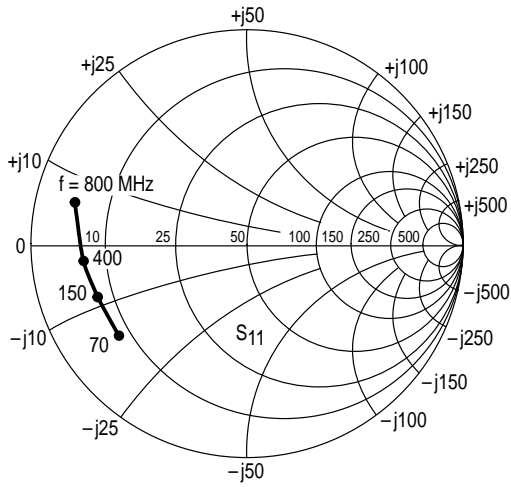


Figure 24. S_{11} , Input Reflection Coefficient versus Frequency
 $V_{DS} = 28\text{ V}$ $I_D = 0.5\text{ A}$

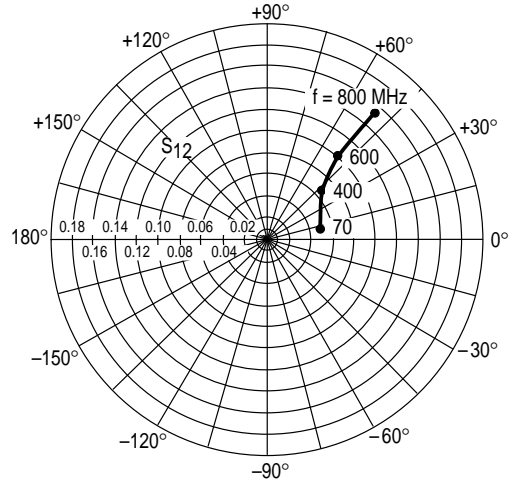


Figure 25. S_{12} , Reverse Transmission Coefficient versus Frequency
 $V_{DS} = 28\text{ V}$ $I_D = 0.5\text{ A}$

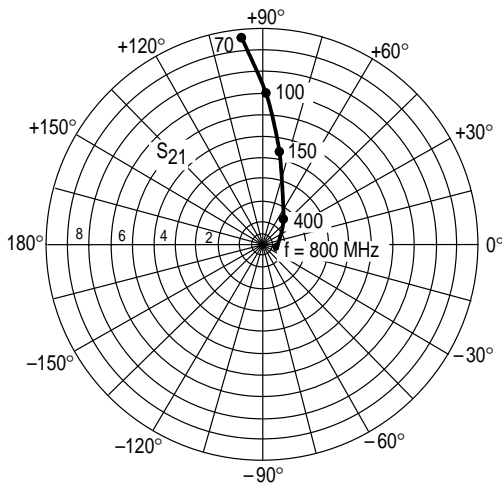


Figure 26. S_{21} , Forward Transmission Coefficient versus Frequency
 $V_{DS} = 28\text{ V}$ $I_D = 0.5\text{ A}$

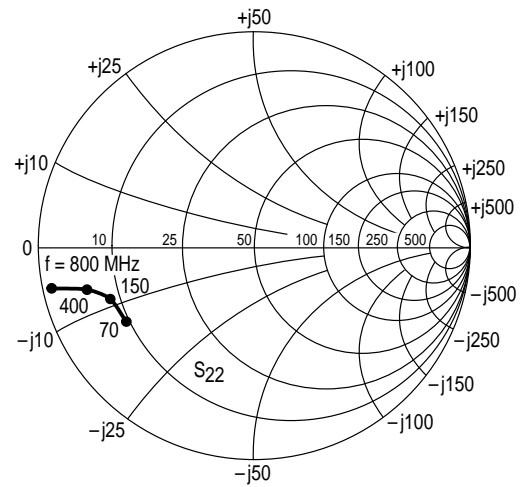


Figure 27. S_{22} , Output Reflection Coefficient versus Frequency
 $V_{DS} = 28\text{ V}$ $I_D = 0.5\text{ A}$

DESIGN CONSIDERATIONS

The MRF136 and MRF136Y are RF power N-Channel enhancement mode field-effect transistors (FETs) designed especially for HF and VHF power amplifier applications. Motorola RF MOS FETs feature planar design for optimum manufacturability.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF136 and MRF136Y are enhancement mode FETs and, therefore, do not conduct when drain voltage is applied without gate bias. A positive gate voltage causes drain current to flow (see Figure 11). RF power FETs require forward bias for optimum gain and power output. A Class AB condition with quiescent drain current (I_{DQ}) in the 25–100 mA range is sufficient for many applications. For special requirements such as linear amplification, I_{DQ} may have to be adjusted to optimize the critical parameters.

The MOS gate is a dc open circuit. Since the gate bias circuit does not have to deliver any current to the FET, a simple resistive divider arrangement may sometimes suffice for this function. Special applications may require more elaborate gate bias systems.

GAIN CONTROL

Power output of the MRF136 and MRF136Y may be controlled from rated values down to the milliwatt region (>20 dB reduction in power output with constant input power) by varying the dc gate voltage. This feature, not available in

bipolar RF power devices, facilitates the incorporation of manual gain control, AGC/ALC and modulation schemes into system designs. A full range of power output control may require dc gate voltage excursions into the negative region.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for MRF136 and MRF136Y. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. Both small signal scattering parameters (MRF136 only) and large signal impedance parameters are provided. Large signal impedances should be used for network designs wherever possible. While the s parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is particularly useful at frequencies outside those presented in the large signal impedance plots.

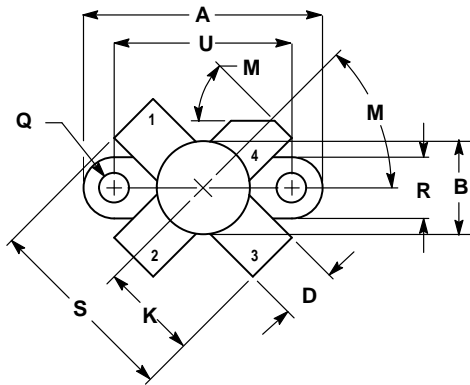
RF power FETs are triode devices and are therefore not unilateral. This, coupled with the very high gain, yields a device capable of self oscillation. Stability may be achieved using techniques such as drain loading, input shunt resistive loading, or feedback. S parameter stability analysis can provide useful information in the selection of loading and/or feedback to insure stable operation. The MRF136 was characterized with a 27 ohm input shunt loading resistor, while the MRF136Y was characterized with a resistive feedback loop around each of its two active devices.

For further discussion of RF amplifier stability and the use of two port parameters in RF amplifier design, see Motorola Application Note AN215A on page 6–204 in the RF Device Data (DL110 Rev 1).

LOW NOISE OPERATION

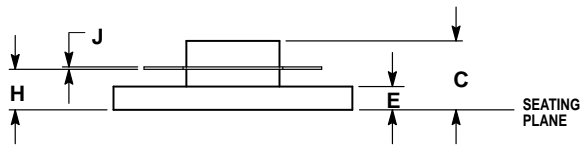
Input resistive loading will degrade noise performance, and noise figure may vary significantly with gate driving impedance. A low loss input matching network with its gate impedance optimized for lowest noise is recommended.

PACKAGE DIMENSIONS



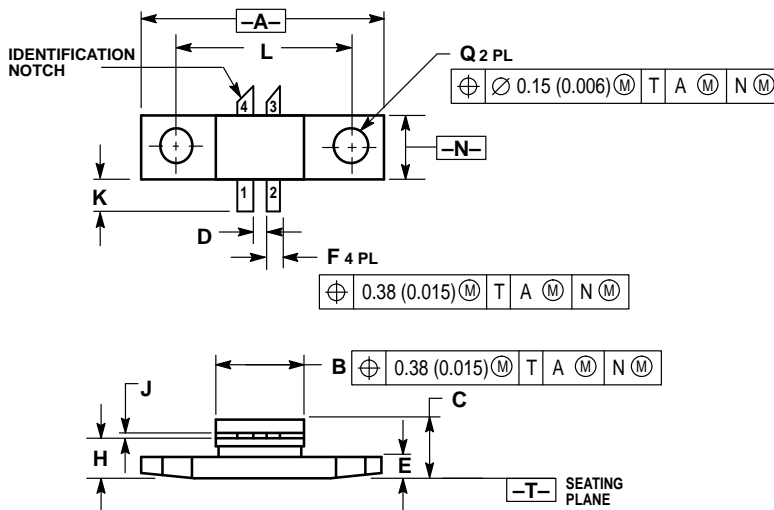
- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.960	0.990	24.39	25.14
B	0.370	0.390	9.40	9.90
C	0.229	0.281	5.82	7.13
D	0.215	0.235	5.47	5.96
E	0.085	0.105	2.16	2.66
H	0.150	0.108	3.81	4.57
J	0.004	0.006	0.11	0.15
K	0.395	0.405	10.04	10.28
M	40°	50°	40°	50°
Q	0.113	0.130	2.88	3.30
R	0.245	0.255	6.23	6.47
S	0.790	0.810	20.07	20.57
U	0.720	0.730	18.29	18.54



- STYLE 2:
 PIN 1. SOURCE
 2. GATE
 3. SOURCE
 4. DRAIN

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- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.965	0.985	24.51	25.02
B	0.355	0.375	9.02	9.52
C	0.230	0.260	5.84	6.60
D	0.055	0.065	1.40	1.65
E	0.102	0.114	2.59	2.90
F	0.055	0.065	1.40	1.65
H	0.160	0.170	4.06	4.31
J	0.004	0.006	0.10	0.15
K	0.120	0.140	3.05	3.55
L	0.725 BSC		18.42 BSC	
N	0.225	0.241	5.72	6.12
Q	0.125	0.135	3.18	3.42

- STYLE 1:
 PIN 1. GATE (INPUT)
 2. GATE (INPUT)
 3. DRAIN (OUTPUT)
 4. DRAIN (OUTPUT)
 SOURCE IS FLANGE

**CASE 319B-02
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