Features

- **High-speed - 150 ps Gate Delay - 2-input NAND, FO = 2 (nominal)**
- **Up to 2.7 Million Used Gates and 976 Pins**
- **System Level Integration Technology**
  - **Cores: ARM7TDMI™ and AVR® RISC Microcontrollers, OakDSP™ and LodeDSPCores™, 10T/100 Ethernet MAC, USB and PCI Cores**
  - **Memory: SRAM, ROM, CAM and FIFO; Gate Level or Embedded**
- **I/O Interfaces; CMOS, LVTTL, LVDS, PCI, USB - Output Currents up to 20 mA, 5V Tolerant I/O**
- **Deep Submicron CAD Flow**

Description

The ATL35 Series Gate Array and Embedded Array families are fabricated on a 0.35µ CMOS process with up to 4 levels of metal. This family features arrays with up to 2.7 million routable gates and 976 pins. The high density and high pin-count capabilities of the ATL35 family, coupled with the ability to embed microcontroller cores, DSP engines, and memory, all on the same silicon, make the ATL35 series of arrays an ideal choice for System Level Integration.

ATL35 Array Organization

Device Number	4LM Routable Gates(1)	3LM Routable Gates(1)	Available Routing Sites(2)	Max Pad Count	Max I/O Count	Gate Speed(3)
ATL35/44	4,195	3,729	6,216	44	36	150 ps
ATL35/68	13,230	11,760	19,600	68	60	150 ps
ATL35/84	22,200	19,734	32,890	84	76	150 ps
ATL35/100	33,480	29,760	49,600	100	92	150 ps
ATL35/120	47,839	42,211	75,042	120	112	150 ps
ATL35/132	59,185	52,222	92,840	132	124	150 ps
ATL35/144	71,737	63,298	112,530	144	136	150 ps
ATL35/160	90,514	79,866	141,984	160	152	150 ps
ATL35/184	121,877	107,538	191,180	184	176	150 ps
ATL35/208	150,085	131,324	250,142	208	200	150 ps
ATL35/228	182,880	160,020	304,800	228	220	150 ps
ATL35/256	233,774	204,552	389,624	256	240	150 ps
ATL35/304	334,044	292,288	556,740	304	288	150 ps
ATL35/352	425,958	369,164	757,260	352	336	150 ps
ATL35/388	520,695	451,269	925,680	388	372	150 ps
ATL35/432	652,421	565,431	1,159,860	432	416	150 ps
ATL35/484	768,033	658,314	1,462,920	484	468	150 ps
ATL35/540	964,078	826,353	1,836,340	540	516	150 ps
ATL35/600	1,196,371	1,025,460	2,278,802	600	576	150 ps
ATL35/700	1,642,242	1,407,636	3,128,080	700	676	150 ps
ATL35/800	1,999,526	1,691,906	4,101,592	800	776	150 ps
ATL35/900	2,542,995	2,151,765	5,216,400	900	876	150 ps
ATL35/976	2,767,931	2,306,609	6,150,958	976	952	150 ps

Notes: 1. One gate = NAN2
2. Routing site = 4 transistors
3. Nominal 2-input NAND gate FO = 2 at 3.3V

Gate Array/ Embedded Array

ATL35 Series

Rev. 0802E–10/99

Design

Design Systems Supported

Atmel supports several major software systems for design with complete cell libraries, as well as utilities for netlist verification, test vector verification and accurate delay simulations.

The following design systems are supported:

System	Version	Tools
Cadence®	4.4.3 2.1.p2 4.1-s051 2.5 3.4B 2.3	Opus™ - Schematic and Layout NC Verilog™ - Verilog Simulator Pearl™ - Static Path Verilog-XL™ - Verilog Simulator Logic Design Planner™ - Floorplanner BuildGates™ - Synthesis (Ambit)
Mentor/Model Tech™	5.2e B2 and Later	Modelsim Verilog and VHDL (VITAL) Simulator QuickVHDL™
Synopsys™	98.08, 98.05 5.0.1A	VSS™ - VHDL Simulator Design Compiler™ - Synthesis Test Compiler™ - Scan Insertion and ATPG Primetime™ - Static Path VCS™ - Verilog Simulator
Exemplar™	1998.2f	Leonardo Spectrum™ - Synthesis
Syntest	V2.2 V2.2 V1.6	TurboCheck - Gate TurboScan TurboFault

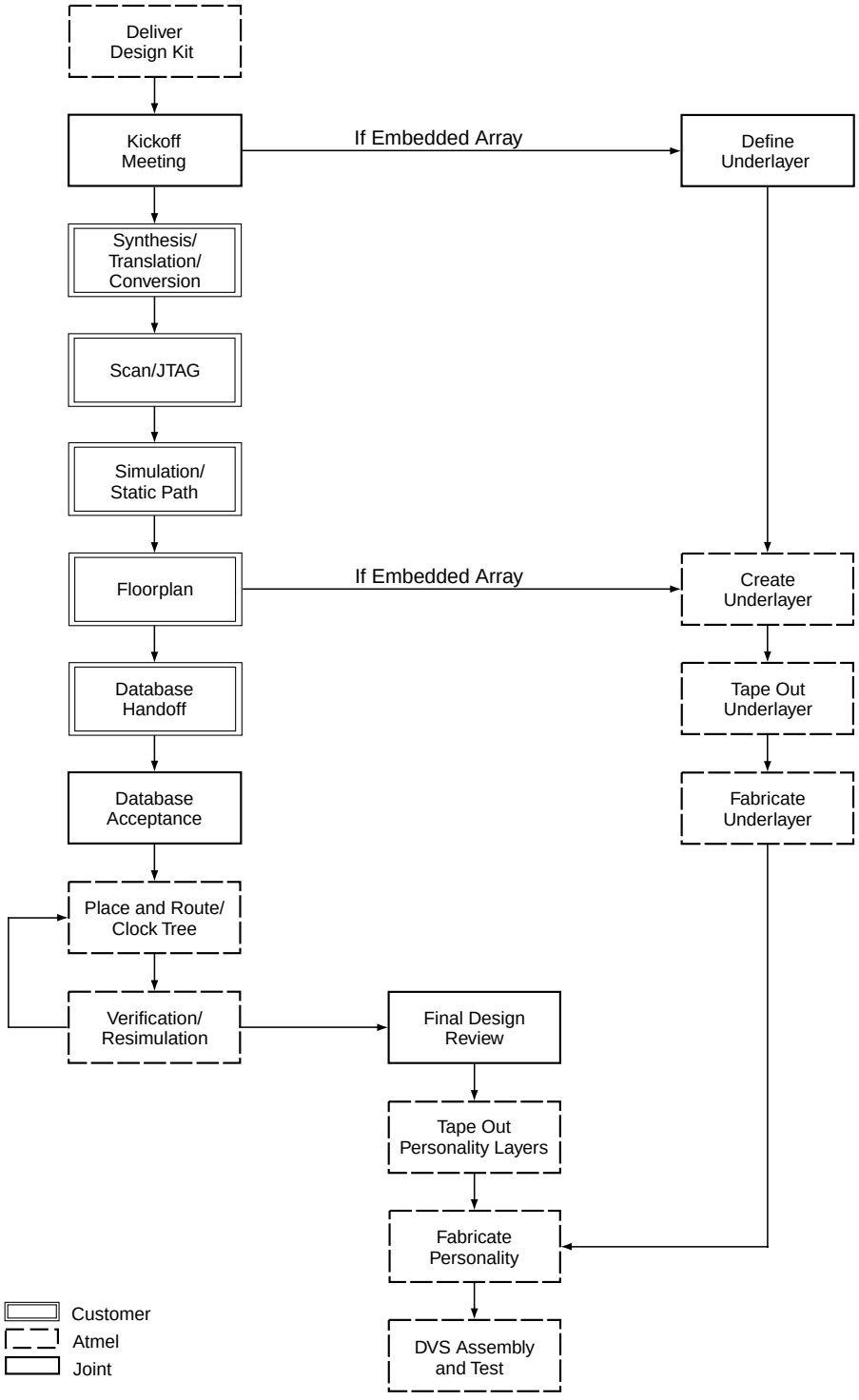
Design Flow and Tools

Atmel's Gate Array/Embedded Array design flow is structured to allow the designer to consolidate the greatest number of system components onto the same silicon chip, using widely available third party design tools. Atmel's cell library reflects silicon performance over extremes of temperature, voltage and process, and includes the effects of metal loading, inter-level capacitance and edge rise and fall times. The design flow includes clock tree synthesis to customer-specified skew and latency goals. RC extraction is performed on the final design database and incorporated into the timing analysis.

The Gate Array/Embedded Array Design Flow, shown on the following page, provides a pictorial description of the typical interaction between Atmel's design staff and the customer. Atmel will deliver design kits to support the customer's synthesis, verification, floorplanning and scan insertion activities. Tools such as Synopsys™, Cadence®, Verilog-HDL™, CTgen™, Exemplar™, PathMILL™ and TimeMILL™ are used, and many others are available. Should a design include embedded memory (SRAM or ROM) or an embedded core, Atmel will conduct a design review with the customer to understand the partition of the Gate Array/Embedded Array and to define the location of the memory blocks and/or cores so that an underlayer layout model can be created.

Following Database Acceptance, automated test pattern generation (ATPG) is performed, if required, on scan paths using Synopsys or Sunrise™ tools, the design is routed, and post-route RC data is extracted. After post-route verification and a Final Design Review, the design is taped out for fabrication.

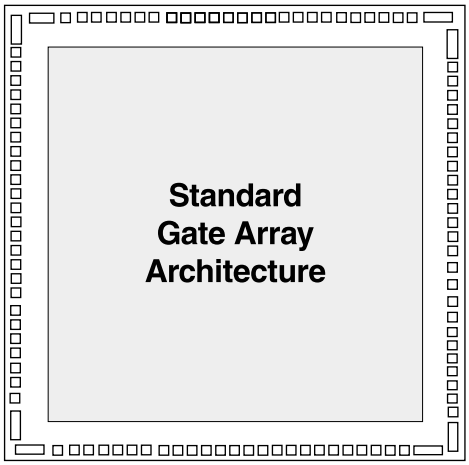
Gate Array/Embedded Array Design Flow



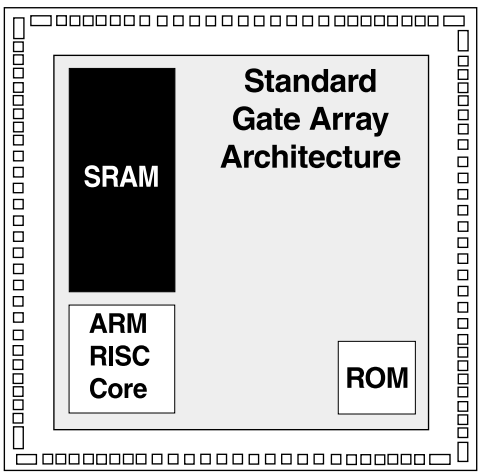
Pin Definition Requirements

The corner pads are reserved for Power and Ground only. All other pads are fully programmable as Input, Output, Bidirectional, Power or Ground. When implementing a design with 5V compliant buffers, one buffer site must be reserved for the VDD5 pin, which is used to distribute 5V power to the compliant buffers.

Gate Array



Embedded Array



Design Options

Logic Synthesis

Atmel can accept netlists in VHDL (MIL-STD-454, IEEE STD 1076) or Verilog-HDL format. Atmel fully supports Synopsys for VHDL™ simulation as well as synthesis. VHDL or Verilog-HDL is Atmel's preferred database format for Gate Array/Embedded Array design.

ASIC Design Translation

Atmel has successfully translated existing designs from most major ASIC vendors (LSI Logic®, Motorola®, SMOS™, Oki®, NEC®, Fujitsu®, AMI® and others) into Atmel ASICs. These designs have been optimized for speed and gate count and modified to add logic or memory, or replicated as a pin-for-pin compatible, drop-in replacement.

FPGA and PLD Conversions

Atmel has successfully translated existing FPGA/PLD designs from most major vendors (Xilinx®, Actel®, Altera®, AMD® and Atmel) into Atmel ASICs. There are four primary reasons to convert from an FPGA/PLD to an ASIC. Conversion of high volume devices for a single or combined design is cost effective. Performance can often be optimized for speed or low power consumption. Several FPGA/PLDs can be combined onto a single chip to minimize cost while reducing on-board space requirements. Finally, in situations where an FPGA/PLD was used for fast cycle time prototyping, an ASIC may provide a lower cost answer for long-term volume production.

Macro Cores

AVR (8-bit RISC) Microcontroller (8515)

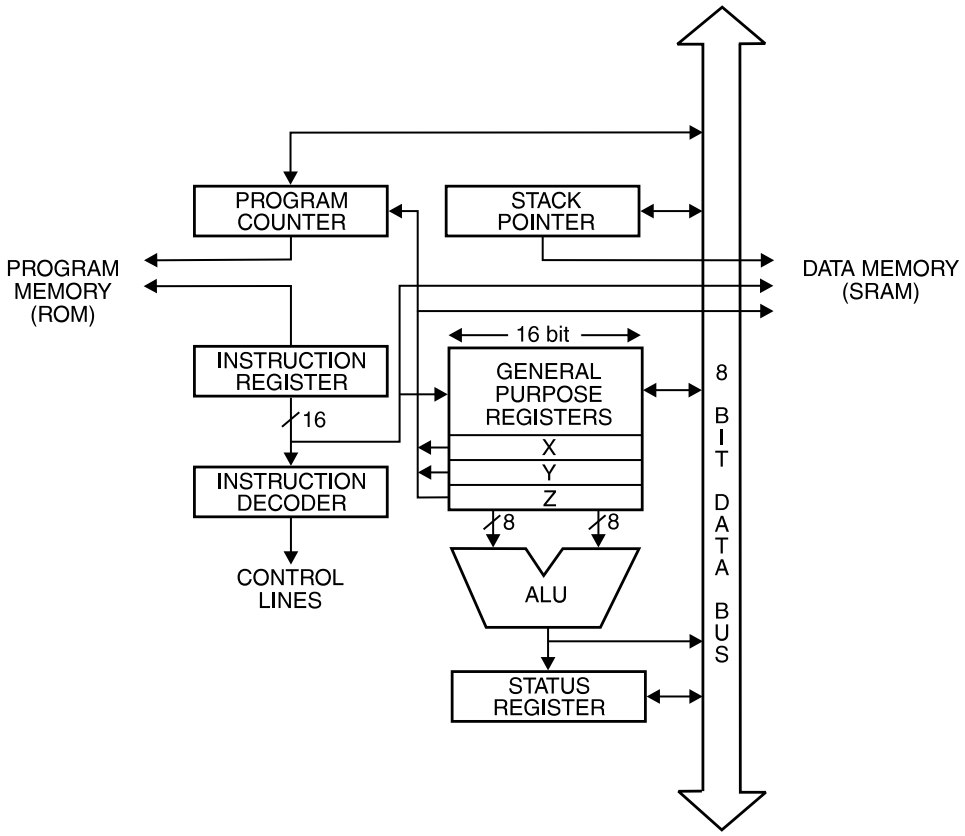
The AVR RISC microcontroller is a true 8-bit RISC architecture, ideally suited for embedded control applications. The AVR is offered as a gate level, soft macro in the ATL35 family.

The AVR supports a powerful set of 120 instructions. The AVR pre-fetches an instruction during prior instruction execution, enabling the execution of one instruction per clock cycle.

The Fast Access RISC register file consists of 32 general purpose working registers. These 32 registers eliminate the data transfer delay in the traditional program code intensive accumulator architectures.

The AVR can incorporate up to 8K x 8 program memory (ROM) and 64K x 8 data memory (SRAM). Also included are several optional peripherals: UART, 8-bit timer/counter, 16-bit timer/counter, external and internal interrupts and programmable watchdog timer.

AVR (8-bit RISC) ASIC Core



ARM7TDMI Embedded Microcontroller Core

The ARM7TDMI is a powerful 32-bit processor offered as an embedded core in the ATL35 series arrays.

The ARM7TDMI is a member of the Advanced RISC Machines (ARM) family of general purpose 32-bit microprocessors, which offer high performance for very low power consumption.

The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective chip.

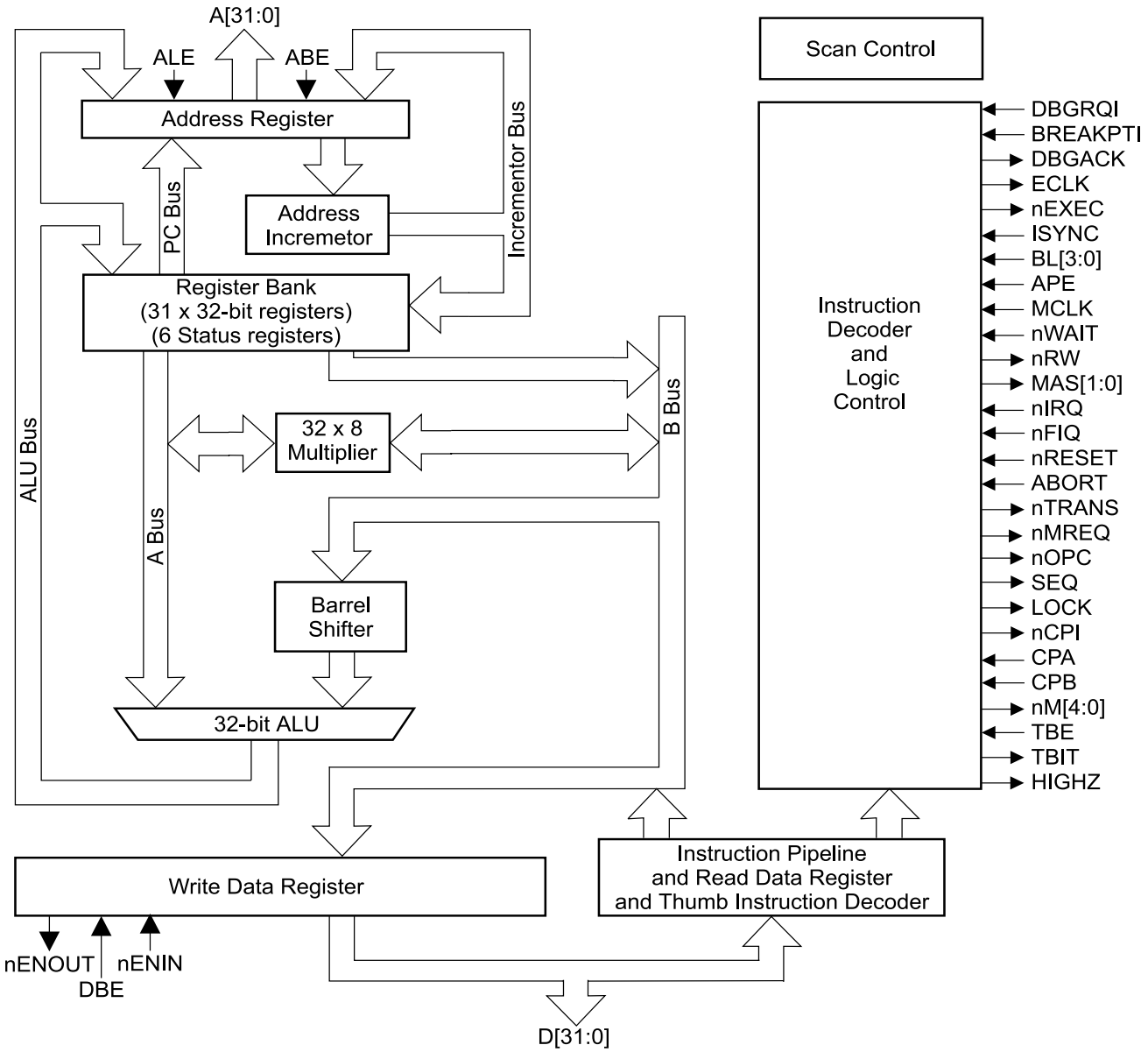
Pipelining is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is

being decoded, and a third instruction is being fetched from memory.

The ARM memory interface has been designed to allow the performance potential to be realized without incurring high costs in the memory system. Speed critical control signals are pipelined to allow system control functions to be implemented in standard low-power logic, and these control signals facilitate the exploitation of the fast local access modes offered by industry standard SRAMs.

The ARM7TDMI core includes several optional peripheral macros. The options offered are Real-time Clock, DMA Controller, USART, External Bus Interface, Interrupt, Timer and Advanced Power Management and Controller.

ARM7TDMI Embedded Microcontroller Core



OakDSPCore

Atmel's embedded OakDSPCore is a 16-bit, general purpose, low-power, low-voltage and high-speed Digital Signal Processor (DSP).

OAK is designed for mid-to-high-end telecommunications and consumer electronics applications, where low-power and portability are major requirements. Among the applications supported are digital cellular telephones, fast modems, advanced facsimile machines and hard disk drives. Oak is available as a DSP core in Atmel's Gate Array cell library, to be utilized as an engine for DSP-based Gate Array/Embedded Array. It is specified with several levels of modularity in SRAM, ROM, I/O blocks, allowing efficient DSP-based Gate Array/Embedded Array development.

OAK is aimed at achieving the best cost-performance factor for a given (small) silicon area. As a key element of a system-on-chip, it takes into account such requirements as program size, data memory size, glue logic and power management.

The Oak core consists of three main execution units operating in parallel: the Computation/Bit-Manipulation Unit (CBU), the Data Addressing Arithmetic Unit (DAAU) and the Program Control Unit (PCU).

The Core also contains ROM and SRAM addressing units, and Program Control Logic (PCL). All other peripheral blocks, which are application specific, are defined as part of the user-specific logic and implemented around the DSP core on the same silicon die.

Oak has an enhanced set of DSP and general microprocessor functions to meet most application requirements. The OAK programming model and instruction set are aimed at straightforward generation of efficient and compact code.

LodeDSPCore

The LodeDSPCore will be offered in the ATL35 series arrays as an embedded core. Lode is an advanced, 16-bit Digital Signal Processor (DSP) core designed for optimal performance in digital cellular, speech and voice communications applications.

The Lode core architecture efficiently performs the baseband functions - speech compression, forward error correction, and modem functions - required by digital cellular standards.

Lode is the first general-purpose DSP that provides two multiplier-accumulators (MACs) that reduce power consumption by effectively cutting cycle times in half.

Lode's suite of user-friendly development tools are easy to learn, thus accelerating the time it takes to get your product to market.

ATL35 Series Cell Library

Atmel's ATL35 Series gate arrays make use of an extensive library of cell structures, including logic cells, buffers and inverters, multiplexers, decoders, and I/O options. Soft macros are also available.

The ATL35 Series PLL operates at frequencies of up to 250 MHz with minimal phase error and jitter, making it ideal for frequency synthesis of high speed on-chip clocks and chip to chip synchronization.

Output buffers are programmable to meet the voltage and current requirements of PCI (20 mA).

These cells are characterized by use of SPICE modeling at the transistor level, with performance verified on manufactured test arrays. Characterization is performed over the rated temperature and voltage ranges to ensure that the simulation accurately predicts the performance of the finished product.

Cell Index

Cell Name	Description	Gate Count
ADD3X	1-bit Full Adder with Buffered Outputs	10
AND2	2-input AND	2
AND2H	2-input AND - High-drive	3
AND3	3-input AND	3
AND3H	3-input AND - High-drive	4
AND4	4-input AND	3
AND4H	4-input AND - High-drive	4
AND5	5-input AND	5
AOI22	2-input AND into 2-input NOR	2
AOI222	Two, 2-input ANDs into 2-input NOR	2
AOI2223	Three, 2-input ANDs into 3-input NOR	4
AOI2223H	Three, 2-input ANDs into 3-input NOR - High-drive	8
AOI222H	Two, 2-input ANDs into 2-input NOR - High-drive	4
AOI22H	2-input AND into 2-input NOR - High-drive	4
AOI23	2-input AND into 3-input NOR	3
BUF1	1x Buffer	2
BUF2	2x Buffer	2
BUF2T	2x Tri-state Bus Driver with Active-high Enable	4
BUF2Z	2x Tri-state Bus Driver with Active-low Enable	4
BUF3	3x Buffer	3
BUF4	4x Buffer	3
BUF8	8x Buffer	5
BUF12	12x Buffer	8
BUF16	16x Buffer	10
CLA7X	7-input Carry Lookahead	5
DEC4	2:4 Decoder	8
DEC4N	2:4 Decoder with Active-low Enable	10
DEC8N	3:8 Decoder with Active-low Enable	22

Cell Index (Continued)

Cell Name	Description	Gate Count
DFF	D Flip-flop	8
DFFBCPX	D Flip-flop with Asynchronous Clear and Preset with Complementary Outputs	16
DFFBSRX	D Flip-flop with Asynchronous Set and Reset with Complementary Outputs	16
DFFC	D Flip-flop with Asynchronous Clear	9
DFFR	D Flip-flop with Asynchronous Reset	10
DFFRQ	Quad D Flip-flop with Asynchronous Reset	40
DFFS	D Flip-flop with Asynchronous Set	9
DFFSR	D Flip-flop with Asynchronous Set and Reset	11
DLY1	Delay Buffer 1.0 ns	7
DLY2	Delay Buffer 1.5 ns	9
DLY3	Delay Buffer 2.0 ns	11
DLY4	Delay Buffer 4.5 ns	20
DSS	Set scan Flip-flop	12
DSSBCPY	Set scan Flip-flop with Clear and Preset	16
DSSBR	Set scan Flip-flop with Reset	14
DSSBS	Set scan Flip-flop with Set	14
DSSR	Set scan D Flip-flop with Reset	12
DSSS	Set scan D Flip-flop with Set	14
DSSSR	Set scan D Flip-flop with Set and Reset	16
HLD1	Bus Hold Cell	4
INV1	1x Inverter	1
INV1D	Dual 1x Inverter	2
INV1Q	Quad 1x Inverter	4
INV1TQ	Quad 1x Tri-state Inverter with Active-high Enable	8
INV2	2x Inverter	1
INV2T	2x Tri-state Inverter with Active-high Enable	3
INV3	3x Inverter	2
INV4	4x Inverter	2
INV8	8x Inverter	4
INV10	10x Inverter	8
JKF	JK Flip-flop	10
JKFBCPX	Clear Preset JK Flip-flop with Asynchronous Clear and Preset and Complementary Outputs	16
JKFC	JK Flip-flop with Asynchronous Clear	12
LAT	LATCH	6

Cell Index (Continued)

Cell Name	Description	Gate Count
LATBG	LATCH with Complementary Outputs and Inverted Gate Signal	6
LATBH	LATCH with High-drive Complementary Outputs	7
LATR	LATCH with Reset	5
LATS	LATCH with Set	6
LATSR	LATCH with Set and Reset	8
MUX2	2:1 MUX	4
MUX2H	2:1 MUX - High-drive	5
MUX2I	2:1 MUX with Inverted Output	3
MUX2IH	2:1 MUX with Inverted Output - High-drive	4
MUX2N	2:1 MUX with Active-low Enable	5
MUX2NQ	Quad 2:1 MUX with Active-low Enable	18
MUX2Q	Quad 2:1 MUX	16
MUX3I	3:1 MUX with Inverted Output	6
MUX3IH	3:1 MUX with Inverted Output - High-drive	8
MUX4	4:1 MUX	10
MUX4X	4:1 MUX with Transmission Gate Data Inputs	9
MUX4XH	4:1 MUX with Transmission Gate Data Inputs - High-drive	10
MUX5H	5:1 MUX - High-drive	14
MUX8	8:1 MUX	20
MUX8N	8:1 MUX with Active-low Enable	20
MUX8XH	8:1 MUX with Transmission Gate Data Inputs - High-drive	16
NAN2	2-input NAND	2
NAN2D	Dual 2-input NAND	3
NAN2H	2-input NAND - High-drive	2
NAN3	3-input NAND	2
NAN3H	3-input NAND - High-drive	3
NAN4	4-input NAND	3
NAN4H	4-input NAND - High-drive	4
NAN5	5-input NAND	5
NAN5H	5-input NAND - High-drive	6
NAN5S	5-input NAND with Set	3
NAN6	6-input NAND	6
NAN6H	6-input NAND - High-drive	7
NAN8	8-input NAND	7
NAN8H	8-input NAND - High-drive	8
NOR2	2-input NOR	2

Cell Index (Continued)

Cell Name	Description	Gate Count
NOR2D	Dual 2-input NOR	3
NOR2H	2-input NOR - High-drive	2
NOR3	3-input NOR	2
NOR3H	3-input NOR - High-drive	3
NOR4	4-input NOR	3
NOR4H	4-input NOR - High-drive	5
NOR5	5-input NOR	5
NOR5S	5-input NOR with Set	3
NOR8	8-input NOR	7
OAI22	2-input OR into 2-input NAND	2
OAI222	Two, 2-input ORs into 2-input NAND	3
OAI22224	Four, 2-input ORs into 4-input NAND	8
OAI222H	Two, 2-input ORs into 2-input NAND - High-drive	6
OAI22H	2-input OR into 2-input NAND - High-drive	4
OAI23	2-input OR into 3-input NAND	3
ORR2	2-input OR	2
ORR2H	2-input OR - High-drive	3
ORR3	3-input OR	3
ORR3H	3-input OR - High-drive	4
ORR4	4-input OR	3
ORR4H	4-input OR - High-drive	4
ORR5	5-input OR	5
XNR2	2-input Exclusive NOR	4
XNR2H	2-input Exclusive NOR - High-drive	4
XOR2	2-input Exclusive OR	4
XOR2H	2-input Exclusive OR - High-drive	4

3.3 Volt I/O Buffer Cell Index

Cell Name	Description
PFIPCI	PCI Input
PFPECLL	Positive ECL Output
PFPECLR	Positive ECL Output
PIC	CMOS Input
PICH	CMOS Input - High-drive
PICI	CMOS Inverting Input
PICS	CMOS Input with Schmitt Trigger
PICSI	CMOS Inverting Input with Schmitt Trigger
PID	Differential Input
PO11	2 mA Tri-state Output
PO11F	2 mA Tri-state Output (fast)
PO11S	2 mA Tri-state Output (slow)
PO22	4 mA Tri-state Output
PO22F	4 mA Tri-state Output (fast)
PO22I	4 mA Inverting Tri-state Output
PO22S	4 mA Tri-state Output (slow)
PO33	6 mA Tri-state Output
PO33F	6 mA Tri-state Output (fast)
PO33S	6 mA Tri-state Output (slow)
PO44	8 mA Tri-state Output
PO44F	8 mA Tri-state Output (fast)
PO44S	8 mA Tri-state Output (slow)
PO55	10 mA Tri-state Output
PO55F	10 mA Tri-state Output (fast)
PO55S	10 mA Tri-state Output (slow)

3.3 Volt I/O Buffer Cell Index

Cell Name	Description
PO66	12 mA Tri-state Output
PO66F	12 mA Tri-state Output (fast)
PO66S	12 mA Tri-state Output (slow)
PO77	14 mA Tri-state Output
PO77F	14 mA Tri-state Output (fast)
PO77S	14 mA Tri-state Output (slow)
PO88	16 mA Tri-state Output
PO88F	16 mA Tri-state Output (fast)
PO88S	16 mA Tri-state Output (slow)
PO99	18 mA Tri-state Output
PO99F	18 mA Tri-state Output (fast)
PO99S	18 mA Tri-state Output (slow)
POAA	Tri-state Output
POAAF	Tri-state Output (fast)
POAAS	Tri-state Output (slow)
POBB	Tri-state Output
POBBF	Tri-state Output (fast)
POBBS	Tri-state Output (slow)
POCC	Tri-state Output
POCCF	Tri-state Output (fast)
POCCS	Tri-state Output (slow)
PX1L	XTAL Oscillator
PX2L	XTAL Oscillator
PX3L	XTAL Oscillator
PX4L	XTAL Oscillator

5.0 Volt Tolerant[1]

Cell Name	Description
PFIPCI	PCI Input
PFIPCIV	5V Tolerant PCI Input
PIC	CMOS Input
PICH	CMOS Input - High-drive
PICI	CMOS Inverting Input
PICS	CMOS Input with Schmitt Trigger
PICSI	CMOS Inverting Input with Schmitt Trigger
PICSV	5V Tolerant CMOS Input with Schmitt Trigger
PICV	5V Tolerant CMOS Input
PO11	2 mA Tri-state Output
PO11F	2 mA Tri-state Output (fast)
PO11S	2 mA Tri-state Output (slow)
PO11V	5V Tolerant 2 mA Tri-state Output
PO11VF	5V Tolerant 2 mA Tri-state Output (fast)
PO11VS	5V Tolerant 2 mA Tri-state Output (slow)
PO22	4 mA Tri-state Output
PO22F	4 mA Tri-state Output (fast)
PO22I	4 mA Inverting Tri-state Output
PO22S	4 mA Tri-state Output (slow)
PO22V	5V Tolerant 4 mA Tri-state Output
PO22VF	5V Tolerant 4 mA Tri-state Output (fast)
PO22VS	5V Tolerant 4 mA Tri-state Output (slow)
PO33	6 mA Tri-state Output
PO33F	6 mA Tri-state Output (fast)
PO33S	6 mA Tri-state Output (slow)
PO33V	5V Tolerant 6 mA Tri-state Output
PO33VF	5V Tolerant 6 mA Tri-state Output (fast)
PO33VS	5V Tolerant 6 mA Tri-state Output (slow)
PO44	8 mA Tri-state Output
PO44F	8 mA Tri-state Output (fast)
PO44S	8 mA Tri-state Output (slow)
PO44V	5V Tolerant 8 mA Tri-state Output
PO44VF	5V Tolerant 8 mA Tri-state Output (fast)
PO44VS	5V Tolerant 8 mA Tri-state Output (slow)
PO55	10 mA Tri-state Output
PO55F	10 mA Tri-state Output (fast)

5.0 Volt Tolerant[1]

Cell Name	Description
PO55S	10 mA Tri-state Output (slow)
PO55V	5V Tolerant 10 mA Tri-state Output
PO55VF	5V Tolerant 10 mA Tri-state Output (fast)
PO55VS	5V Tolerant 10 mA Tri-state Output (slow)
PO66	12 mA Tri-state Output
PO66F	12 mA Tri-state Output (fast)
PO66S	12 mA Tri-state Output (slow)
PO66V	5V Tolerant 12 mA Tri-state Output
PO66VF	5V Tolerant 12 mA Tri-state Output (fast)
PO66VS	5V Tolerant 12 mA Tri-state Output (slow)
PO77	14 mA Tri-state Output
PO77F	14 mA Tri-state Output (fast)
PO77S	14 mA Tri-state Output (slow)
PO77V	5V Tolerant 14 mA Tri-state Output
PO77VF	5V Tolerant 14 mA Tri-state Output (fast)
PO77VS	5V Tolerant 14 mA Tri-state Output (slow)
PO88	16 mA Tri-state Output
PO88F	16 mA Tri-state Output (fast)
PO88S	16 mA Tri-state Output (slow)
PO88V	5V Tolerant 16 mA Tri-state Output
PO88VF	5V Tolerant 16 mA Tri-state Output (fast)
PO88VS	5V Tolerant 16 mA Tri-state Output (slow)
PO99	18 mA Tri-state Output
PO99F	18 mA Tri-state Output (fast)
PO99S	18 mA Tri-state Output (slow)
PO99V	5V Tolerant 18 mA Tri-state Output
PO99VF	5V Tolerant 18 mA Tri-state Output (fast)
PO99VS	5V Tolerant 18 mA Tri-state Output (slow)
POAA	Tri-state Output
POAAF	Tri-state Output (fast)
POAAS	Tri-state Output (slow)
POAAV	5V Tolerant mA Tri-state Output
POAAVF	5V Tolerant mA Tri-state Output (fast)
POAAVS	5V Tolerant mA Tri-state Output (slow)
POBB	Tri-state Output
POBBF	Tri-state Output (fast)

5.0 Volt Tolerant[1]

Cell Name	Description
POBBS	Tri-state Output (slow)
POBBV	5V Tolerant mA Tri-state Output
POBBVF	5V Tolerant mA Tri-state Output (fast)
POBBVS	5V Tolerant mA Tri-state Output (slow)
POCC	Tri-state Output
POCCF	Tri-state Output (fast)
POCCS	Tri-state Output (slow)
PX1L	XTAL Oscillator
PX2L	XTAL Oscillator
PX3L	XTAL Oscillator
PX4L	XTAL Oscillator

5.0 Volt Compliant[2]

Cell Name	Description
PICV5	5V Compliant
PO22V5	5V Compliant 4 mA Tri-state Output
PO44V5	5V Compliant 8 mA Tri-state Output

Notes:
1. Tolerant: Can accept a 5.0 volt input but uses 3.3 volt power supply.
2. Compliant: Can accept a 5.0 volt input or output. Requires a 5.0 volt power supply.

Absolute Maximum Ratings*

Operating Ambient Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Maximum Input Voltage:	
Inputs	V_{DD} + 0.5V
5V Tolerant/Compliant	V_{DD5} + 0.5V
Maximum Operating Voltage (V_{DD})	3.6V
Maximum Operating Voltage (V_{DD5})	5.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.5 Volt DC Characteristics

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Symbol	Parameter	Buffer	Test Condition	Min	Typ	Max	Units
T_A	Operating Temperature	All		-55		125	°C
V_{DD}	Supply Voltage	All		2.3	2.5	2.7	V
I_{IH}	High-level Input Current	CMOS	$V_{IN} = V_{DD}$, $V_{DD} = V_{DD}$ (max)			10	µA
		PCI				10	
I_{IL}	Low-level Input Current	CMOS	$V_{IN} = V_{SS}$, $V_{DD} = V_{DD}$ (max)	-10			µA
		PCI		-10			
I_{OZ}	High-impedance State Output Current	All	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = V_{DD}$ (max), No pull-up	-10		10	µA
I_{OS}	Output Short-circuit Current	PO11	$V_{OUT} = V_{DD}$, $V_{DD} = V_{DD}$ (max)		9		mA
		PO11	$V_{OUT} = V_{SS}$, $V_{DD} = V_{DD}$ (max)		6		
V_{IH}	High-level Input Voltage	CMOS		$0.7V_{DD}$			V
		PCI		$0.475V_{DD}$			
		CMOS Schmitt		$0.7V_{DD}$	1.5		
V_{IL}	Low-level Input Voltage	CMOS				$0.3V_{DD}$	V
		PCI				$0.325V_{DD}$	
		CMOS Schmitt			1.0	$0.3V_{DD}$	
V_{HYS}	Hysteresis	CMOS Schmitt			0.5		V
V_{OH}	High-level Output Voltage	PO11	I_{OH} = 1.4 mA, $V_{DD} = V_{DD}$ (min)	$0.7V_{DD}$			V
		PCI	I_{OH} = -500 µA	$0.9V_{DD}$			
V_{OL}	Low-level Output Voltage	PO11	I_{OL} = 1.4 mA, $V_{DD} = V_{DD}$ (min)			0.4	V
		PCI	I_{OL} = 1.5 mA			$0.1V_{DD}$	

3.3 Volt DC Characteristics

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Symbol	Parameter	Buffer	Test Condition	Min	Typ	Max	Units
T_A	Operating Temperature	All		-55		125	°C
V_{DD}	Supply Voltage	All		3.0	3.3	3.6	V
I_{IH}	High-level Input Current	CMOS	$V_{IN} = V_{DD}$, $V_{DD} = V_{DD}$ (max)			10	µA
		PCI				10	
I_{IL}	Low-level Input Current	CMOS	$V_{IN} = V_{SS}$, $V_{DD} = V_{DD}$ (max)	-10			µA
		PCI		-10			
I_{OZ}	High-impedance State Output Current	All	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = V_{DD}$ (max), No pull-up	-10		10	µA
I_{OS}	Output Short-circuit Current	PO11	$V_{OUT} = V_{DD}$, $V_{DD} = V_{DD}$ (max)		14		mA
		PO11	$V_{OUT} = V_{SS}$, $V_{DD} = V_{DD}$ (max)		-9		
V_{IH}	High-level Input Voltage	CMOS, LVTTL		2.0			V
		PCI		$0.475V_{DD}$			
		CMOS/TTL-level Schmitt		2.0	1.7		
V_{IL}	Low-level Input Voltage	CMOS				0.8	V
		PCI				$0.325V_{DD}$	
		CMOS/TTL-level Schmitt			1.1	0.8	
V_{HYS}	Hysteresis	TTL-level Schmitt			0.6		V
V_{OH}	High-level Output Voltage	PO11	I_{OH} = 2 mA, $V_{DD} = V_{DD}$ (min)	$0.7V_{DD}$			V
		PCI	I_{OH} = -500 µA	$0.9V_{DD}$			
V_{OL}	Low-level Output Voltage	PO11	I_{OL} = 2 mA, $V_{DD} = V_{DD}$ (min)			0.4	V
		PCI	I_{OL} = 1.5 mA			$0.1V_{DD}$	

5.0 Volt DC Characteristics

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Symbol	Parameter	Buffer	Test Condition	Min	Typ	Max	Units
T_A	Operating Temperature	All		-55		125	°C
V_{DD}	Supply Voltage	5V Tolerant		3.0	3.3	3.6	V
V_{DD5}	Supply Voltage	5V Compliant		4.5	5.0	5.5	V
I_{IH}	High-level Input Current	CMOS	$V_{IN} = V_{DD}$, $V_{DD} = V_{DD}$ (max)			10	µA
I_{IL}	Low-level Input Current	CMOS	$V_{IN} = V_{SS}$, $V_{DD} = V_{DD}$ (max)	-10			µA
I_{OZ}	High-impedance State Output Current	All	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = V_{DD}$ (max), No pull up	-10		10	µA
I_{OS}	Output Short-circuit Current	PO11V	$V_{OUT} = V_{DD}$, $V_{DD} = V_{DD}$ (max)		8		mA
		PO11V	$V_{OUT} = V_{SS}$, $V_{DD} = V_{DD}$ (max)		-7		
V_{IH}	High-level Input Voltage	PICV, PICV5		2.0	5.0	5.5	V
		PCI		$0.475V_{DD}$	5.0	5.5	
		CMOS/TTL-level Schmitt		2.0	1.7		
V_{IL}	Low-level Input Voltage	PICV, PICV5			$0.5V_{DD}$	0.8	V
		PCI				$0.325V_{DD}$	
		CMOS/TTL-level Schmitt			1.1	0.8	
V_{HYS}	Hysteresis	CMOS/TTL-level Schmitt			0.6		V
V_{OH}	High-level Output Voltage	PO11V	I_{OH} = -1.7 mA	$0.7V_{DD}$			V
		PO11V5	I_{OH} = -1.7 mA	$0.7V_{DD5}$			
V_{OL}	Low-level Output Voltage	PO11V, PO11V5	I_{OL} = 1.7 mA			0.5	V

I/O Buffer DC Characteristics

Symbol	Parameter	Test Condition	Typical	Units
C_{IN}	Capacitance, Input Buffer (die)	3.3V	2.4	pF
C_{OUT}	Capacitance, Output Buffer (die)	3.3V	5.6	pF
$C_{I/O}$	Capacitance, Bidirectional	3.3V	6.6	pF

Testability Techniques

For complex designs, involving blocks of memory and/or cores, careful attention must be given to design-for-test techniques. The sheer size of complex designs and the number of functional vectors that would need to be created to exercise them fully, strongly suggests the use of more efficient techniques. Combinations of SCAN paths, multiplexed access to memory and/or core blocks, and built-in-self-test logic must be employed, in addition to functional test patterns, to provide both the user and Atmel the ability to test the finished product.

An example of a highly complex design could include a PLL for clock management or synthesis, a microcontroller or DSP engine or both, SRAM to support the microcontroller or DSP engine, and glue logic to support the interconnectivity of each of these blocks. The design of each of these blocks must take into consideration the fact that the manufactured device will be tested on a high performance digital tester. Combinations of parametric, functional, and structural tests, defined for digital testers, should be employed to create a suite of manufacturing tests.

The type of block dictates the type of testability technique to be employed. The PLL will, by construction, provide access to key nodes so that functional and / or parametric testing can be performed. Since a digital tester must control

all the clocks during the testing of a Gate Array/Embedded Array, provision must be made for the VCO to be bypassed. Atmel's PLLs include a multiplexing capability for just this purpose. The addition of a few pins will allow other portions of the PLL to be isolated for test, without impinging upon the normal functionality.

In a similar vein, access to microcontroller, DSP and SRAM blocks must be provided so that controllability and observability of the inputs and outputs to the blocks are achieved with the minimum amount of preconditioning. The AVR and ARM microcontrollers support SCAN testing, as do the three main execution units of the OakDSP. SRAM and CAM blocks need to provide access to both address and data ports so that comprehensive memory tests can be performed. Multiplexing I/O pins provides a method for providing this accessibility.

The glue logic can be designed using full SCAN techniques to enhance its testability.

It should be noted that, in almost all of these cases, the purpose of the testability technique is to provide Atmel a means to assess the structural integrity of a Gate Array/Embedded Array; i.e., sort devices with manufacturing-induced defects. All of the techniques described above should be considered supplemental to a set of patterns which exercise the functionality of the design in its anticipated operating modes.

Advanced Packaging

The ATL35 Series gate arrays are offered in a wide variety of standard packages, including plastic and ceramic quad flatpacks, thin quad flatpacks, ceramic pin grid arrays, and ball grid arrays. High volume onshore and offshore contractors provide assembly and test for commercial product, with prototype capability in Colorado Springs. Custom package designs are also available as required to meet a customer's specific needs, and are supported through Atmel's package design center. When a standard package cannot meet a customer's need, a package can be designed to precisely fit the application and to maintain the performance obtained in silicon. Atmel has delivered custom-designed packages in a wide variety of configurations.

Packaging Options

Package Type	Pin Count
PQFP	44, 52, 64, 80, 100, 120, 128, 132, 144, 160, 184, 208, 240, 304
Power Quad	144, 160, 208, 240, 304
L/TQFP	32, 44, 48, 64, 80, 100, 120, 128, 144, 160, 176, 216
PLCC	20, 28, 32, 44, 52, 68, 84
CPGA	64, 68, 84, 100, 124, 144, 155, 180, 223, 224, 299, 391
CQFP	64, 68, 84, 100, 120, 132, 144, 160, 224, 340
PBGA	121, 169, 208, 217, 225, 256, 272, 300, 304, 313, 316, 329, 352, 388, 420, 456
Super BGA	168, 204, 240, 256, 304, 352, 432, 560, 600
Low-profile Mini BGA	132, 144, 160, 180, 208
Chip-scale BGA[1]	40, 49, 56, 64, 81, 84, 96, 100, 128

Note: 1. Partial list

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