

MN100370-X REV 0C0

 Original Creation Date: 10/30/95
 Last Update Date: 10/21/96
 Last Major Revision Date: 10/30/95

LOW POWER UNIVERSAL DEMULTIPLEXER/DECODER
General Description

The 100370 universal demultiplexer/decoder functions as either a dual 1-of-4 decoder or as a single 1-of-8 decoder, depending on the signal applied to the Mode Control (M) input. In the dual mode, each half has a pair of active - LOW Enable (E) inputs. Pin assignments for the E Inputs are such that in the 1-of-8 mode they can easily be tied together in pairs to provide two active-LOW enable (E1a to E1b, E2a to E2b). Signals applied to auxiliary inputs Ha, Hb and Hc determine whether the outputs are active HIGH or active LOW. In the dual 1-of-4 mode the Address inputs are Aoa, Ala and Aob, Alb with A2a unused (i.e., left open, tied to VEE or with LOW signal applied). In the 1-of-8 mode, the Address inputs are Aoa, Ala, A2a with Aob and Alb LOW or open. All inputs have 50K ohm pulldown resistors.

Industry Part Number

100370

NS Part Numbers

 100370DMQB
 100370FMQB

Prime Die

F370

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp Description Temp (°C)

1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 35% power reduction of the 100170
- 2000V ESD protection
- Pin/function compatible with 100170
- Voltage compensated operating range= -4.2V to -5.7V

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature (Tstg)	-65C to +150C
Maximum Junction Temperature (Tj)	
Ceramic	+175C
Plastic	+150C
Vee Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	Vee to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (Tc)	
Commercial	0 C to +85 C
Industrial	-40 C to +85C
Military	-55C to +125C
Supply Voltage (Vee)	-5.7V to -4.2V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
 DC: Vee Range: -4.2V to -5.7V, Tc= -55C to +125C, VCC=VCCA=GND

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input HIGH Current	VEE=-5.7V, VM=-0.87V	1, 3	INPUTS		240	uA	1, 2
			1, 3	INPUTS		340	uA	3
IIL	Input Low Current	VEE=-4.2V, VM=-1.83V	1, 3	INPUTS	0.5		uA	1, 2, 3
VOH	Output HIGH Voltage	VEE=-4.2V/-5.7V, VIH=-0.87V, VIL=-1.83V, LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1025	-870	mV	1, 2
			1, 3	OUTPUTS	-1085	-870	mV	3
VOL	Output LOW Voltage	Vee=-4.2V/-5.7V, VIH=-0.87V, VIL=-1.83V, LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1830	-1620	mV	1, 2
			1, 3	OUTPUTS	-1830	-1555	mV	3
VOHC	Output HIGH Voltage Corner Point High	Vee=-4.2V/-5.7V, VIH=-1.165V, VIL=-1.475V, Loading: 50 Ohms to -2.0V	1, 3	OUTPUTS	-1035		mV	1, 2
			1, 3	OUTPUTS	-1085		mV	3
VOLC	Output LOW Voltage Corner Point High	Vee=-4.2V/-5.7V, VIH=-1.165V, VIL=-1.475V, LOADING: 50 Ohms to -2.0V	1, 3	OUTPUTS		-1610	mV	1, 2
			1, 3	OUTPUTS		-1555	mV	3
VIH	Input HIGH Voltage		1, 3, 7	INPUTS	-1165	-870	mV	1, 2, 3
VIL	Input LOW Voltage		1, 3, 7	INPUTS	-1830	-1475	mV	1, 2, 3
IEE	Input LOW Voltage	VEE=-4.2/-5.7V	1, 3	INPUTS	-105	-36	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
 AC: VEE Range: -4.2V to -5.7V, LOADING: 50 Ohms to -2.0V, VCC=VCCA=GND

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPLH/tPHL(1)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	$\overline{Ena}/\overline{Enb}$ to Zn	0.4	2.2	ns	9
			2, 4	$\overline{Ena}/\overline{Enb}$ to Zn	0.4	2.7	ns	10
			2, 4	$\overline{Ena}/\overline{Enb}$ to Zn	0.3	2.4	ns	11
tPLH/tPHL(2)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	Ana/Anb to Zn	0.4	2.4	ns	9
			2, 4	Ana/Anb to Zn	0.4	2.9	ns	10
			2, 4	Ana/Anb to Zn	0.3	2.6	ns	11
tPLH/tPHL(3)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	Ha/Hb/Hc to Zn	0.4	2.4	ns	9
			2, 4	Ha/Hb/Hc to Zn	0.4	2.9	ns	10
			2, 4	Ha/Hb/Hc to Zn	0.3	2.6	ns	11
tPLH/tPHL(4)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	M to Zn	0.6	2.8	ns	9
			2, 4	M to Zn	0.7	3.7	ns	10
			2, 4	M to Zn	0.4	3.1	ns	11
tTLH/tTHL	Transistion Time	VEE=-4.2/-5.7V	6	Zn	0.3	1.6	ns	9, 10, 11

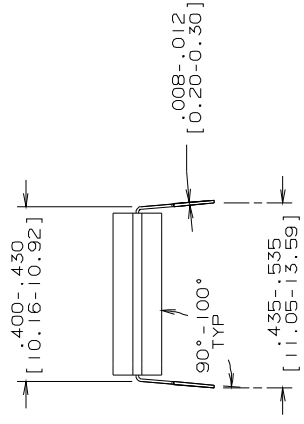
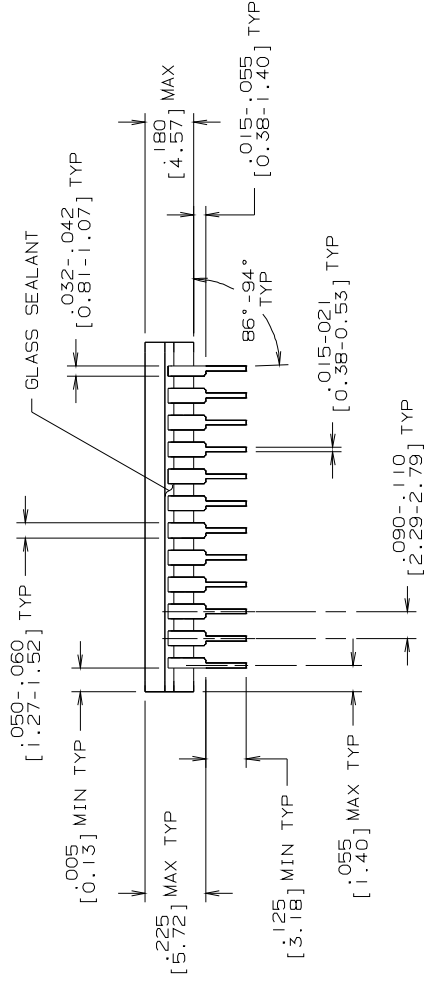
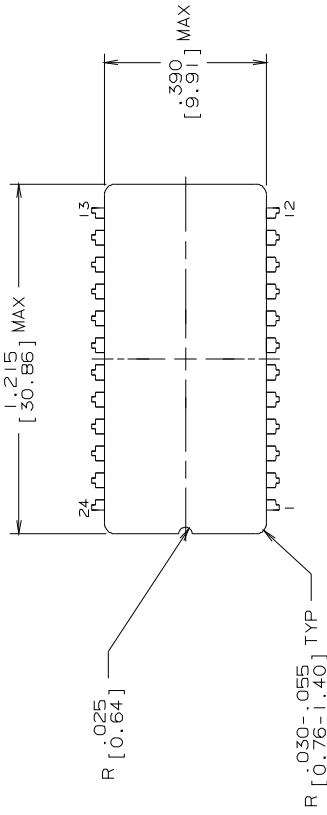
- Note 1: Screen tested 100% on each device at -55 C, +25 C and +125 C temp., subgroups 1, 2, 3, 7 & 8.
- Note 2: Screen tested 100% on each device at +25 C temp only, subgroup A9.
- Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, +125 C & -55 C temp., subgroups A1, 2, 3, 7 & 8.
- Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, subgroup A9, and at +125 C & -55 C temp., subgroups A10 & 11.
- Note 5: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C temp. only, subgroup A9.
- Note 6: Not tested at +25 C, +125 C & -55 C temp. (DESIGN CHARACTERIZATION DATA).
- Note 7: Guaranteed by applying specified input condition and testing VOH/VOL.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
J24ERJ	CERDIP(J), 24LD .400 CENTERS (P/P DWG)
P000090A	CERDIP (J), 24LD .400 CENTERS (PIN OUT)
P000091A	CERPAC, QUAD, 24 LEAD (PIN OUT)
W24BRE	CERPAC, QUAD, 24 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
J	REVISE AND REDRAW	09044	03/05/92 DEG/



MIL/AERO MIL-M-38510 CONFIGURATION CONTROL CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH	
APPROVALS	DATE
DRAWN D.E. GRADY	03/05/92
DTG. CHK.	
ENGR. CHK.	
APPROVAL	
SCALE N/A	DRAWING NUMBER C
FORMERLY I	MKT-J24E
SHEET 1	OF 1

NOTES: UNLESS OTHERWISE SPECIFIED

- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICRONS/5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
- LEAD THICKNESS MAY BE INCREASED BY .003 [0.08] MAXIMUM AFTER LEAD FINISH APPLIED.
- BUMPERS ARE AVAILABLE ON CERTAIN PRODUCTS. BUMPERS WILL ADD .040 [1.02] MAX TO THE LENGTH OF THE PACKAGE.
- NO JEDEC REGISTRATION AS OF 2/17/92.

NATIONAL SEMICONDUCTOR CORPORATION
 2900 Semiconductor Drive, Santa Clara, CA 95052-8090
 CERDIP (J),
 24 LEAD,
 .400 CENTERS