ProASIC3L Low-Power Flash FPGAs
with Flash*Freeze Technology

FlashLock

Features and Benefits

Low Power
- Dramatic Reduction in Dynamic and Static Power Savings
- 1.2 V to 1.5 V Core and I/O Voltage Support for Low Power
- Low Power Consumption in Flash*Freeze Mode Allows for Instantaneous Entry to / Exit from Low-Power Flash*Freeze Mode
- Supports Single-Voltage System Operation
- Low-Impedance Switches

High Capacity
- 250 k to 3 M System Gates
- Up to 504 kbits of True Dual-Port SRAM
- Up to 620 User I/Os

Reprogrammable Flash Technology
- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Live-at-Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design when Powered Off

High Performance
- 350 MHz (1.5 V systems) and 250 MHz (1.2 V systems) System Performance
- 3.3 V, 66 MHz, 66-Bit PCI (1.5 V systems) and 66 MHz, 32-Bit PCI (1.2 V systems)

In-System Programming (ISP) and Security
- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE 1532–compliant)
- FlashLock® to Secure FPGA Contents

High-Performance Routing Hierarchy
- Segmented, Hierarchical Routing and Clock Structure
- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

Advanced and Pro (Professional) I/Os
- 700 Mbps DDR, LVDS-Capable I/Os
- 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—up to 8 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V / 1.2 V, 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, and M-LVDS
- Voltage-Referenced I/O Standards: GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II (A3PE3000L only)
- Wide Range Power Supply Voltage Support per JESD8-B, Allowing I/Os to Operate from 2.7 V to 3.6 V
- Wide Range Power Supply Voltage Support per JESD8-12, Allowing I/Os to Operate from 1.14 V to 1.575 V
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold-Sparing I/Os Programmable Output Slew Rate and Drive Strength
- Programmable Input Delay (A3PE3000L only)
- Schmitt Trigger Option on Single-Ended Inputs (A3PE3000L)
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the ProASIC®3L Family (except PQ208)

Clock Conditioning Circuit (CCC) and PLL
- Six CCC Blocks, One with Integrated PLL (ProASIC3L) and All with Integrated PLL (ProASIC3EL)
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range 1.5 MHz to 250 MHz (1.2 V systems) and 350 MHz (1.5 V systems))

SRAMs and FIFOs
- Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations available)
- True Dual-Port SRAM (except ×18)
- 24 SRAM and FIFO Configurations with Synchronous Operation:
  - 250 MHz: For 1.2 V systems
  - 350 MHz: For 1.5 V systems

ARM® Processor Support in ProASIC3L FPGAs
- ARM Cortex™-M1 Soft Processor Available with or without Debug

Table 1 • **ProASIC3 Low-Power Product Family**

ProASIC3L Devices	A3P250L	A3P600L	A3P1000L	A3PE3000L
ARM Cortex-M1 Devices [1]		M1A3P600L	M1A3P1000L	M1A3PE3000L
System Gates	250 k	600 k	1 M	3 M
VersaTiles (D-flip-flops)	6,144	13,824	24,576	75,264
RAM kbits (1,024 bits)	36	108	144	504
4,608-Bit Blocks	8	24	32	112
FlashROM Bits	1 k	1 k	1 k	1 k
Secure (AES) ISP [2]	Yes	Yes	Yes	Yes
Integrated PLL in CCCs [3]	1	1	1	6
VersaNet Globals	18	18	18	18
I/O Banks	4	4	4	8
Maximum User I/Os	157	235	300	620
Package Pins VQFP PQFP FBGA	 VQ100 PQ208 FG144, FG256	 PQ208 FG144, FG256, FG484	 PQ208 FG144, FG256, FG484	 PQ208 [3] FG324, FG484, FG896

Notes:
1. *Refer to the Cortex-M1 product brief for more information.*
2. *AES is not available for ARM-enabled ProASIC3L devices.*
3. *For the A3PE3000L, the PQ208 package has six CCCs and two PLLs.*

I/Os Per Package [1]

ProASIC3L Low-Power Devices	A3P250L [2]		A3P600L		A3P1000L		A3PE3000L	
ARM Cortex-M1 Devices			M1A3P600L		M1A3P1000L		M1A3PE3000L [3]	
	I/O Type							
Package	Single-Ended I/O [4]	Differential I/O Pairs	Single-Ended I/O [4]	Differential I/O Pairs	Single-Ended I/O [4]	Differential I/O Pairs	Single-Ended I/O [4]	Differential I/O Pairs
VQ100	68	13		–	–	–	–	–
PQ208	151	34	154	35	154	35	147	65
FG144	97	24	97	25	97	25		
FG256	157	38	177	43	177	44	–	–
FG324	–	–	–	–	–	–	221	110
FG484	–	–	235	60	300	74	341	168
FG896	–	–	–	–	–	–	620	310

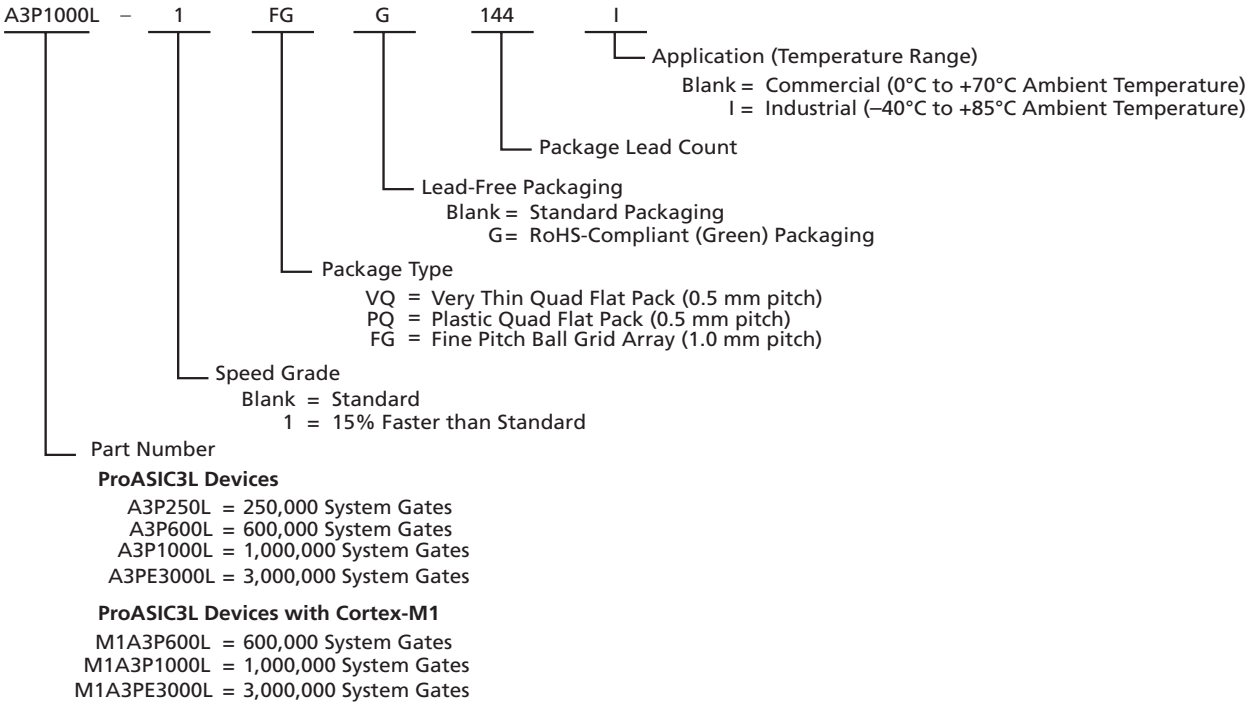
Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to the packaging section of the datasheet to ensure you are complying with design and board migration requirements.*
2. *For A3P250L devices, the maximum number of LVPECL pairs in east and west banks cannot exceed 15.*
3. *ARM Cortex-M1 support is TBD on this device.*
4. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
5. *FG256 and FG484 are footprint-compatible packages.*
6. *"G" indicates RoHS-compliant packages. Refer to "ProASIC3L Ordering Information" on page III for the location of the "G" in the part number.*
7. *For A3PE3000L devices, the usage of certain I/O standards is limited as follows:*
   – SSTL3(I) and (II): up to 40 I/Os per north or south bank
   – LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
   – SSTL2(I) and (II) / GTL+ 2.5 V/ GTL 2.5 V: up to 72 I/Os per north or south bank
8. *When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not as a regular I/O, the number of single-ended user I/Os available is reduced by one.*

Table 2 • **ProASIC3L FPGAs Package Sizes Dimensions**

Package	VQ100	PQ208	FG144	FG256	FG324	FG484	FG896
Length × Width (mm\mm)	14 × 14	28 × 28	13 × 13	17 × 17	19 × 19	23 × 23	31 × 31
Nominal Area (mm^2)	196	784	169	289	361	529	961
Pitch (mm)	0.5	0.5	1.0	1.0	1.0	1.0	1.0
Height (mm)	1.00	3.40	1.45	1.60	1.63	2.23	2.23

ProASIC3L Ordering Information



Temperature Grade Offerings

Package	A3P250L	A3P600L	A3P1000L	A3PE3000L
ARM Cortex-M1 Devices		**M1A3P600L**	**M1A3P1000L**	**M1A3PE3000L**
VQ100	C, I	–	–	
PQ208	C, I	C, I	C, I	C, I
FG144	C, I	C, I	C, I	
FG256	C, I	C, I	C, I	
FG324	–	–	–	C, I
FG484	–	C, I	C, I	C, I
FG896	–	–	–	C, I

Notes:

1. *C = Commercial temperature range: 0°C to 70°C ambient temperature.*
2. *I = Industrial temperature range: –40°C to 85°C ambient temperature.*

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.	–1
C [1]	✓	✓
I [2]	✓	✓

Notes:

1. *C = Commercial temperature range: 0°C to 70°C ambient temperature.*
2. *I = Industrial temperature range: –40°C to 85°C ambient temperature.*

Contact your local Actel representative for device availability:
http://www.actel.com/contact/default.aspx.

1 – ProASIC3L Device Family Overview

General Description

The ProASIC3L family of Actel flash FPGAs dramatically reduces dynamic power consumption by 40% and static power by 50%. These power savings are coupled with performance, density, true single-chip, 1.2 V to 1.5 V core and I/O operation as low as 1.2 V, reprogrammability, and advanced features.

Using Actel's proven Flash*Freeze technology enables users to shut off dynamic power instantaneously and switch the device to static mode without the need to switch off clocks or power supplies while retaining internal states of the device. This greatly simplifies power management on a board done through I/Os and clocks. In addition, optimized software tools using power-driven layout provide instant push-button power reduction.

Nonvolatile flash technology gives ProASIC3L devices the advantage of being a secure, low-power, single-chip solution that is live at power-up (LAPU). ProASIC3L offers dramatic dynamic power savings giving the FPGA users flexibility to combine low power with high performance.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC3L devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry (CCC) based on an integrated phase-locked loop (PLL). ProASIC3L devices support devices from 250 k system gates to 3 million system gates with up to 504 kbits of true dual-port SRAM and 620 user I/Os.

M1 ProASIC3L devices support the high-performance, 32-bit Cortex-M1 processor developed by ARM for implementation in FPGAs. ARM Cortex-M1 is a soft processor that is fully implemented in the FPGA fabric. It has a three-stage pipeline that offers a good balance between low-power consumption and speed when implemented in an M1 ProASIC3L device. The processor runs the ARMv6-M instruction set, has a configurable nested interrupt controller, and can be implemented with or without the debug block. ARM Cortex-M1 is available for free from Actel for use in M1 ProASIC3L FPGAs.

The ARM-enabled devices have Actel ordering numbers that begin with M1 and do not support AES decryption.

Flash*Freeze Technology

The ProASIC3L devices offer Actel's proven Flash*Freeze technology, which allows instantaneous switching from an active state to a static state. ProASIC3L devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of ProASIC3L devices to support a wide range core voltage (1.2 V to 1.5 V) allows for an even greater reduction in power consumption, which enables low total system power.

When the ProASIC3L device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

The availability of low-power modes, combined with a reprogrammable, single-chip, single-voltage solution, make ProASIC3L devices suitable for low-power data transfer and manipulation in portable media, secure communications, radio applications as well as high performance portable, industrial, test, scientific, and medical applications.

Flash Advantages

Low Power

The ProASIC3L family of Actel flash-based FPGAs provide a low-power advantage, and when coupled with high performance, enables designers to make power-smart choices using a single-chip, reprogrammable, and live-at-power-up device.

ProASIC3L devices offer 40% dynamic power and 50% static power savings by reducing the core operating voltage to 1.2 V. In addition, the Power Driven Layout (PDL) feature in Libero® Integrated Design Environment (IDE) offers up to 30% additional power reduction. With Flash*Freeze technology, ProASIC3L is able to retain device SRAM and logic while dynamic power is reduced to a minimum, without the need to stop clock or power supplies. Combining these features provides a low-power, feature-rich and high-performance solution.

Security

Nonvolatile, flash-based ProASIC3L devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC3L devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

ProASIC3L devices utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in ProASIC3L devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. ProASIC3L devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC3L devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed device cannot be read back, although secure design verification is possible.

Security, built into the FPGA fabric, is an inherent component of the ProASIC3L family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The ProASIC3L family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. A ProASIC3L device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based ProASIC3L FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Live at Power-Up

The Actel flash-based ProASIC3L devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based ProASIC3L devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the ProASIC3L device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC3L devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based ProASIC3L devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC3L family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC3L family a cost-effective ASIC replacement solution, manipulation in portable media and secure communications, radio applications as well as high performance portable Industrial, test, scientific and medical applications.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of ProASIC3L flash-based FPGAs. Once it is programmed, the flash cell configuration element of ProASIC3L FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The ProASIC3L family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with 7 layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary ProASIC3L architecture provides granularity comparable to standard-cell ASICs. The ProASIC3L device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC3L core tile, as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable, allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of ProASIC3L devices via an IEEE 1532 JTAG interface.

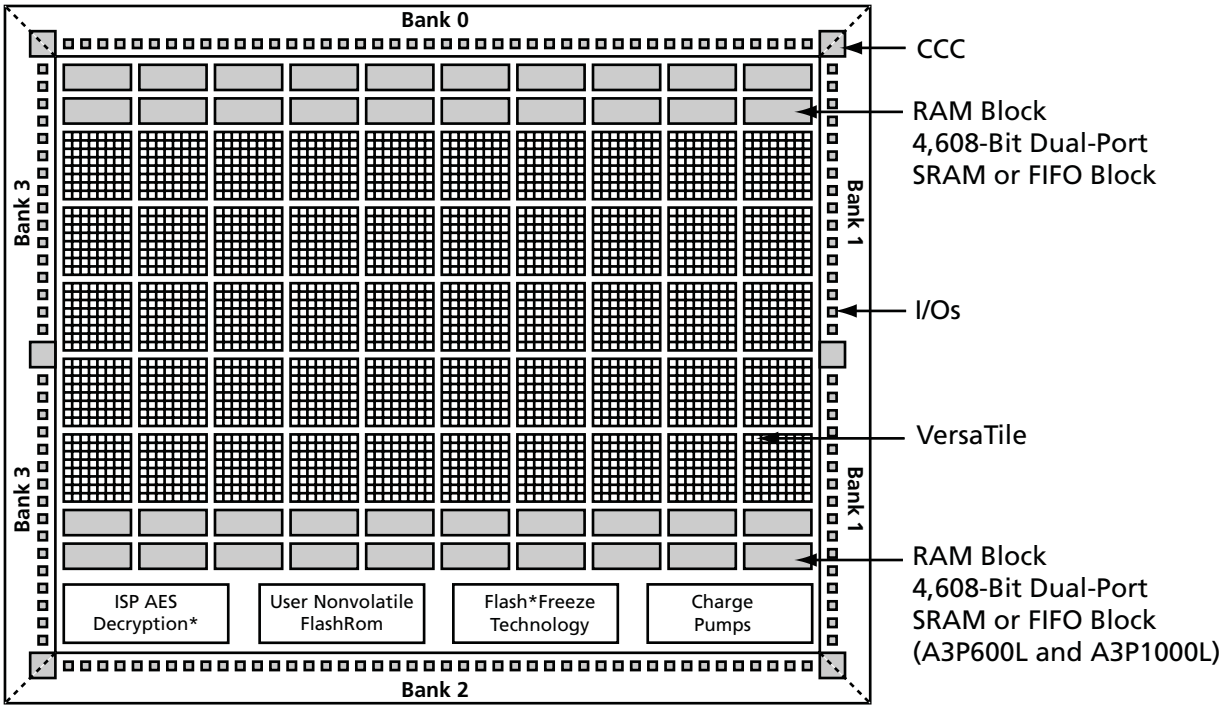


Figure 1-1 • **ProASIC3L Device Architecture Overview with Four I/O Banks (A3P250L, A3P600L, and A3P1000L)**

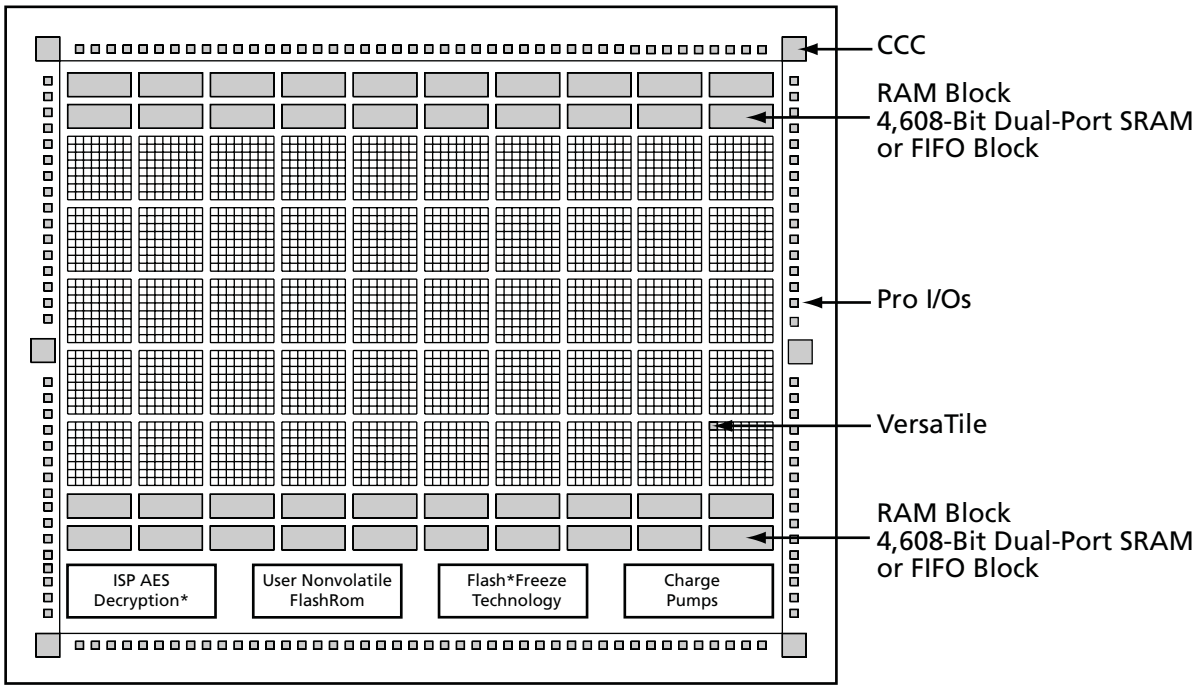


Figure 1-2 • **ProASIC3EL Device Architecture Overview**

Flash*Freeze Technology

The ProASIC3L devices offer Actel's proven Flash*Freeze technology, which enables designers to instantaneously shut off dynamic power consumption while retaining all SRAM and register information. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze (FF) pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption; clocks can still be driven or can be toggling without impact on power consumption; and the device retains all core registers, SRAM information, and states. I/O states are tristated during Flash*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL. Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The FF pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the FF pin as a regular I/O if Flash*Freeze mode usage is not planned, which is advantageous because of the inherent low-power static and dynamic capabilities of the ProASIC3L device. Refer to Figure 1-3 for an illustration of entering/exiting Flash*Freeze mode.

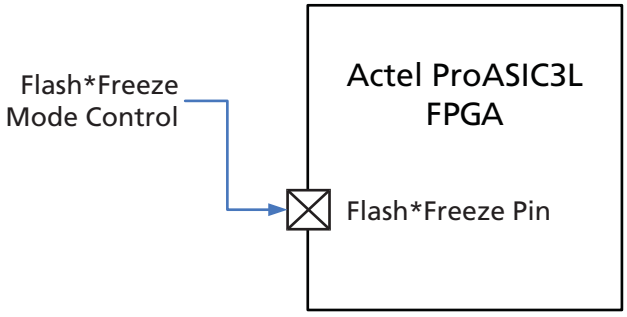


Figure 1-3 • **ProASIC3L Flash*Freeze Mode**

VersaTiles

The ProASIC3L core consists of VersaTiles, which have been enhanced beyond the ProASIC[PLUS]® core tiles. The ProASIC3L VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-4 for VersaTile configurations.

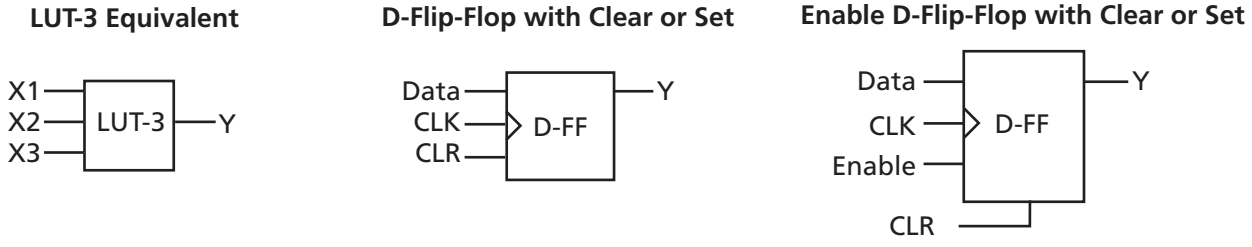


Figure 1-4 • **VersaTile Configurations**

User Nonvolatile FlashROM

Actel ProASIC3L devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet Protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3L IEEE 1532 JTAG programming interface.The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel ProASIC3L development software solutions, Libero IDE and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

ProASIC3L devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

ProASIC3L devices provide designers with flexible clock conditioning circuit (CCC) capabilities. Each member of the ProASIC3L family contains six CCCs. One CCC (center west side) has a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time is 300 µs
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / f_{OUT_CCC}

Global Clocking

ProASIC3L devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

The ProASIC3L family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V). ProASIC3L FPGAs support different I/O standards, including single-ended, differential, and voltage-referenced (ProASIC3EL only). The I/Os are organized into banks, with two, four, or eight (ProASIC3EL only) banks per device. The configuration of these banks determines the I/O standards supported. For ProASIC3EL, each I/O bank is subdivided into V_{REF} minibanks, which are used by voltage-referenced I/Os. V_{REF} minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common V_{REF} line. Therefore, if any I/O in a given V_{REF} minibank is configured as a V_{REF} pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-data-rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-data-Rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II).

ProASIC3L banks support LVPECL, LVDS, B-LVDS, and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Wide Range I/O Support

Actel ProASIC3L devices support JEDEC-defined wide range I/O operation. ProASIC3L devices support both the JESD8-B specification, covering 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Part Number and Revision Date

Part Number 51700100-001-4
Revised February 2009

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v1.3)	Page
v1.2 (February 2009)	The "I/Os Per Package [1]" table was revised to change the number of differential I/O pairs for A3PE3000L from 300 to 310.	II
	Table 2 · ProASIC3L FPGAs Package Sizes Dimensions is new.	II
v1.1 (July 2008)	The "Advanced and Pro (Professional) I/Os" section was revised to add two bullets regarding wide range power supply voltage support.	I
	3.0 V wide range was added to the list of supported voltages in the "I/Os with Advanced I/O Standards" section. The "Wide Range I/O Support" section is new.	1-7
v1.0 (April 2008)	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
51700100-001-1 (April 2008)	This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
51700100-001-0 (January 2008)	Reference to M1A3P250L was removed from Table 1 · ProASIC3 Low-Power Product Family, the "I/Os Per Package [1]" table, the "ProASIC3L Ordering Information" section, and the "Temperature Grade Offerings" table. The table note regarding M1A3P250L was removed from the "I/Os Per Package [1]" table.	I, II, III, IV

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advance," "Preliminary," and "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

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2 – ProASIC3L DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
V_{CC}	DC core supply voltage	–0.3 to 1.65	V
V_{JTAG}	JTAG DC voltage	–0.3 to 3.75	V
V_{PUMP}	Programming voltage	–0.3 to 3.75	V
V_{CCPLL}	Analog power supply (PLL)	–0.3 to 1.65	V
V_{CCI} and VMV [3]	DC I/O buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (V_{CCI} + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [2]	Storage temperature	–65 to +150	°C
T_J [2]	Junction temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *For flash programming and retention maximum limits, refer to Table 2-3 on page 2-2, and for recommended operating limits, refer to Table 2-2 on page 2-2.*
3. *VMV pins must be connected to the corresponding V_{CCI} pins. See Pin Descriptions for further information.*

Table 2-2 • Recommended Operating Conditions [1]

Symbol	Parameter		Commercial	Industrial	Units
T_A	Ambient temperature		0 to +70	–40 to +85	°C
T_J	Junction Temperature		0 to + 85	–40 to +100	°C
V_{CC} [2]	1.2 V–1.5 V wide range core voltage		1.14 to 1.575	1.14 to 1.575	V
V_{JTAG}	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
V_{PUMP} [3]	Programming voltage	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation [3]	0 to 3.45	0 to 3.45	V
V_{CCPLL} [6]	Analog power supply (PLL)	1.2 V–1.5 V wide range core voltage	1.14 to 1.575	1.14 to 1.575	V
V_{CCI} and VMV [5]	1.2 V DC supply voltage[4]		1.14 to 1.26	1.14 to 1.26	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V wide range DC supply voltage[7]		2.7 to 3.6	2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-13 on page 2-10. V_{CCI} should be at the same voltage within a given I/O bank.*
3. *V_{PUMP} can be left floating during normal operation (not programming mode).*
4. *For ProASIC®3L devices, $V_{CCI} \geq V_{CC}$.*
5. *VMV pins must be connected to the corresponding V_{CCI} pins. See Pin Descriptions for further information.*
6. *V_{CCPLL} pins should be tied to V_{CC} pins. See Pin Descriptions for further information.*
7. *3.3 V wide range is compliant to the JDEC8a specification and supports 3.0 V V_{CCI} operation.*

Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature[1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Table 2-4 • **Overshoot and Undershoot Limits [1]**

V_{CCI}	Average V_{CCI}–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at junction temperature at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table does not provide PCI overshoot/undershoot limits.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5.

There are five regions to consider during power-up.

ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. V_{CC} and V_{CCI} are above the minimum specified trip points (Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5).
2. $V_{CCI} > V_{CC} – 0.75$ V (typical)
3. Chip is in the operating mode.

V_{CCI} Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

V_{CC} Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

V_{CC} and V_{CCI} ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to V_{CCI}.
- JTAG supply, PLL power supplies, and charge pump V_{PUMP} supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Actel recommends using monotonic power supplies or voltage regulators to ensure proper powerup behavior. Power ramp-up should be monotonic at least until V_{CC} and V_{CCPLX} exceed brownout activation levels. The V_{CC} activation level is specified as 1.1 V worst-case (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or V_{CC} levels drop below the V_{CC} brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the *Power-Up/-Down Behavior of Low-Power Flash Devices* chapter of the handbook for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation.

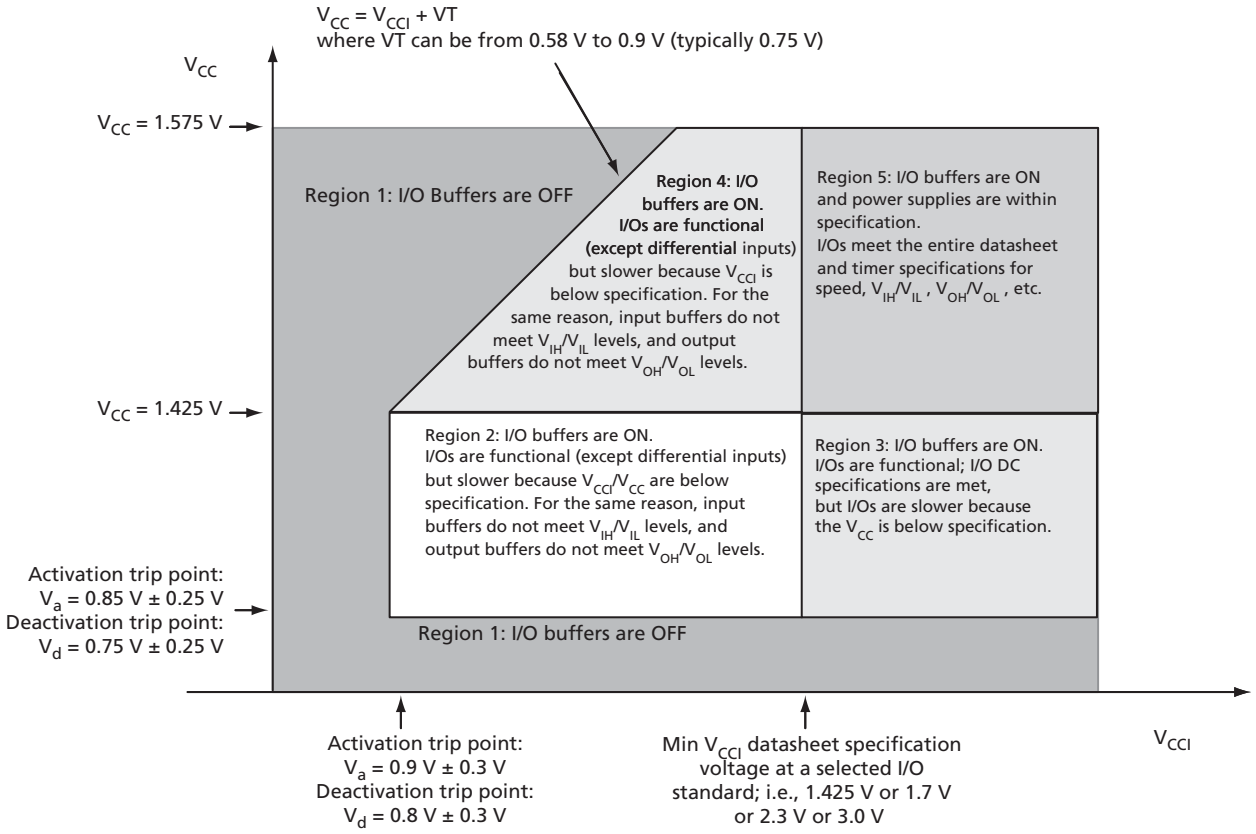


Figure 2-1 • **V5 Devices – I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels**

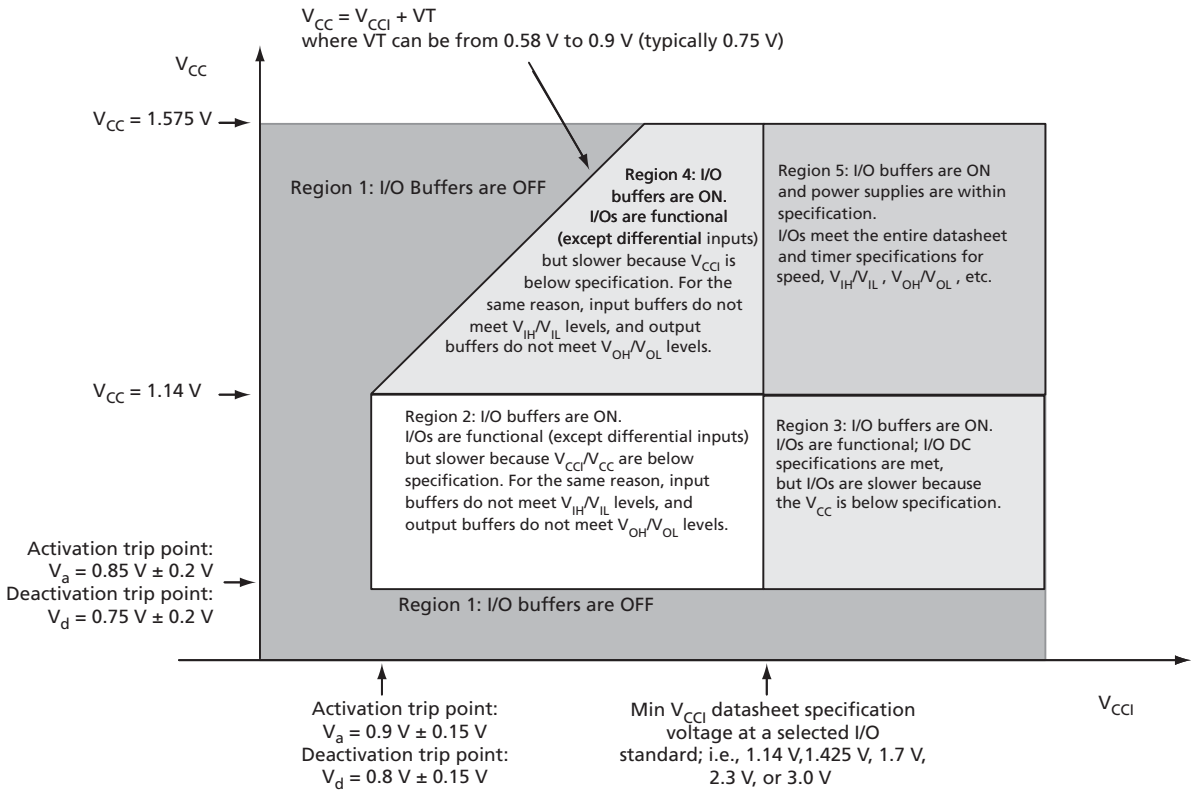


Figure 2-2 • **V2 Devices – I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in the Actel Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature.

EQ 2-1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A \qquad \textit{EQ 2-1}$$

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 100°C. EQ 2-2 shows a sample calculation of the absolute maximum power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{100\text{°C} - 70\text{°C}}{20.5\text{°C/W}} = 1.463\ \text{W} \qquad \textit{EQ 2-2}$$

Table 2-5 • **Package Thermal Resistivities**

Package Type	Device	Pin Count	θ_{jc}	θ_{ja}			Units
				Still Air	200 ft./min.	500 ft./min.	
Very Thin Quad Flat Pack (VQFP)	All devices	100	10.0	35.3	29.4	27.1	C/W
Plastic Quad Flat Pack (PQFP)	All devices	208	8.0	26.1	22.5	20.8	C/W
PQFP with embedded heatspreader	All devices	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	A3P250L	144	12.2	43.8	37.7	35.8	C/W
	A3P600L	144	8.3	35.8	30.2	28.3	C/W
	A3P1000L	144	6.3	31.6	26.2	24.2	C/W
	A3P250L	256	12.0	38.6	34.7	33.0	C/W
	A3P600L	256	8.5	32.0	27.5	25.8	C/W
	A3P1000L	256	6.6	28.1	24.4	22.7	C/W
	AGLE3000	324	TBD	TBD	TBD	TBD	C/W
	A3P600L	484	9.5	27.5	21.9	20.2	C/W
	A3P1000L	484	8.0	23.3	19.0	16.7	C/W
	A3PE3000L	484	4.7	20.6	15.7	14.0	C/W
	A3PE3000L	896	2.4	13.6	10.4	9.4	C/W

Temperature and Voltage Derating Factors

Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, V_{CC} = 1.14 V)

Array Voltage V_{CC} (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	110°C
1.14	0.90	0.94	0.96	1.00	1.01	1.03
1.2	0.87	0.90	0.92	0.96	0.97	0.99
1.26	0.83	0.86	0.88	0.92	0.93	0.85
1.3	0.81	0.84	0.86	0.90	0.91	0.93
1.35	0.78	0.81	0.83	0.87	0.88	0.89
1.4	0.75	0.78	0.80	0.83	0.84	0.86
1.425	0.74	0.77	0.78	0.82	0.83	0.85
1.5	0.70	0.72	0.74	0.77	0.79	0.80
1.575	0.67	0.70	0.72	0.75	0.76	0.77

Calculating Power Dissipation

Quiescent Supply Current

Table 2-7 • Quiescent Supply Current (I_{DD}) Characteristics, ProASIC3L Flash*Freeze Mode*

	Core Voltage	A3P250L	A3P600L	A3P1000L	A3PE3000L	Units
Typical (25°C)	1.2 V	0.33	0.55	0.88	2.75	mA
	1.5 V					mA

* *I_{DD} includes V_{CC}, V_{PUMP}, V_{CCI}, V_{JTAG}, and V_{CCPLL} currents. Values do not include I/O static contribution (P_{DC6} and P_{DC7}).*

Table 2-8 • Quiescent Supply Current (I_{DD}) Characteristics, ProASIC3L Sleep Mode (V_{CC} = 0 V)*

	Core Voltage	A3P250L	A3P600L	A3P1000L	A3PE3000L	Units
V_{CCI} / V_{JTAG} = 1.2 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.7	1.7	1.7	1.7	µA
V_{CCI} / V_{JTAG} = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	µA
V_{CCI} / V_{JTAG} = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	µA
V_{CCI} / V_{JTAG} = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	µA
V_{CCI} / V_{JTAG} = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	µA

* *I_{DD} includes V_{CC}, V_{PUMP}, and V_{CCPLL} currents. Values do not include I/O static contribution (P_{DC6} and P_{DC7}).*

Table 2-9 • Quiescent Supply Current (I_{DD}) Characteristics, Shutdown Mode (V_{CC}, V_{CCI} = 0 V)

	Core Voltage	A3PE3000L	Units
Typical (25°C)	1.2 V / 1.5 V	0	µA

* *I_{DD} includes V_{CC}, V_{PUMP}, V_{CCI}, V_{JTAG}, and V_{CCPLL} currents. Values do not include I/O static contribution (P_{DC6} and P_{DC7}).*

Table 2-10 • **Quiescent Supply Current (I_{DD}), No ProASIC3L Flash*Freeze Mode[1]**

	Core Voltage	A3P250L	A3P600L	A3P1000L	A3PE3000L	Units
I_{CCA} Current[2]						
Typical (25°C)	1.2 V	0.33	0.55	0.88	2.75	mA
	1.5 V					mA
I_{CCI} or I_{JTAG} Current[3, 4]						
V_{CCI} / V_{JTAG} = 1.2 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.7	1.7	1.7	1.7	µA
V_{CCI} / V_{JTAG} = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	µA
V_{CCI} / V_{JTAG} = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	µA
V_{CCI} / V_{JTAG} = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	µA
V_{CCI} / V_{JTAG} = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	µA

Notes:

1. *To calculate total device I_{DD}, multiply the number of banks used by I_{CCI} and add I_{CCA} contribution.*
2. *Includes V_{CC}, V_{CCPLL}, and V_{PUMP} currents.*
3. *Per V_{CCI} or V_{JTAG} bank.*
4. *Values do not include I/O static contribution (P_{DC6} and P_{DC7}).*

Power per I/O Pin

Table 2-11 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Pro I/O Banks**

	V_{CCI} (V)	Static Power P_{DC6} (mW)[1]	Dynamic Power P_{AC9} (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	16.34
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	–	24.49
2.5 V LVCMOS	2.5	–	4.71
2.5 V LVCMOS – Schmitt trigger	2.5	–	6.13
1.8 V LVCMOS	1.8	–	1.66
1.8 V LVCMOS – Schmitt trigger	1.8	–	1.78
1.5 V LVCMOS (JESD8-11)	1.5	–	1.01
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	0.97
1.2 V LVCMOS	1.2	–	0.60
1.2 V LVCMOS – Schmitt trigger	1.2	–	0.53
3.3 V PCI	3.3	–	17.76
3.3 V PCI – Schmitt trigger	3.3	–	19.10
3.3 V PCI-X	3.3	–	17.76
3.3 V PCI-X – Schmitt trigger	3.3	–	19.10
Voltage-Referenced			
3.3 V GTL	3.3	2.90	7.07
2.5 V GTL	2.5	2.13	3.62
3.3 V GTL+	3.3	2.81	2.97
2.5 V GTL+	2.5	2.57	2.55
HSTL (I)	1.5	0.17	0.85
HSTL (II)	1.5	0.17	0.85
SSTL2 (I)	2.5	1.38	3.30
SSTL2 (II)	2.5	1.38	3.30
SSTL3 (I)	3.3	3.21	8.08
SSTL3 (II)	3.3	3.21	8.08
Differential			
LVDS	2.5	2.26	0.95
LVPECL	3.3	5.71	1.62

Notes:

1. *P_{DC6} is the static power (where applicable) measured on V_{CCI}.*
2. *P_{AC9} is the total dynamic power measured on V_{CCI}.*

Table 2-12 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings[1] Applicable to Advanced I/O Banks

	V_{CCI} (V)	Static Power P_{DC6} (mW)[2]	Dynamic Power P_{AC10} (µW/MHz)[3]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.22
2.5 V LVCMOS	2.5	–	4.65
1.8 V LVCMOS	1.8	–	1.65
1.5 V LVCMOS (JESD8-11)	1.5	–	0.98
1.2 V LVCMOS	1.2	–	0.61
3.3 V PCI	3.3	–	17.64
3.3 V PCI-X	3.3	–	17.64
Differential			
LVDS	2.5	2.26	0.95
LVPECL	3.3	5.72	1.63

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC6} is the static power (where applicable) measured on V_{CCI}.*
3. *P_{AC10} is the total dynamic power measured on V_{CCI}.*

Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Standard Plus I/O Banks

	V_{CCI} (V)	Static Power P_{DC6} (mW)[1]	Dynamic Power P_{AC9} (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.23
2.5 V LVCMOS	2.5	–	4.66
1.8 V LVCMOS	1.8	–	1.64
1.5 V LVCMOS (JESD8-11)	1.5	–	0.99
1.2 V LVCMOS	1.2	–	0.58
3.3 V PCI	3.3	–	17.64
3.3 V PCI-X	3.3	–	17.64

Notes:

1. *P_{DC6} is the static power (where applicable) measured on V_{CCI}.*
2. *P_{AC9} is the total dynamic power measured on V_{CCI}.*

Table 2-14 • **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Pro I/Os**

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC7} (mW)[2]	Dynamic Power P_{AC10} (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL/LVCMOS	5	3.3	–	148.00
2.5 V LVCMOS	5	2.5	–	83.23
1.8 V LVCMOS	5	1.8	–	54.58
1.5 V LVCMOS (JESD8-11)	5	1.5	–	37.05
1.2 V LVCMOS	5	1.2	–	17.94
3.3 V PCI	10	3.3	–	204.61
3.3 V PCI-X	10	3.3	–	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	–	24.08
2.5 V GTL	10	2.5	–	13.52
3.3 V GTL+	10	3.3	–	24.10
2.5 V GTL+	10	2.5	–	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
Differential				
LVDS	–	2.5	7.70	89.62
LVPECL	–	3.3	19.42	168.02

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC7} is the static power (where applicable) measured on V_{CCI}.*
3. *P_{AC10} is the total dynamic power measured on V_{CCI}.*

Table 2-15 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Advanced I/O Banks

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC7} (mW)[2]	Dynamic Power P_{AC10} (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	–	141.97
2.5 V LVCMOS	5	2.5	–	79.98
1.8 V LVCMOS	5	1.8	–	52.26
1.5 V LVCMOS (JESD8-11)	5	1.5	–	35.62
1.2 V LVCMOS	5	1.2	–	21.29
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	89.71
LVPECL	–	3.3	19.54	167.54

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC7} is the static power (where applicable) measured on V_{CCI}.*
3. *P_{AC10} is the total dynamic power measured on V_{CCI}.*

Table 2-16 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1] Applicable to Standard Plus I/O Banks

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC7} (mW)[2]	Dynamic Power P_{AC10} (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	–	125.97
2.5 V LVCMOS	5	2.5	–	70.82
1.8 V LVCMOS	5	1.8	–	36.39
1.5 V LVCMOS (JESD8-11)	5	1.5	–	25.34
1.2 V LVCMOS	5	1.2	–	16.24
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC7} is the static power (where applicable) measured on V_{CCI}.*
3. *P_{AC10} is the total dynamic power measured on V_{CCI}.*

Power Consumption of Various Internal Resources

Table 2-17 • **Different Components Contributing to Dynamic Power Consumption in ProASIC3L Devices at 1.2 V V_{CC}**

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)			
		A3PE3000L	A3P1000L	A3P600L	A3P250L
P_{AC1}	Clock contribution of a Global Rib	12.61	9.28	8.19	7.07
P_{AC2}	Clock contribution of a Global Spine	2.66	1.59	1.19	1.01
P_{AC3}	Clock contribution of a VersaTile row	0.56	0.52		
P_{AC4}	Clock contribution of a VersaTile used as a sequential module	0.07			
P_{AC5}	First contribution of a VersaTile used as a sequential module	0.05			
P_{AC6}	Second contribution of a VersaTile used as a sequential module	0.19			
P_{AC7}	Contribution of a VersaTile used as a combinatorial Module	0.11			
P_{AC8}	Average contribution of a routing net	0.45			
P_{AC9}	Contribution of an I/O input pin (standard-dependent)	See Table 2-11 on page 2-9. through Table 2-13 on page 2-10.			
P_{AC10}	Contribution of an I/O output pin (standard-dependent)	See Table 2-14 on page 2-11 through Table 2-16 on page 2-12.			
P_{AC11}	Average contribution of a RAM block during a read operation	25.00			
P_{AC12}	Average contribution of a RAM block during a write operation	30.00			
P_{AC13}	Dynamic contribution for PLL	1.74			

* *For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or SmartPower tool in Libero IDE.*

Table 2-18 • Different Components Contributing to Dynamic Power Consumption in ProASIC3L Devices at 1.5 V V_{CC}

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)			
		A3PE3000L	A3P1000L	A3P600L	A3P250L
P_{AC1}	Clock contribution of a Global Rib	19.7	14.50	12.80	11.00
P_{AC2}	Clock contribution of a Global Spine	4.16	2.48	1.85	1.58
P_{AC3}	Clock contribution of a VersaTile row	0.88	0.81		
P_{AC4}	Clock contribution of a VersaTile used as a sequential module	0.12			
P_{AC5}	First contribution of a VersaTile used as a sequential module	0.07			
P_{AC6}	Second contribution of a VersaTile used as a sequential module	0.29			
P_{AC7}	Contribution of a VersaTile used as a combinatorial Module	0.29			
P_{AC8}	Average contribution of a routing net	0.70			
P_{AC9}	Contribution of an I/O input pin (standard-dependent)	See Table 2-11 on page 2-9. through Table 2-13 on page 2-10.			
P_{AC10}	Contribution of an I/O output pin (standard-dependent)	See Table 2-14 on page 2-11 through Table 2-16 on page 2-12.			
P_{AC11}	Average contribution of a RAM block during a read operation	25.00			
P_{AC12}	Average contribution of a RAM block during a write operation	30.00			
P_{AC13}	Dynamic contribution for PLL	2.60			

* *For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or SmartPower tool in Libero IDE.*

Table 2-19 • Different Components Contributing to the Static Power Consumption in ProASIC3L Devices

Parameter	Definition	Device Specific Dynamic Power (µW)			
		A3PE3000L	A3P1000L	A3P600L	A3P250L
P_{DC1}	Array static power in Active mode	See Table 2-10 on page 2-8.			
P_{DC2}	Array static power in Static (Idle) mode	See Table 2-8 on page 2-7.			
P_{DC3}	Array static power in Flash*Freeze mode	See Table 2-7 on page 2-7.			
P_{DC4}	Static PLL contribution at 1.2 V core (operating mode only)	1.42 mW			
	Static PLL contribution at 1.5 V core (operating mode only)	2.55 mW			
P_{DC5}	Bank quiescent power (V_{CCI}-dependent)	See Table 2-7 on page 2-7, Table 2-8 on page 2-7, Table 2-10 on page 2-8.			
P_{DC6}	I/O input pin static power (standard-dependent)	See Table 2-11 on page 2-9 through Table 2-13 on page 2-10.			
P_{DC7}	I/O output pin static power (standard-dependent)	See Table 2-14 on page 2-11 through Table 2-16 on page 2-12.			

* *For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or SmartPower tool in Libero IDE.*

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Actel Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-20 on page 2-17.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-21 on page 2-17.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-21 on page 2-17. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

$P_{STAT} = (P_{DC1}$ or P_{DC2} or $P_{DC3}) + N_{BANKS} * P_{DC5} + N_{INPUTS} * P_{DC6} + N_{OUTPUTS} * P_{DC7}$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{BANKS} is the number of I/O banks powered in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in Table 2-20 on page 2-17.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in Table 2-20 on page 2-17.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

P_{AC1}, P_{AC2}, P_{AC3}, and P_{AC4} are device-dependent.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-20 on page 2-17.

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-20 on page 2-17.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-20 on page 2-17.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-20 on page 2-17.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-20 on page 2-17.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-21 on page 2-17.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-21 on page 2-17.

PLL Contribution—P_{PLL}

$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[1]

1. *If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.*

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-20 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-21 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

User I/O Characteristics

Timing Model

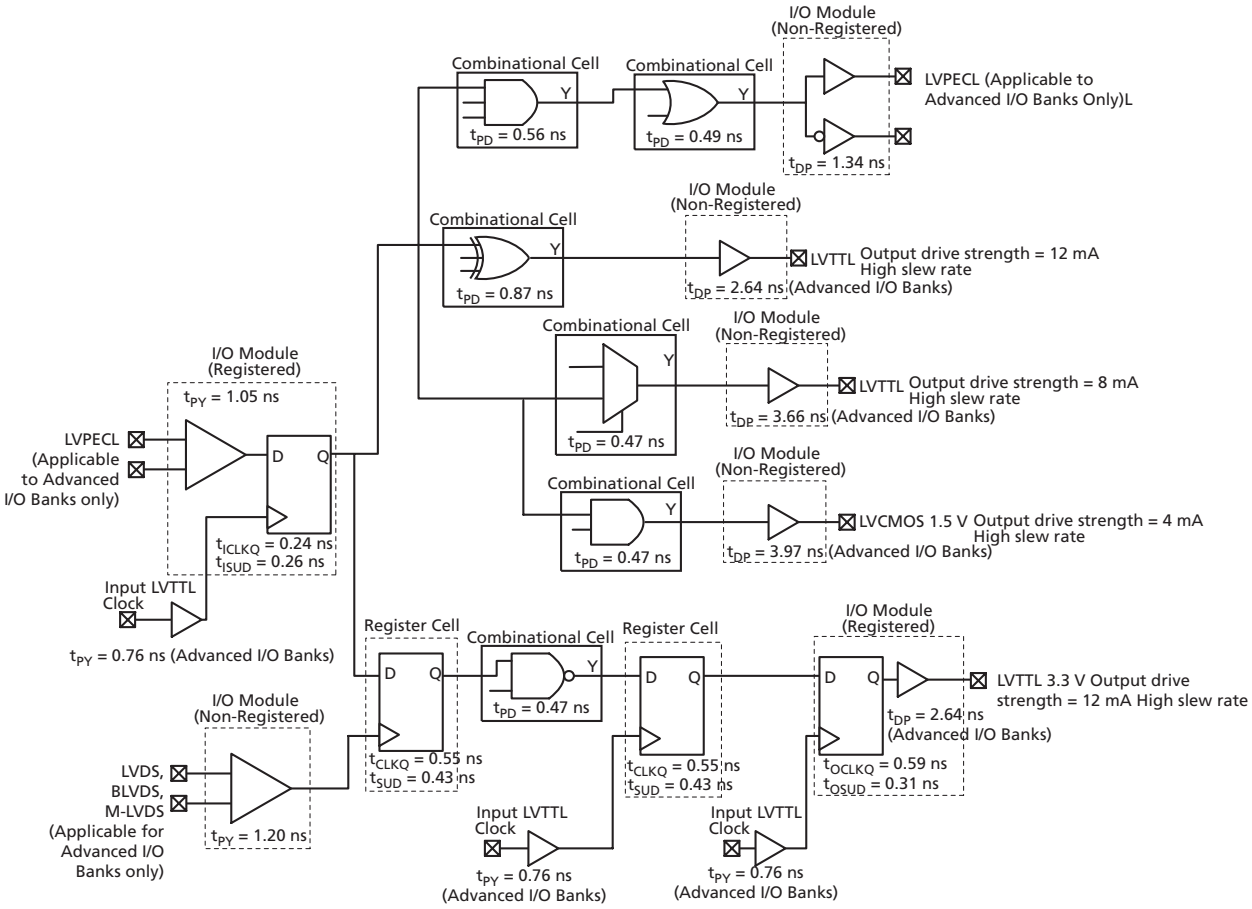


Figure 2-3 • **Timing Model**
Operating Conditions: –1 Speed, Commercial Temperature Range (T_J = 70°C), Worst-Case V_{CC} = 1.14 V

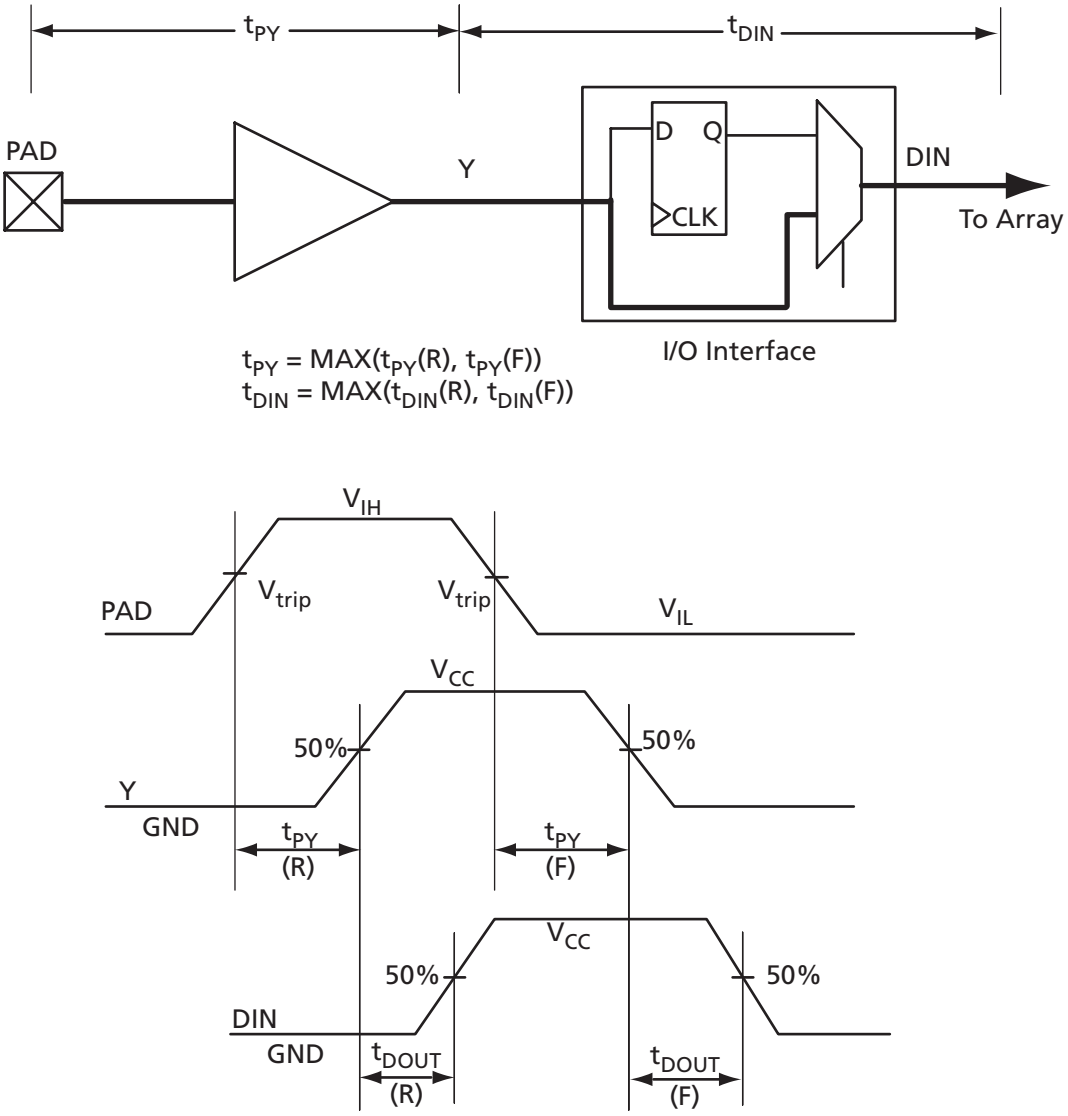


Figure 2-4 • **Input Buffer Timing Model and Delays (example)**

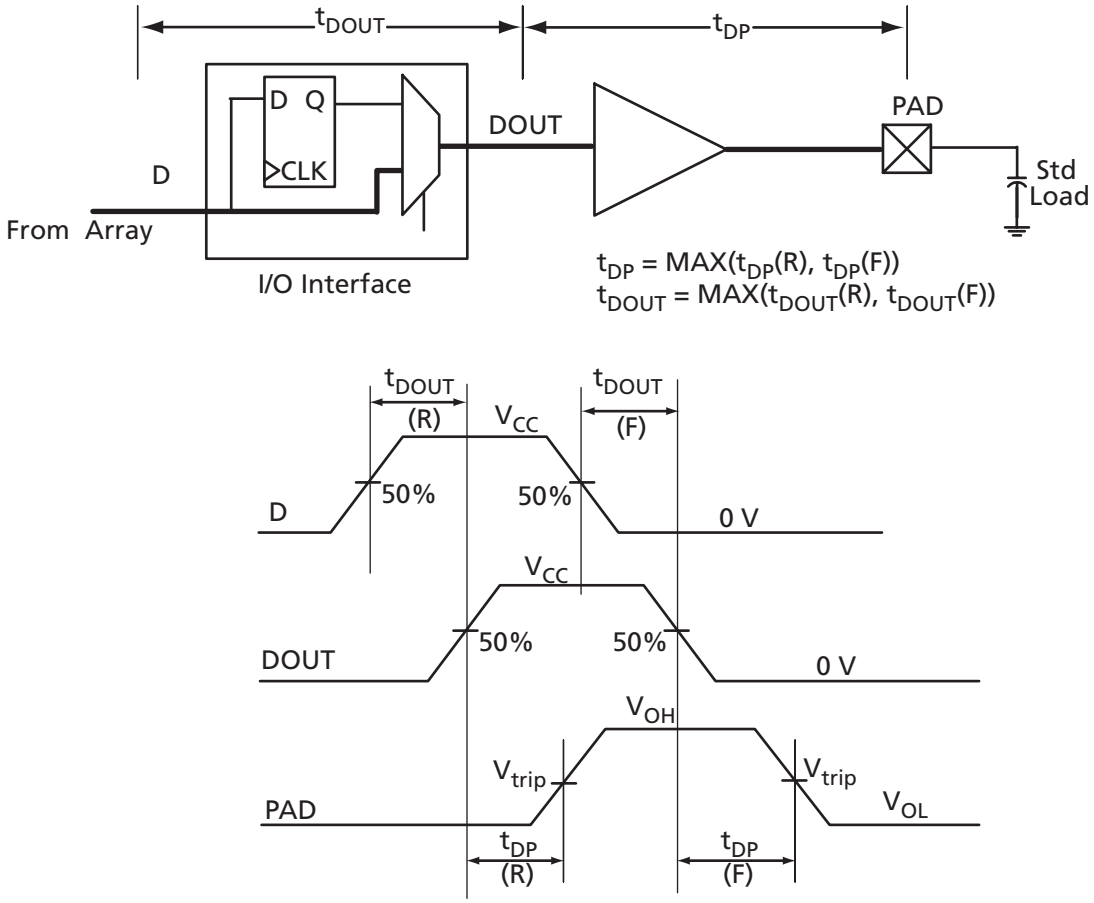


Figure 2-5 • **Output Buffer Model and Delays (example)**

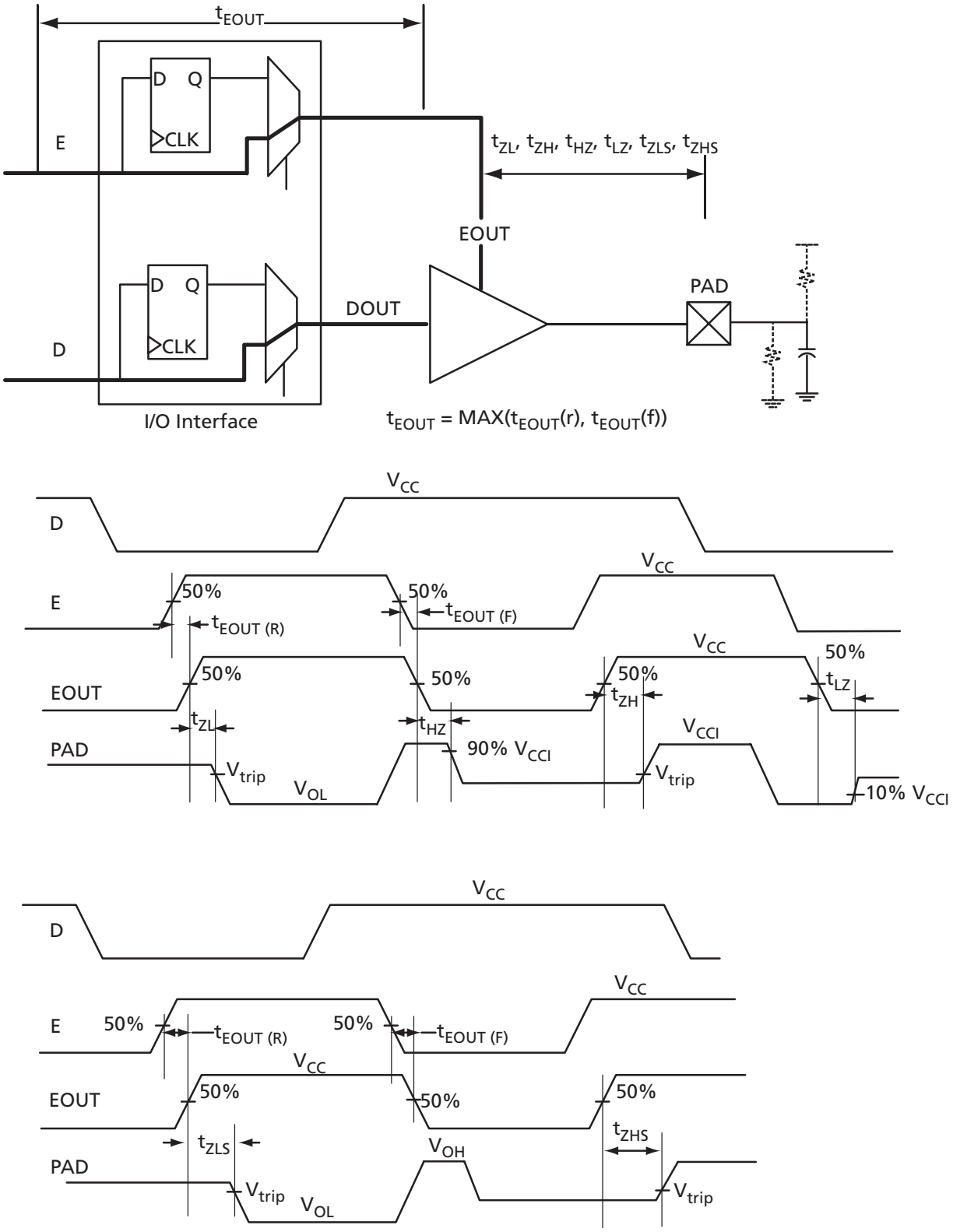


Figure 2-6 • **Tristate Output Buffer Timing Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-22 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Pro I/O

I/O Standard	Drive Strength	Slew Rate	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}[1]	I_{OH}[1]
			Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range	Any[2]	High	–0.3	0.8	2	3.6	0.2	V_{CCI} – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12
1.2 V LVCMOS	2 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.26	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2
3.3 V PCI	Per PCI Specification									
3.3 V PCI-X	Per PCI-X Specification									
3.3 V GTL	25 mA[3]	High	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25
2.5 V GTL	25 mA[3]	High	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	2.7	0.4	–	25	25
3.3 V GTL+	35 mA	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	51	51
2.5 V GTL+	33 mA	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	2.7	0.6	–	40	40
HSTL (I)	8 mA	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575	0.4	V_{CCI} – 0.4	8	8
HSTL (II)	15 mA[3]	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575	0.4	V_{CCI} – 0.4	15	15
SSTL2 (I)	15 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	2.7	0.54	V_{CCI} – 0.62	15	15
SSTL2 (II)	18 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	2.7	0.35	V_{CCI} – 0.43	18	18
SSTL3 (I)	14 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCI} – 1.1	14	14
SSTL3 (II)	21 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCI} – 0.9	21	21

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specificied in the JDEC8a specification.*
3. *Output drive strength is below JEDEC specification.*
4. *Output slew rate can be extracted using the IBIS Models.*

Table 2-23 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Slew Rate	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}[1]	I_{OH}[1]
			Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range	Any[3]	High	–0.3	0.8	2	3.6	0.2	V_{CCI} – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12
1.2 V LVCMOS	2 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.26	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Output slew rate can be extracted using the IBIS Models*
3. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specificied in the JDEC8a specification.*

Table 2-24 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Standard Plus I/O Banks

I/O Standard	Drive Strength	Slew Rate	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}[1]	I_{OH}[1]
			Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range	Any[3]	High	–0.3	0.8	2	3.6	0.2	V_{CCI} – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	8	8
1.5 V LVCMOS	4 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4
1.2 V LVCMOS	2 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.26	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Output slew rate can be extracted using the IBIS Models.*
3. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specificied in the JDEC8a specification.*

Table 2-25 • **Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions**

	Commercial[1]		Industrial[2]	
	I_{IL}	I_{IH}	I_{IL}	I_{IH}
DC I/O Standard	**µA**	**µA**	**µA**	**µA**
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCMOS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
1.2 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15
3.3 V GTL	10	10	15	15
2.5 V GTL	10	10	15	15
3.3 V GTL+	10	10	15	15
2.5 V GTL+	10	10	15	15
HSTL (I)	10	10	15	15
HSTL (II)	10	10	15	15
SSTL2 (I)	10	10	15	15
SSTL2 (II)	10	10	15	15
SSTL3 (I)	10	10	15	15
SSTL3 (II)	10	10	15	15

Notes:

1. *Commercial range (0°C < T_A < 70°C)*
2. *Industrial range (–40°C < T_A < 85°C)*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-26 • Summary of AC Memory Points

Standard	Input Reference Voltage (V_{REF_TYP})	Board Termination Voltage (V_{TT_REF})	Measuring Trip Point (V_{trip})
3.3 V LVTTL / 3.3 V LVCMOS	–	–	1.4 V
3.3 V LVCMOS Wide Range	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
1.2 V LVCMOS	–	–	0.6V
3.3 V PCI	–	–	0.285 * V_{CCI} (RR)
			0.615 * V_{CCI} (FF))
3.3 V PCI-X	–	–	0.285 * V_{CCI} (RR)
			0.615 * V_{CCI} (FF)
3.3 V GTL	0.8 V	1.2 V	V_{REF}
2.5 V GTL	0.8 V	1.2 V	V_{REF}
3.3 V GTL+	1.0 V	1.5 V	V_{REF}
2.5 V GTL+	1.0 V	1.5 V	V_{REF}
HSTL (I)	0.75 V	0.75 V	V_{REF}
HSTL (II)	0.75 V	0.75 V	V_{REF}
SSTL2 (I)	1.25 V	1.25 V	V_{REF}
SSTL2 (II)	1.25 V	1.25 V	V_{REF}
SSTL3 (I)	1.5 V	1.485 V	V_{REF}
SSTL3 (II)	1.5 V	1.485 V	V_{REF}
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

Table 2-27 • I/O AC Parameter Definitions

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—HIGH to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to HIGH
t_{LZ}	Enable to Pad delay through the Output Buffer—LOW to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to LOW
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW

1.5 V DC Core Voltage

Table 2-28 • Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425V, Worst Case V_{CCI} Pro I/O Banks

Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	5	–	0.50	1.89	0.03	1.34	1.85	0.33	1.93	1.42	2.51	2.77	3.64	3.13	ns
2.5 V LVCMOS	12 mA	High	5	–	0.50	1.92	0.03	1.58	1.97	0.33	1.96	1.59	2.58	2.68	3.67	3.30	ns
1.8 V LVCMOS	12 mA	High	5	–	0.50	2.14	0.03	1.53	2.17	0.33	2.18	1.76	2.86	3.24	3.89	3.47	ns
1.5 V LVCMOS	12 mA	High	5	–	0.50	2.46	0.03	1.69	2.36	0.33	2.51	2.04	3.03	3.35	4.22	3.75	ns
3.3 V PCI	Per PCI spec.	High	5	–	0.50	2.15	0.03	2.10	2.84	0.33	2.19	1.53	2.51	2.77	3.90	3.24	ns
3.3 V PCI-X	Per PCI-X spec.	High	10	25	0.50	2.15	0.03	2.10	2.84	0.33	2.19	1.53	2.51	2.77	3.90	3.24	ns
3.3 V GTL	25 mA	High	10	25	0.50	1.59	0.03	1.80	–	0.33	1.56	1.59	–	–	3.27	3.30	ns
2.5 V GTL	25 mA	High	10	25	0.50	1.63	0.03	1.75	–	0.33	1.66	1.63	–	–	3.37	3.34	ns
3.3 V GTL+	35 mA	High	10	25	0.50	1.57	0.03	1.80	–	0.33	1.60	1.57	–	–	3.31	3.29	ns
2.5 V GTL+	33 mA	High	10	25	0.50	1.69	0.03	1.75	–	0.33	1.72	1.61	–	–	3.43	3.32	ns
HSTL (I)	8 mA	High	20	25	0.50	2.43	0.03	2.12	–	0.33	2.48	2.41	–	–	4.19	4.12	ns
HSTL (II)	15 mA	High	20	50	0.50	2.32	0.03	2.12	–	0.33	2.36	2.08	–	–	4.07	3.79	ns
SSTL2 (I)	15 mA	High	30	25	0.50	1.63	0.03	1.61	–	0.33	1.66	1.41	–	–	1.66	1.41	ns
SSTL2 (II)	18 mA	High	30	50	0.50	1.66	0.03	1.61	–	0.33	1.69	1.36	–	–	1.69	1.36	ns
SSTL3 (I)	14 mA	High	30	25	0.50	1.77	0.03	1.54	–	0.33	1.80	1.41	–	–	1.80	1.41	ns
SSTL3 (II)	21 mA	High	30	50	0.50	1.58	0.03	1.54	–	0.33	1.61	1.28	–	–	1.61	1.28	ns
LVDS	24 mA	High	-	-	0.50	1.40	0.03	1.85	–	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	-	-	0.50	1.40	0.03	1.67	–	–	–	–	–	–	–	–	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-75 for connectivity. This resistor is not required during normal operation.*

Table 2-29 • Summary of I/O Timing Characteristics—Software Default Settings
–1 Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI}
Advanced I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	5pF	–	0.46	1.83	0.03	0.78	0.33	1.87	1.39	2.46	2.74	3.58	3.10	ns
2.5 V LVCMOS	12 mA	High	5 pF	–	0.46	1.85	0.03	1.00	0.33	1.88	1.55	2.53	2.63	3.59	3.26	ns
1.8 V LVCMOS	12 mA	High	5 pF	–	0.46	2.04	0.03	0.93	0.33	2.08	1.73	2.83	3.12	3.79	3.45	ns
1.5 V LVCMOS	12 mA	High	5 pF	–	0.46	2.33	0.03	1.10	0.33	2.37	2.01	3.02	3.22	4.08	3.72	ns
3.3 V PCI	Per PCI spec.	High	5 pF	25 [2]	0.46	2.05	0.03	0.66	0.33	2.09	1.49	2.46	2.74	3.80	3.21	ns
3.3 V PCI-X	Per PCI-X spec.	High	10 pF	25 [2]	0.46	2.05	0.03	0.64	0.33	2.09	1.49	2.46	2.74	3.80	3.21	ns
LVDS	24 mA	High	–	–	0.46	1.40	0.03	1.23	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL	24 mA	High	–	–	0.46	1.38	0.03	1.08	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-75 for connectivity. This resistor is not required during normal operation.*

Table 2-30 • Summary of I/O Timing Characteristics—Software Default Settings
–1 Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V
Standard Plus I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	5pF	–	0.46	1.56	0.03	0.77	0.33	1.59	1.20	2.14	2.47	3.30	2.91	ns
2.5 V LVCMOS	12 mA	High	5pF	–	0.46	1.59	0.03	0.99	0.33	1.61	1.32	2.16	2.38	3.33	3.03	ns
1.8 V LVCMOS	8 mA	High	5pF	–	0.46	1.59	0.03	0.99	0.33	1.61	1.32	2.16	2.38	3.33	3.03	ns
1.5 V LVCMOS	4 mA	High	5pF	–	0.46	2.15	0.03	1.09	0.33	2.19	1.82	2.32	2.40	3.90	3.53	ns
3.3 V PCI	Per PCI spec.	High	10 pF	25 [2]	0.46	1.77	0.03	0.65	0.33	1.80	1.31	2.14	2.47	3.51	3.02	ns
3.3 V PCI-X	Per PCI-X spec.	High	10 pF	25 [2]	0.46	1.77	0.03	0.64	0.33	1.80	1.31	2.14	2.47	3.51	3.02	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-75 for connectivity. This resistor is not required during normal operation.*

1.2 V DC Core Voltage

Table 2-31 • Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.14 V, Worst Case V_{CCI} Pro I/O Banks

Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	5	–	0.66	1.89	0.04	1.34	1.85	0.43	1.93	1.42	2.51	2.77	3.64	3.13	ns
2.5 V LVCMOS	12 mA	High	5	–	0.66	1.92	0.04	1.58	1.97	0.43	1.96	1.59	2.58	2.68	3.67	3.30	ns
1.8 V LVCMOS	12 mA	High	5	–	0.66	2.14	0.04	1.53	2.17	0.43	2.18	1.76	2.86	3.24	3.89	3.47	ns
1.5 V LVCMOS	12 mA	High	5	–	0.66	2.46	0.04	1.69	2.36	0.43	2.51	2.04	3.03	3.35	4.22	3.75	ns
1.2 V LVCMOS	2 mA	High	5	–	0.66	4.12	0.04	2.02	2.99	0.43	3.83	3.37	4.06	3.84	5.48	5.02	ns
3.3 V PCI	Per PCI spec.	High	10	–	0.66	2.15	0.04	2.10	2.84	0.43	2.19	1.53	2.51	2.77	3.90	3.24	ns
3.3 V PCI-X	Per PCI-X spec.	High	10	25	0.66	2.15	0.04	2.10	2.84	0.43	2.19	1.53	2.51	2.77	3.90	3.24	ns
3.3 V GTL	25 mA	High	10	25	0.66	1.59	0.04	1.80	–	0.43	1.56	1.59	–	–	3.27	3.30	ns
2.5 V GTL	25 mA	High	10	25	0.66	1.63	0.04	1.75	–	0.43	1.66	1.63	–	–	3.37	3.34	ns
3.3 V GTL+	35 mA	High	10	25	0.66	1.57	0.04	1.80	–	0.43	1.60	1.57	–	–	3.31	3.29	ns
2.5 V GTL+	33 mA	High	10	25	0.66	1.69	0.04	1.75	–	0.43	1.72	1.61	–	–	3.43	3.32	ns
HSTL (I)	8 mA	High	20	25	0.66	2.43	0.04	2.12	–	0.43	2.48	2.41	–	–	4.19	4.12	ns
HSTL (II)	15 mA	High	20	50	0.66	2.32	0.04	2.12	–	0.43	2.36	2.08	–	–	4.07	3.79	ns
SSTL2 (I)	15 mA	High	30	25	0.66	1.63	0.04	1.61	–	0.43	1.66	1.41	–	–	1.66	1.41	ns
SSTL2 (II)	18 mA	High	30	50	0.66	1.66	0.04	1.61	–	0.43	1.69	1.36	–	–	1.69	1.36	ns
SSTL3 (I)	14 mA	High	30	25	0.66	1.77	0.04	1.54	–	0.43	1.80	1.41	–	–	1.80	1.41	ns
SSTL3 (II)	21 mA	High	30	50	0.66	1.58	0.04	1.54	–	0.43	1.61	1.28	–	–	1.61	1.28	ns
LVDS	24 mA	High	-	-	0.66	1.43	0.04	1.85	–	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	-	-	0.66	1.37	0.04	1.67	–	–	–	–	–	–	–	–	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-75 for connectivity. This resistor is not required during normal operation.*

Table 2-32 • Summary of I/O Timing Characteristics—Software Default Settings
–1 Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.14 V, Worst Case V_{CCI}
Advanced I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	5pF	–	0.60	1.83	0.04	0.78	0.43	1.87	1.39	2.46	2.74	3.58	3.10	ns
2.5 V LVCMOS	12 mA	High	5 pF	–	0.60	1.85	0.04	1.00	0.43	1.88	1.55	2.53	2.63	3.59	3.26	ns
1.8 V LVCMOS	12 mA	High	5 pF	–	0.60	2.04	0.04	0.93	0.43	2.08	1.73	2.83	3.12	3.79	3.45	ns
1.5 V LVCMOS	12 mA	High	5 pF	–	0.60	2.33	0.04	1.10	0.43	2.37	2.01	3.02	3.22	4.08	3.72	ns
1.2 V LVCMOS	2 mA	High	5pF	–	0.60	3.17	0.04	1.55	0.43	2.11	1.76	2.38	2.46	3.76	3.41	ns
3.3 V PCI	Per PCI spec.	High	10 pF	25 [2]	0.60	2.05	0.04	0.66	0.43	2.09	1.49	2.46	2.74	3.80	3.21	ns
3.3 V PCI-X	Per PCI-X spec.	High	10 pF	25 [2]	0.60	2.05	0.04	0.64	0.43	2.09	1.49	2.46	2.74	3.80	3.21	ns
LVDS	24 mA	High	–	–	0.60	1.40	0.04	1.23	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL	24 mA	High	–	–	0.60	1.38	0.04	1.08	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-75 for connectivity. This resistor is not required during normal operation.*

Table 2-33 • **Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.14 V, Worst Case V_{CCI} = 3.0 V Standard Plus I/O Banks**

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	5pF	–	0.60	1.56	0.04	0.77	0.43	1.59	1.20	2.14	2.47	3.30	2.91	ns
2.5 V LVCMOS	12 mA	High	5pF	–	0.60	1.59	0.04	0.99	0.43	1.61	1.32	2.16	2.38	3.33	3.03	ns
1.8 V LVCMOS	8 mA	High	5pF	–	0.60	1.59	0.04	0.99	0.43	1.61	1.32	2.16	2.38	3.33	3.03	ns
1.5 V LVCMOS	4 mA	High	5pF	–	0.60	2.15	0.04	1.09	0.43	2.19	1.82	2.32	2.40	3.90	3.53	ns
1.2 V LVCMOS	2 mA	High	5pF	–	0.60	3.54	0.04	1.56	0.43	2.37	2.11	3.60	3.87	4.02	3.76	ns
3.3 V PCI	Per PCI spec.	High	10 pF	25 [2]	0.60	1.77	0.04	0.65	0.43	1.80	1.31	2.14	2.47	3.51	3.02	ns
3.3 V PCI-X	Per PCI-X spec.	High	10 pF	25 [2]	0.60	1.77	0.04	0.64	0.43	1.80	1.31	2.14	2.47	3.51	3.02	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-75 for connectivity. This resistor is not required during normal operation.*

Detailed I/O DC Characteristics

Table 2-34 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	V_{IN} = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	V_{IN} = 0, f = 1.0 MHz		8	pF

Table 2-35 • **I/O Output Buffer Maximum Resistances[1] Applicable to Pro I/Os**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω) [2]	$R_{PULL\text{-}UP}$ (Ω) [3]
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
1.2 V LVCMOS	2 mA	TBD	TBD
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	25 mA	11	–
2.5 V GTL	25 mA	14	–
3.3 V GTL+	35 mA	12	–
2.5 V GTL+	33 mA	15	–
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA	25	25
SSTL2 (I)	15 mA	27	31
SSTL2 (II)	18 mA	13	15
SSTL3 (I)	14 mA	44	69
SSTL3 (II)	21 mA	18	32

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-36 • **I/O Output Buffer Maximum Resistances[1] Applicable to Advanced I/O Banks**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω) [2]	$R_{PULL\text{-}UP}$ (Ω) [3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
1.8 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
1.2 V LVCMOS	2 mA	TBD	TBD
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-37 • I/O Output Buffer Maximum Resistances[1]
Applicable to Standard Plus I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω) [2]	$R_{PULL\text{-}UP}$ (Ω) [3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
1.2 V LVCMOS	2 mA	TBD	TBD
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-38 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	$R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω)	
V_{CCI}	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k
1.2 V LVCMOS	TBD	TBD	TBD	TBD

Notes:

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (V_{OLspec}) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$

Table 2-39 • I/O Short Currents I_{OSH}/I_{OSL} Applicable to Pro I/Os

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2 mA	TBD	TBD
3.3 V PCI/PCIX	Per PCI/PCI-X Specification	Per PCI Curves	
3.3 V GTL	25 mA	268	181
2.5 V GTL	25 mA	169	124
3.3 V GTL+	35 mA	268	181
2.5 V GTL+	33 mA	169	124
HSTL (I)	8 mA	32	39
HSTL (II)	15 mA	66	55
SSTL2 (I)	15 mA	83	87
SSTL2 (II)	18 mA	169	124
SSTL3 (I)	14 mA	51	54

* T_J = 100°C

Table 2-40 • I/O Short Currents I_{OSH}/I_{OSL} Applicable to Advanced I/O Banks

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2 mA	TBD	TBD
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

* T_J = 100°C

Table 2-41 • I/O Short Currents I_{OSH}/I_{OSL} Applicable to Standard Plus I/O Banks

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	103	109
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	35	44
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
1.2 V LVCMOS	2 mA	TBD	TBD
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

* T_J = 100°C

Table 2-42 • Schmitt Trigger Input Hysteresis, Hysteresis Voltage Value (Typ) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV
1.2 V LVCMOS (Schmitt trigger mode)	40 mV

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-43 • Duration of Short Circuit Event before Failure

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months

Table 2-44 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/B-LVDS/ M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

* *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. Furthermore, all LVCMOS 3.3 V software macros comply with LVCMOS 3.3 V wide range as specified in the JESD8a specification.

Table 2-45 • Minimum and Maximum DC Input and Output Levels Applicable to Pro I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	27	25	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-46 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-47 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	103	109	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-48 • Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range Applicable to Pro, Advanced, and Standard Plus I/O Banks

3.3 V LVCMOS Wide Range	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	µA[2]	µA[2]
All[2]	–0.3	0.8	2	3.6	0.2	V_{CCI} – 0.2	0.1	0.1	10	10

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *All LVMCOS 3.3 V software macros supports LVCMOS 3.3 V wide range as specificied in the JDEC8a specification*

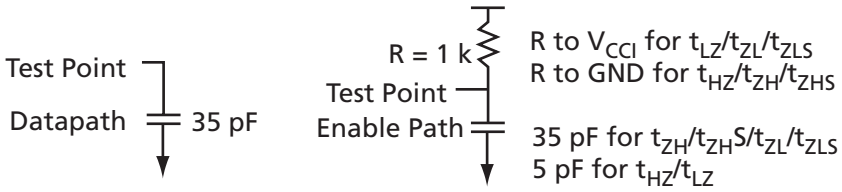


Figure 2-7 • AC Loading

Table 2-49 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	5

* *Measuring point = V_{trip}. See Table 2-26 on page 2-25 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-50 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.59	5.48	0.04	1.58	2.17	0.38	5.58	4.40	2.42	2.20	7.60	6.42	ns
	–1	0.50	4.66	0.03	1.34	1.85	0.33	4.75	3.75	2.06	1.87	6.46	5.46	ns
8 mA	Std.	0.59	4.48	0.04	1.58	2.17	0.38	4.56	3.76	2.73	2.76	6.57	5.78	ns
	–1	0.50	3.81	0.03	1.34	1.85	0.33	3.88	3.20	2.33	2.35	5.59	4.91	ns
12 mA	Std.	0.59	3.77	0.04	1.58	2.17	0.38	3.84	3.28	2.95	3.12	5.85	5.29	ns
	–1	0.50	3.21	0.03	1.34	1.85	0.33	3.27	2.79	2.51	2.65	4.98	4.50	ns
16 mA	Std.	0.59	3.57	0.04	1.58	2.17	0.38	3.63	3.18	2.99	3.22	5.64	5.19	ns
	–1	0.50	3.03	0.03	1.34	1.85	0.33	3.09	2.70	2.54	2.74	4.80	4.41	ns
24 mA	Std.	0.59	3.46	0.04	1.58	2.17	0.38	3.52	3.19	3.05	3.57	5.54	5.20	ns
	–1	0.50	2.94	0.03	1.34	1.85	0.33	3.00	2.71	2.59	3.03	4.71	4.42	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-51 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.59	3.08	0.04	1.58	2.17	0.38	3.14	2.36	2.42	2.33	5.15	4.38	ns
	–1	0.50	2.62	0.03	1.34	1.85	0.33	2.67	2.01	2.06	1.98	4.38	3.72	ns
8 mA	Std.	0.59	2.53	0.04	1.58	2.17	0.38	2.58	1.89	2.74	2.89	4.59	3.90	ns
	–1	0.50	2.16	0.03	1.34	1.85	0.33	2.20	1.61	2.33	2.46	3.91	3.32	ns
12 mA	Std.	0.59	2.22	0.04	1.58	2.17	0.38	2.27	1.67	2.95	3.25	4.28	3.68	ns
	–1	0.50	1.89	0.03	1.34	1.85	0.33	1.93	1.42	2.51	2.77	3.64	3.13	ns
16 mA	Std.	0.59	2.17	0.04	1.58	2.17	0.38	2.21	1.63	3.00	3.35	4.23	3.64	ns
	–1	0.50	1.85	0.03	1.34	1.85	0.33	1.88	1.38	2.55	2.85	3.59	3.09	ns
24 mA	Std.	0.59	2.19	0.04	1.58	2.17	0.38	2.24	1.57	3.05	3.71	4.25	3.58	ns
	–1	0.50	1.87	0.03	1.34	1.85	0.33	1.90	1.33	2.59	3.16	3.61	3.05	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-52 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	5.11	0.04	0.91	0.38	5.21	4.33	2.38	2.21	7.22	6.34	ns
	–1	0.46	4.35	0.03	0.78	0.33	4.43	3.68	2.02	1.88	6.14	5.40	ns
6 mA	Std.	0.54	4.30	0.04	0.91	0.38	4.38	3.75	2.68	2.74	6.39	5.76	ns
	–1	0.46	3.66	0.03	0.78	0.33	3.73	3.19	2.28	2.33	5.44	4.90	ns
8 mA	Std.	0.54	4.30	0.04	0.91	0.38	4.38	3.75	2.68	2.74	6.39	5.76	ns
	–1	0.46	3.66	0.03	0.78	0.33	3.73	3.19	2.28	2.33	5.44	4.90	ns
12 mA	Std.	0.54	3.68	0.04	0.91	0.38	3.75	3.32	2.89	3.07	5.76	5.33	ns
	–1	0.46	3.13	0.03	0.78	0.33	3.19	2.82	2.45	2.62	4.90	4.53	ns
16 mA	Std.	0.54	3.50	0.04	0.91	0.38	3.56	3.21	2.93	3.16	5.57	5.23	ns
	–1	0.46	2.97	0.03	0.78	0.33	3.03	2.73	2.49	2.69	4.74	4.45	ns
24 mA	Std.	0.54	3.39	0.04	0.91	0.38	3.45	3.25	2.99	3.50	5.47	5.26	ns
	–1	0.46	2.88	0.03	0.78	0.33	2.94	2.76	2.54	2.97	4.65	4.48	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-53 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	2.90	0.04	0.91	0.38	2.96	2.28	2.38	2.35	4.97	4.29	ns
	–1	0.46	2.47	0.03	0.78	0.33	2.52	1.94	2.03	2.00	4.23	3.65	ns
6 mA	Std.	0.54	2.41	0.04	0.91	0.38	2.46	1.84	2.69	2.88	4.47	3.85	ns
	–1	0.46	2.05	0.03	0.78	0.33	2.09	1.57	2.29	2.45	3.80	3.28	ns
8 mA	Std.	0.54	2.41	0.04	0.91	0.38	2.46	1.84	2.69	2.88	4.47	3.85	ns
	–1	0.46	2.05	0.03	0.78	0.33	2.09	1.57	2.29	2.45	3.80	3.28	ns
12 mA	Std.	0.54	2.16	0.04	0.91	0.38	2.20	1.63	2.89	3.22	4.21	3.64	ns
	–-1	0.46	1.83	0.03	0.78	0.33	1.87	1.39	2.46	2.74	3.58	3.10	ns
16 mA	Std.	0.54	2.11	0.04	0.91	0.38	2.15	1.59	2.94	3.31	4.17	3.61	ns
	–-1	0.46	1.80	0.03	0.78	0.33	1.83	1.36	2.50	2.82	3.54	3.07	ns
24 mA	Std.	0.54	2.14	0.04	0.91	0.38	2.17	1.55	2.99	3.65	4.19	3.56	ns
	–1	0.46	1.82	0.03	0.78	0.33	1.85	1.32	2.54	3.11	3.56	3.03	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-54 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	4.61	0.04	0.90	0.38	4.70	3.91	2.05	1.99	6.71	5.92	ns
	–1	0.46	3.92	0.03	0.77	0.33	4.00	3.32	1.74	1.69	5.71	5.04	ns
6 mA	Std.	0.54	3.80	0.04	0.90	0.38	3.87	3.40	2.32	2.47	5.88	5.41	ns
	–1	0.46	3.23	0.03	0.77	0.33	3.29	2.89	1.98	2.10	5.00	4.60	ns
8 mA	Std.	0.54	3.80	0.04	0.90	0.38	3.87	3.40	2.32	2.47	5.88	5.41	ns
	–1	0.46	3.23	0.03	0.77	0.33	3.29	2.89	1.98	2.10	5.00	4.60	ns
12 mA	Std.	0.54	3.22	0.04	0.90	0.38	3.28	3.00	2.51	2.77	5.30	5.01	ns
	–1	0.46	2.74	0.03	0.77	0.33	2.79	2.55	2.14	2.36	4.51	4.27	ns
16 mA	Std.	0.54	3.22	0.04	0.90	0.38	3.28	3.00	2.51	2.77	5.30	5.01	ns
	–1	0.46	2.74	0.03	0.77	0.33	2.79	2.55	2.14	2.36	4.51	4.27	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-55 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	2.51	0.04	0.90	0.38	2.56	2.01	2.05	2.10	4.57	4.02	ns
	–1	0.46	2.14	0.03	0.77	0.33	2.18	1.71	1.74	1.79	3.89	3.42	ns
6 mA	Std.	0.54	2.05	0.04	0.90	0.38	2.09	1.61	2.32	2.59	4.10	3.62	ns
	–1	0.46	1.74	0.03	0.77	0.33	1.78	1.37	1.97	2.20	3.49	3.08	ns
8 mA	Std.	0.54	2.05	0.04	0.90	0.38	2.09	1.61	2.32	2.59	4.10	3.62	ns
	–1	0.46	1.74	0.03	0.77	0.33	1.78	1.37	1.97	2.20	3.49	3.08	ns
12 mA	Std.	0.54	1.83	0.04	0.90	0.38	1.86	1.41	2.51	2.90	3.88	3.42	ns
	–1	0.46	1.56	0.03	0.77	0.33	1.59	1.20	2.14	2.47	3.30	2.91	ns
16 mA	Std.	0.54	1.83	0.04	0.90	0.38	1.86	1.41	2.51	2.90	3.88	3.42	ns
	–1	0.46	1.56	0.03	0.77	0.33	1.59	1.20	2.14	2.47	3.30	2.91	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

1.2 V DC Core Voltage

Table 2-56 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.77	5.48	0.05	1.58	2.17	0.50	5.58	4.40	2.42	2.20	7.60	6.42	ns
	–1	0.66	4.66	0.04	1.34	1.85	0.43	4.75	3.75	2.06	1.87	6.46	5.46	ns
8 mA	Std.	0.77	4.48	0.05	1.58	2.17	0.50	4.56	3.76	2.73	2.76	6.57	5.78	ns
	–1	0.66	3.81	0.04	1.34	1.85	0.43	3.88	3.20	2.33	2.35	5.59	4.91	ns
12 mA	Std.	0.77	3.77	0.05	1.58	2.17	0.50	3.84	3.28	2.95	3.12	5.85	5.29	ns
	–1	0.66	3.21	0.04	1.34	1.85	0.43	3.27	2.79	2.51	2.65	4.98	4.50	ns
16 mA	Std.	0.77	3.57	0.05	1.58	2.17	0.50	3.63	3.18	2.99	3.22	5.64	5.19	ns
	–1	0.66	3.03	0.04	1.34	1.85	0.43	3.09	2.70	2.54	2.74	4.80	4.41	ns
24 mA	Std.	0.77	3.46	0.05	1.58	2.17	0.50	3.52	3.19	3.05	3.57	5.54	5.20	ns
	–1	0.66	2.94	0.04	1.34	1.85	0.43	3.00	2.71	2.59	3.03	4.71	4.42	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-57 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.77	3.08	0.05	1.58	2.17	0.50	3.14	2.36	2.42	2.33	5.15	4.38	ns
	–1	0.66	2.62	0.04	1.34	1.85	0.43	2.67	2.01	2.06	1.98	4.38	3.72	ns
8 mA	Std.	0.77	2.53	0.05	1.58	2.17	0.50	2.58	1.89	2.74	2.89	4.59	3.90	ns
	–1	0.66	2.16	0.04	1.34	1.85	0.43	2.20	1.61	2.33	2.46	3.91	3.32	ns
12 mA	Std.	0.77	2.22	0.05	1.58	2.17	0.50	2.27	1.67	2.95	3.25	4.28	3.68	ns
	–1	0.66	1.89	0.04	1.34	1.85	0.43	1.93	1.42	2.51	2.77	3.64	3.13	ns
16 mA	Std.	0.77	2.17	0.05	1.58	2.17	0.50	2.21	1.63	3.00	3.35	4.23	3.64	ns
	–1	0.66	1.85	0.04	1.34	1.85	0.43	1.88	1.38	2.55	2.85	3.59	3.09	ns
24 mA	Std.	0.77	2.19	0.05	1.58	2.17	0.50	2.24	1.57	3.05	3.71	4.25	3.58	ns
	–1	0.66	1.87	0.04	1.34	1.85	0.43	1.90	1.33	2.59	3.16	3.61	3.05	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-58 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	5.11	0.05	0.91	0.50	5.21	4.33	2.38	2.21	7.22	6.34	ns
	–1	0.60	4.35	0.04	0.78	0.43	4.43	3.68	2.02	1.88	6.14	5.40	ns
6 mA	Std.	0.70	4.30	0.05	0.91	0.50	4.38	3.75	2.68	2.74	6.39	5.76	ns
	–1	0.60	3.66	0.04	0.78	0.43	3.73	3.19	2.28	2.33	5.44	4.90	ns
8 mA	Std.	0.70	4.30	0.05	0.91	0.50	4.38	3.75	2.68	2.74	6.39	5.76	ns
	–1	0.60	3.66	0.04	0.78	0.43	3.73	3.19	2.28	2.33	5.44	4.90	ns
12 mA	Std.	0.70	3.68	0.05	0.91	0.50	3.75	3.32	2.89	3.07	5.76	5.33	ns
	–1	0.60	3.13	0.04	0.78	0.43	3.19	2.82	2.45	2.62	4.90	4.53	ns
16 mA	Std.	0.70	3.50	0.05	0.91	0.50	3.56	3.21	2.93	3.16	5.57	5.23	ns
	–1	0.60	2.97	0.04	0.78	0.43	3.03	2.73	2.49	2.69	4.74	4.45	ns
24 mA	Std.	0.70	3.39	0.05	0.91	0.50	3.45	3.25	2.99	3.50	5.47	5.26	ns
	–1	0.60	2.88	0.04	0.78	0.43	2.94	2.76	2.54	2.97	4.65	4.48	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-59 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	2.90	0.05	0.91	0.50	2.96	2.28	2.38	2.35	4.97	4.29	ns
	–1	0.60	2.47	0.04	0.78	0.43	2.52	1.94	2.03	2.00	4.23	3.65	ns
6 mA	Std.	0.70	2.41	0.05	0.91	0.50	2.46	1.84	2.69	2.88	4.47	3.85	ns
	–1	0.60	2.05	0.04	0.78	0.43	2.09	1.57	2.29	2.45	3.80	3.28	ns
8 mA	Std.	0.70	2.41	0.05	0.91	0.50	2.46	1.84	2.69	2.88	4.47	3.85	ns
	–1	0.60	2.05	0.04	0.78	0.43	2.09	1.57	2.29	2.45	3.80	3.28	ns
12 mA	Std.	0.70	2.16	0.05	0.91	0.50	2.20	1.63	2.89	3.22	4.21	3.64	ns
	–1	0.60	1.83	0.04	0.78	0.43	1.87	1.39	2.46	2.74	3.58	3.10	ns
16 mA	Std.	0.70	2.11	0.05	0.91	0.50	2.15	1.59	2.94	3.31	4.17	3.61	ns
	–1	0.60	1.80	0.04	0.78	0.43	1.83	1.36	2.50	2.82	3.54	3.07	ns
24 mA	Std.	0.70	2.14	0.05	0.91	0.50	2.17	1.55	2.99	3.65	4.19	3.56	ns
	–1	0.60	1.82	0.04	0.78	0.43	1.85	1.32	2.54	3.11	3.56	3.03	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-60 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	4.61	0.05	0.90	0.50	4.70	3.91	2.05	1.99	6.71	5.92	ns
	–1	0.60	3.92	0.04	0.77	0.43	4.00	3.32	1.74	1.69	5.71	5.04	ns
6 mA	Std.	0.70	3.80	0.05	0.90	0.50	3.87	3.40	2.32	2.47	5.88	5.41	ns
	–1	0.60	3.23	0.04	0.77	0.43	3.29	2.89	1.98	2.10	5.00	4.60	ns
8 mA	Std.	0.70	3.80	0.05	0.90	0.50	3.87	3.40	2.32	2.47	5.88	5.41	ns
	–1	0.60	3.23	0.04	0.77	0.43	3.29	2.89	1.98	2.10	5.00	4.60	ns
12 mA	Std.	0.70	3.22	0.05	0.90	0.50	3.28	3.00	2.51	2.77	5.30	5.01	ns
	–1	0.60	2.74	0.04	0.77	0.43	2.79	2.55	2.14	2.36	4.51	4.27	ns
16 mA	Std.	0.70	3.22	0.05	0.90	0.50	3.28	3.00	2.51	2.77	5.30	5.01	ns
	–1	0.60	2.74	0.04	0.77	0.43	2.79	2.55	2.14	2.36	4.51	4.27	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-61 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	2.51	0.05	0.90	0.50	2.56	2.01	2.05	2.10	4.57	4.02	ns
	–1	0.60	2.14	0.04	0.77	0.43	2.18	1.71	1.74	1.79	3.89	3.42	ns
6 mA	Std.	0.70	2.05	0.05	0.90	0.50	2.09	1.61	2.32	2.59	4.10	3.62	ns
	–1	0.60	1.74	0.04	0.77	0.43	1.78	1.37	1.97	2.20	3.49	3.08	ns
8 mA	Std.	0.70	2.05	0.05	0.90	0.50	2.09	1.61	2.32	2.59	4.10	3.62	ns
	–1	0.60	1.74	0.04	0.77	0.43	1.78	1.37	1.97	2.20	3.49	3.08	ns
12 mA	Std.	0.70	1.83	0.05	0.90	0.50	1.86	1.41	2.51	2.90	3.88	3.42	ns
	–1	0.60	1.56	0.04	0.77	0.43	1.59	1.20	2.14	2.47	3.30	2.91	ns
16 mA	Std.	0.70	1.83	0.05	0.90	0.50	1.86	1.41	2.51	2.90	3.88	3.42	ns
	–1	0.60	1.56	0.04	0.77	0.43	1.59	1.20	2.14	2.47	3.30	2.91	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications. It uses a 5 V–tolerant input buffer and push-pull output buffer.

Table 2-62 • Minimum and Maximum DC Input and Output Levels Applicable to Pro I/Os

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	10	10
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-63 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	10	10
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-64 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

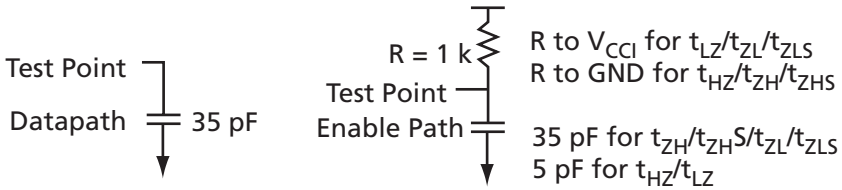


Figure 2-8 • AC Loading

Table 2-65 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	2.5	1.2	5

* *Measuring point = V_{trip}. See Table 2-26 on page 2-25 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-66 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.59	6.24	0.04	1.86	2.31	0.38	6.36	5.30	2.45	1.98	8.37	7.31	ns
	–1	0.50	5.31	0.03	1.58	1.97	0.33	5.41	4.51	2.08	1.68	7.12	6.22	ns
8 mA	Std.	0.59	5.10	0.04	1.86	2.31	0.38	5.20	4.49	2.79	2.64	7.21	6.50	ns
	–1	0.50	4.34	0.03	1.58	1.97	0.33	4.42	3.82	2.37	2.24	6.13	5.53	ns
12 mA	Std.	0.59	4.29	0.04	1.86	2.31	0.38	4.37	3.91	3.03	3.05	6.39	5.92	ns
	–1	0.50	3.65	0.03	1.58	1.97	0.33	3.72	3.32	2.58	2.60	5.43	5.04	ns
16 mA	Std.	0.59	4.05	0.04	1.86	2.31	0.38	4.12	3.78	3.08	3.17	6.13	5.79	ns
	–1	0.50	3.44	0.03	1.58	1.97	0.33	3.51	3.22	2.62	2.70	5.22	4.93	ns
24 mA	Std.	0.59	3.94	0.04	1.86	2.31	0.38	4.01	3.80	3.15	3.60	6.03	5.81	ns
	–1	0.50	3.35	0.03	1.58	1.97	0.33	3.41	3.23	2.68	3.06	5.13	4.94	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-67 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.59	3.18	0.04	1.86	2.31	0.38	3.24	2.84	2.45	2.06	5.25	4.85	ns
	–1	0.50	2.71	0.03	1.58	1.97	0.33	2.76	2.42	2.08	1.75	4.47	4.13	ns
8 mA	Std.	0.59	2.61	0.04	1.86	2.31	0.38	2.65	2.19	2.79	2.73	4.67	4.20	ns
	–1	0.50	2.22	0.03	1.58	1.97	0.33	2.26	1.86	2.37	2.32	3.97	3.57	ns
12 mA	Std.	0.59	2.26	0.04	1.86	2.31	0.38	2.30	1.86	3.03	3.15	4.32	3.88	ns
	–1	0.50	1.92	0.03	1.58	1.97	0.33	1.96	1.59	2.58	2.68	3.67	3.30	ns
16 mA	Std.	0.59	2.20	0.04	1.86	2.31	0.38	2.24	1.80	3.08	3.26	4.26	3.82	ns
	–1	0.50	1.87	0.03	1.58	1.97	0.33	1.91	1.54	2.62	2.77	3.62	3.25	ns
24 mA	Std.	0.59	2.21	0.04	1.86	2.31	0.38	2.25	1.73	3.15	3.70	4.27	3.74	ns
	–1	0.50	1.88	0.03	1.58	1.97	0.33	1.92	1.47	2.68	3.14	3.63	3.18	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-68 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	5.79	0.04	1.18	0.38	5.90	5.18	2.41	1.98	7.91	7.19	ns
	–1	0.46	4.92	0.03	1.00	0.33	5.01	4.40	2.05	1.69	6.73	6.11	ns
6 mA	Std.	0.54	4.84	0.04	1.18	0.38	4.93	4.43	2.74	2.60	6.94	6.44	ns
	–1	0.46	4.11	0.03	1.00	0.33	4.19	3.77	2.33	2.21	5.90	5.48	ns
8 mA	Std.	0.54	4.84	0.04	1.18	0.38	4.93	4.43	2.74	2.60	6.94	6.44	ns
	–1	0.46	4.11	0.03	1.00	0.33	4.19	3.77	2.33	2.21	5.90	5.48	ns
12 mA	Std.	0.54	4.13	0.04	1.18	0.38	4.21	3.92	2.97	2.99	6.22	5.93	ns
	–1	0.46	3.52	0.03	1.00	0.33	3.58	3.33	2.53	2.54	5.29	5.04	ns
16 mA	Std.	0.54	3.91	0.04	1.18	0.38	3.98	3.80	3.02	3.09	5.99	5.81	ns
	–1	0.46	3.32	0.03	1.00	0.33	3.39	3.23	2.57	2.63	5.10	4.94	ns
24 mA	Std.	0.54	3.85	0.04	1.18	0.38	3.87	3.85	3.09	3.48	5.88	5.87	ns
	–1	0.46	3.28	0.03	1.00	0.33	3.29	3.28	2.63	2.96	5.01	4.99	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-69 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	2.97	0.04	1.18	0.38	3.03	2.74	2.41	2.07	5.04	4.75	ns
	–1	0.46	2.53	0.03	1.00	0.33	2.58	2.33	2.05	1.76	4.29	4.04	ns
6 mA	Std.	0.54	2.44	0.04	1.18	0.38	2.49	2.12	2.74	2.70	4.50	4.13	ns
	–1	0.46	2.08	0.03	1.00	0.33	2.12	1.80	2.33	2.30	3.83	3.51	ns
8 mA	Std.	0.54	2.44	0.04	1.18	0.38	2.49	2.12	2.74	2.70	4.50	4.13	ns
	–1	0.46	2.08	0.03	1.00	0.33	2.12	1.80	2.33	2.30	3.83	3.51	ns
12 mA	Std.	0.54	2.17	0.04	1.18	0.38	2.21	1.82	2.97	3.09	4.22	3.83	ns
	–1	0.46	1.85	0.03	1.00	0.33	1.88	1.55	2.53	2.63	3.59	3.26	ns
16 mA	Std.	0.54	2.12	0.04	1.18	0.38	2.16	1.76	3.03	3.19	4.17	3.78	ns
	–1	0.46	1.81	0.03	1.00	0.33	1.84	1.50	2.57	2.72	3.55	3.21	ns
24 mA	Std.	0.54	2.13	0.04	1.18	0.38	2.17	1.71	3.09	3.60	4.19	3.72	ns
	–1	0.46	1.81	0.03	1.00	0.33	1.85	1.45	2.63	3.06	3.56	3.16	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-70 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	5.27	0.04	1.17	0.38	5.37	4.68	2.03	1.79	7.38	6.69	ns
	–1	0.46	4.49	0.03	0.99	0.33	4.57	3.98	1.73	1.52	6.28	5.69	ns
6 mA	Std.	0.54	4.32	0.04	1.17	0.38	4.40	4.03	2.33	2.35	6.42	6.04	ns
	–1	0.46	3.68	0.03	0.99	0.33	3.75	3.43	1.98	2.00	5.46	5.14	ns
8 mA	Std.	0.54	4.32	0.04	1.17	0.38	4.40	4.03	2.33	2.35	6.42	6.04	ns
	–1	0.46	3.68	0.03	0.99	0.33	3.75	3.43	1.98	2.00	5.46	5.14	ns
12 mA	Std.	0.54	3.66	0.04	1.17	0.38	3.73	3.56	2.54	2.71	5.74	5.57	ns
	–1	0.46	3.12	0.03	0.99	0.33	3.17	3.03	2.16	2.30	4.89	4.74	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-71 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.54	2.60	0.04	1.17	0.38	2.65	2.39	2.03	1.87	4.66	4.40	ns
	–1	0.46	2.21	0.03	0.99	0.33	2.25	2.03	1.72	1.59	3.96	3.74	ns
6 mA	Std.	0.54	2.10	0.04	1.17	0.38	2.14	1.83	2.33	2.44	4.16	3.84	ns
	–1	0.46	1.79	0.03	0.99	0.33	1.82	1.56	1.98	2.07	3.54	3.27	ns
8 mA	Std.	0.54	2.10	0.04	1.17	0.38	2.14	1.83	2.33	2.44	4.16	3.84	ns
	–1	0.46	1.79	0.03	0.99	0.33	1.82	1.56	1.98	2.07	3.54	3.27	ns
12 mA	Std.	0.54	1.86	0.04	1.17	0.38	1.90	1.55	2.54	2.80	3.91	3.57	ns
	–1	0.46	1.59	0.03	0.99	0.33	1.61	1.32	2.16	2.38	3.33	3.03	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

1.2 V DC Core Voltage

Table 2-72 • 2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.77	6.24	0.05	1.86	2.31	0.50	6.36	5.30	2.45	1.98	8.37	7.31	ns
	–1	0.66	5.31	0.04	1.58	1.97	0.43	5.41	4.51	2.08	1.68	7.12	6.22	ns
8 mA	Std.	0.77	5.10	0.05	1.86	2.31	0.50	5.20	4.49	2.79	2.64	7.21	6.50	ns
	–1	0.66	4.34	0.04	1.58	1.97	0.43	4.42	3.82	2.37	2.24	6.13	5.53	ns
12 mA	Std.	0.77	4.29	0.05	1.86	2.31	0.50	4.37	3.91	3.03	3.05	6.39	5.92	ns
	–1	0.66	3.65	0.04	1.58	1.97	0.43	3.72	3.32	2.58	2.60	5.43	5.04	ns
16 mA	Std.	0.77	4.05	0.05	1.86	2.31	0.50	4.12	3.78	3.08	3.17	6.13	5.79	ns
	–1	0.66	3.44	0.04	1.58	1.97	0.43	3.51	3.22	2.62	2.70	5.22	4.93	ns
24 mA	Std.	0.77	3.94	0.05	1.86	2.31	0.50	4.01	3.80	3.15	3.60	6.03	5.81	ns
	–1	0.66	3.35	0.04	1.58	1.97	0.43	3.41	3.23	2.68	3.06	5.13	4.94	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-73 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Pro I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.77	3.18	0.05	1.86	2.31	0.50	3.24	2.84	2.45	2.06	5.25	4.85	ns
	–1	0.66	2.71	0.04	1.58	1.97	0.43	2.76	2.42	2.08	1.75	4.47	4.13	ns
8 mA	Std.	0.77	2.61	0.05	1.86	2.31	0.50	2.65	2.19	2.79	2.73	4.67	4.20	ns
	–1	0.66	2.22	0.04	1.58	1.97	0.43	2.26	1.86	2.37	2.32	3.97	3.57	ns
12 mA	Std.	0.77	2.26	0.05	1.86	2.31	0.50	2.30	1.86	3.03	3.15	4.32	3.88	ns
	–1	0.66	1.92	0.04	1.58	1.97	0.43	1.96	1.59	2.58	2.68	3.67	3.30	ns
16 mA	Std.	0.77	2.20	0.05	1.86	2.31	0.50	2.24	1.80	3.08	3.26	4.26	3.82	ns
	–1	0.66	1.87	0.04	1.58	1.97	0.43	1.91	1.54	2.62	2.77	3.62	3.25	ns
24 mA	Std.	0.77	2.21	0.05	1.86	2.31	0.50	2.25	1.73	3.15	3.70	4.27	3.74	ns
	–1	0.66	1.88	0.04	1.58	1.97	0.43	1.92	1.47	2.68	3.14	3.63	3.18	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-74 • 2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Advanced I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	5.79	0.05	1.18	0.50	5.90	5.18	2.41	1.98	7.91	7.19	ns
	–1	0.60	4.92	0.04	1.00	0.43	5.01	4.40	2.05	1.69	6.73	6.11	ns
6 mA	Std.	0.70	4.84	0.05	1.18	0.50	4.93	4.43	2.74	2.60	6.94	6.44	ns
	–1	0.60	4.11	0.04	1.00	0.43	4.19	3.77	2.33	2.21	5.90	5.48	ns
8 mA	Std.	0.70	4.84	0.05	1.18	0.50	4.93	4.43	2.74	2.60	6.94	6.44	ns
	–1	0.60	4.11	0.04	1.00	0.43	4.19	3.77	2.33	2.21	5.90	5.48	ns
12 mA	Std.	0.70	4.13	0.05	1.18	0.50	4.21	3.92	2.97	2.99	6.22	5.93	ns
	–1	0.60	3.52	0.04	1.00	0.43	3.58	3.33	2.53	2.54	5.29	5.04	ns
16 mA	Std.	0.70	3.91	0.05	1.18	0.50	3.98	3.80	3.02	3.09	5.99	5.81	ns
	–1	0.60	3.32	0.04	1.00	0.43	3.39	3.23	2.57	2.63	5.10	4.94	ns
24 mA	Std.	0.70	3.85	0.05	1.18	0.50	3.87	3.85	3.09	3.48	5.88	5.87	ns
	–1	0.60	3.28	0.04	1.00	0.43	3.29	3.28	2.63	2.96	5.01	4.99	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-75 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Advanced I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	2.97	0.05	1.18	0.50	3.03	2.74	2.41	2.07	5.04	4.75	ns
	–1	0.60	2.53	0.04	1.00	0.43	2.58	2.33	2.05	1.76	4.29	4.04	ns
6 mA	Std.	0.70	2.44	0.05	1.18	0.50	2.49	2.12	2.74	2.70	4.50	4.13	ns
	–1	0.60	2.08	0.04	1.00	0.43	2.12	1.80	2.33	2.30	3.83	3.51	ns
8 mA	Std.	0.70	2.44	0.05	1.18	0.50	2.49	2.12	2.74	2.70	4.50	4.13	ns
	–1	0.60	2.08	0.04	1.00	0.43	2.12	1.80	2.33	2.30	3.83	3.51	ns
12 mA	Std.	0.70	2.17	0.05	1.18	0.50	2.21	1.82	2.97	3.09	4.22	3.83	ns
	–1	0.60	1.85	0.04	1.00	0.43	1.88	1.55	2.53	2.63	3.59	3.26	ns
16 mA	Std.	0.70	2.12	0.05	1.18	0.50	2.16	1.76	3.03	3.19	4.17	3.78	ns
	–1	0.60	1.81	0.04	1.00	0.43	1.84	1.50	2.57	2.72	3.55	3.21	ns
24 mA	Std.	0.70	2.13	0.05	1.18	0.50	2.17	1.71	3.09	3.60	4.19	3.72	ns
	–1	0.60	1.81	0.04	1.00	0.43	1.85	1.45	2.63	3.06	3.56	3.16	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-76 • 2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Plus I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	5.27	0.05	1.17	0.50	5.37	4.68	2.03	1.79	7.38	6.69	ns
	–1	0.60	4.49	0.04	0.99	0.43	4.57	3.98	1.73	1.52	6.28	5.69	ns
6 mA	Std.	0.70	4.32	0.05	1.17	0.50	4.40	4.03	2.33	2.35	6.42	6.04	ns
	–1	0.60	3.68	0.04	0.99	0.43	3.75	3.43	1.98	2.00	5.46	5.14	ns
8 mA	Std.	0.70	4.32	0.05	1.17	0.50	4.40	4.03	2.33	2.35	6.42	6.04	ns
	–1	0.60	3.68	0.04	0.99	0.43	3.75	3.43	1.98	2.00	5.46	5.14	ns
12 mA	Std.	0.70	3.66	0.05	1.17	0.50	3.73	3.56	2.54	2.71	5.74	5.57	ns
	–1	0.60	3.12	0.04	0.99	0.43	3.17	3.03	2.16	2.30	4.89	4.74	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-77 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Plus I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.70	2.60	0.05	1.17	0.50	2.65	2.39	2.03	1.87	4.66	4.40	ns
	–1	0.60	2.21	0.04	0.99	0.43	2.25	2.03	1.72	1.59	3.96	3.74	ns
6 mA	Std.	0.70	2.10	0.05	1.17	0.50	2.14	1.83	2.33	2.44	4.16	3.84	ns
	–1	0.60	1.79	0.04	0.99	0.43	1.82	1.56	1.98	2.07	3.54	3.27	ns
8 mA	Std.	0.70	2.10	0.05	1.17	0.50	2.14	1.83	2.33	2.44	4.16	3.84	ns
	–1	0.60	1.79	0.04	0.99	0.43	1.82	1.56	1.98	2.07	3.54	3.27	ns
12 mA	Std.	0.70	1.86	0.05	1.17	0.50	1.90	1.55	2.54	2.80	3.91	3.57	ns
	–1	0.60	1.59	0.04	0.99	0.43	1.61	1.32	2.16	2.38	3.33	3.03	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-78 • Minimum and Maximum DC Input and Output Levels Applicable to Pro I/Os

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	4	4	17	22	10	10
6 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	6	6	35	44	10	10
8 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	8	8	45	51	10	10
12 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	12	12	91	74	10	10
16 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	16	16	91	74	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-79 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	4	4	17	22	10	10
6 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	6	6	35	44	10	10
8 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	8	8	45	51	10	10
12 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	12	12	91	74	10	10
16 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	16	16	91	74	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-80 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O I/O Banks

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	4	4	17	22	10	10
6 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	6	6	35	44	10	10
8 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	8	8	35	44	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

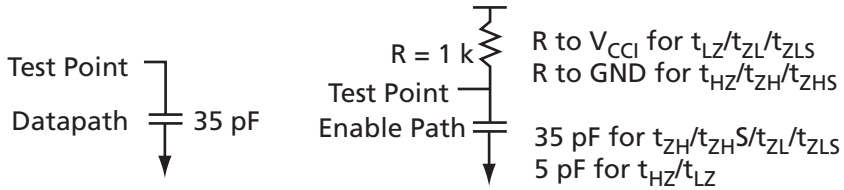


Figure 2-9 • AC Loading

Table 2-81 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.8	0.9	5

* *Measuring point = V_{trip}. See Table 2-26 on page 2-25 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-82 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.59	8.32	0.04	1.80	2.55	0.38	8.48	6.99	2.50	1.42	10.49	9.00	ns
	–1	0.50	7.08	0.03	1.53	2.17	0.33	7.21	5.95	2.13	1.21	8.92	7.66	ns
4 mA	Std.	0.59	6.85	0.04	1.80	2.55	0.38	6.98	5.89	2.93	2.50	8.99	7.90	ns
	–1	0.50	5.83	0.03	1.53	2.17	0.33	5.94	5.01	2.49	2.12	7.65	6.72	ns
6 mA	Std.	0.59	5.81	0.04	1.80	2.55	0.38	5.92	5.13	3.21	3.02	7.93	7.15	ns
	–1	0.50	4.94	0.03	1.53	2.17	0.33	5.03	4.37	2.73	2.57	6.75	6.08	ns
8 mA	Std.	0.59	5.46	0.04	1.80	2.55	0.38	5.56	4.99	3.28	3.17	7.57	7.00	ns
	–1	0.50	4.64	0.03	1.53	2.17	0.33	4.73	4.24	2.79	2.70	6.44	5.95	ns
12 mA	Std.	0.59	5.36	0.04	1.80	2.55	0.38	5.46	4.99	3.37	3.70	7.47	7.01	ns
	–1	0.50	4.56	0.03	1.53	2.17	0.33	4.64	4.25	2.86	3.14	6.35	5.96	ns
16 mA	Std.	0.59	5.36	0.04	1.80	2.55	0.38	5.46	4.99	3.37	3.70	7.47	7.01	ns
	–1	0.50	4.56	0.03	1.53	2.17	0.33	4.64	4.25	2.86	3.14	6.35	5.96	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-83 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.59	3.76	0.04	1.80	2.55	0.38	3.83	3.68	2.50	1.47	5.84	5.70	ns
	–1	0.50	3.20	0.03	1.53	2.17	0.33	3.26	3.13	2.13	1.25	4.97	4.85	ns
4 mA	Std.	0.59	3.05	0.04	1.80	2.55	0.38	3.11	2.73	2.92	2.58	5.12	4.75	ns
	–1	0.50	2.59	0.03	1.53	2.17	0.33	2.64	2.33	2.49	2.19	4.35	4.04	ns
6 mA	Std.	0.59	2.61	0.04	1.80	2.55	0.38	2.66	2.27	3.21	3.12	4.67	4.28	ns
	–1	0.50	2.22	0.03	1.53	2.17	0.33	2.26	1.93	2.73	2.65	3.98	3.64	ns
8 mA	Std.	0.59	2.53	0.04	1.80	2.55	0.38	2.58	2.18	3.27	3.26	4.59	4.19	ns
	–1	0.50	2.15	0.03	1.53	2.17	0.33	2.19	1.85	2.78	2.77	3.90	3.57	ns
12 mA	Std.	0.59	2.52	0.04	1.80	2.55	0.38	2.56	2.07	3.36	3.81	4.58	4.08	ns
	–1	0.50	2.14	0.03	1.53	2.17	0.33	2.18	1.76	2.86	3.24	3.89	3.47	ns
16 mA	Std.	0.59	2.52	0.04	1.80	2.55	0.38	2.56	2.07	3.36	3.81	4.58	4.08	ns
	–1	0.50	2.14	0.03	1.53	2.17	0.33	2.18	1.76	2.86	3.24	3.89	3.47	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-84 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.54	7.77	0.04	1.18	0.38	7.92	6.80	2.50	1.44	9.93	8.81	ns
	–1	0.46	6.61	0.03	1.00	0.33	6.73	5.78	2.13	1.22	8.45	7.49	ns
4 mA	Std.	0.54	6.38	0.04	1.18	0.38	6.50	5.78	2.91	2.46	8.51	7.79	ns
	–1	0.46	5.43	0.03	1.00	0.33	5.53	4.91	2.47	2.09	7.24	6.63	ns
6 mA	Std.	0.54	5.48	0.04	1.18	0.38	5.58	5.11	3.18	2.94	7.59	7.12	ns
	–1	0.46	4.66	0.03	1.00	0.33	4.75	4.35	2.71	2.51	6.46	6.06	ns
8 mA	Std.	0.54	5.17	0.04	1.18	0.38	5.26	4.97	3.24	3.07	7.27	6.98	ns
	–1	0.46	4.40	0.03	1.00	0.33	4.48	4.23	2.76	2.61	6.19	5.94	ns
12 mA	Std.	0.54	5.06	0.04	1.18	0.38	5.15	5.03	3.34	3.55	7.17	7.04	ns
	–1	0.46	4.30	0.03	1.00	0.33	4.38	4.28	2.84	3.02	6.10	5.99	ns
16 mA	Std.	0.54	5.06	0.04	1.18	0.38	5.15	5.03	3.34	3.55	7.17	7.04	ns
	–1	0.46	4.30	0.03	1.00	0.33	4.38	4.28	2.84	3.02	6.10	5.99	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-85 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.54	3.60	0.04	1.10	0.38	3.66	3.52	2.49	1.49	5.68	5.53	ns
	–1	0.46	3.06	0.03	0.93	0.33	3.12	3.00	2.12	1.27	4.83	4.71	ns
4 mA	Std.	0.54	2.81	0.04	1.10	0.38	2.87	2.64	2.90	2.55	4.88	4.65	ns
	–1	0.46	2.39	0.03	0.93	0.33	2.44	2.25	2.47	2.17	4.15	3.96	ns
6 mA	Std.	0.54	2.47	0.04	1.10	0.38	2.51	2.21	3.18	3.04	4.53	4.22	ns
	–1	0.46	2.10	0.03	0.93	0.33	2.14	1.88	2.70	2.59	3.85	3.59	ns
8 mA	Std.	0.54	2.40	0.04	1.10	0.38	2.45	2.13	3.24	3.17	4.46	4.14	ns
	–1	0.46	2.04	0.03	0.93	0.33	2.08	1.81	2.76	2.70	3.79	3.52	ns
12 mA	Std.	0.54	2.39	0.04	1.10	0.38	2.44	2.04	3.33	3.67	4.45	4.05	ns
	–1	0.46	2.04	0.03	0.93	0.33	2.08	1.73	2.83	3.12	3.79	3.45	ns
16 mA	Std.	0.54	2.39	0.04	1.10	0.38	2.44	2.04	3.33	3.67	4.45	4.05	ns
	–1	0.46	2.04	0.03	0.93	0.33	2.08	1.73	2.83	3.12	3.79	3.45	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-86 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.54	7.21	0.04	1.17	0.38	7.35	6.14	2.03	1.32	9.36	8.16	ns
	–1	0.46	6.13	0.03	0.99	0.33	6.25	5.23	1.72	1.12	7.96	6.94	ns
4 mA	Std.	0.54	5.81	0.04	1.17	0.38	5.92	5.26	2.39	2.25	7.93	7.27	ns
	–1	0.46	4.94	0.03	0.99	0.33	5.03	4.47	2.03	1.91	6.74	6.19	ns
6 mA	Std.	0.54	4.96	0.04	1.17	0.38	5.05	4.65	2.64	2.69	7.06	6.66	ns
	–1	0.46	4.22	0.03	0.99	0.33	4.30	3.96	2.25	2.29	6.01	5.67	ns
8 mA	Std.	0.54	4.96	0.04	1.17	0.38	5.05	4.65	2.64	2.69	7.06	6.66	ns
	–1	0.46	4.22	0.03	0.99	0.33	4.30	3.96	2.25	2.29	6.01	5.67	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-87 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.54	3.22	0.04	1.08	0.38	3.28	3.04	2.02	1.37	5.30	5.06	ns
	–1	0.46	2.74	0.03	0.92	0.33	2.79	2.59	1.72	1.17	4.50	4.30	ns
4 mA	Std.	0.54	2.48	0.04	1.08	0.38	2.53	2.25	2.38	2.34	4.54	4.26	ns
	–1	0.46	2.11	0.03	0.92	0.33	2.15	1.92	2.03	1.99	3.86	3.63	ns
6 mA	Std.	0.54	2.17	0.04	1.08	0.38	2.21	1.86	2.64	2.79	4.22	3.87	ns
	–1	0.46	1.85	0.03	0.92	0.33	1.88	1.58	2.24	2.37	3.59	3.29	ns
8 mA	Std.	0.54	2.17	0.04	1.08	0.38	2.21	1.86	2.64	2.79	4.22	3.87	ns
	–1	0.46	1.85	0.03	0.92	0.33	1.88	1.58	2.24	2.37	3.59	3.29	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

1.2 V DC Core Voltage

Table 2-88 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.77	8.32	0.05	1.80	2.55	0.50	8.48	6.99	2.50	1.42	10.49	9.00	ns
	–1	0.66	7.08	0.04	1.53	2.17	0.43	7.21	5.95	2.13	1.21	8.92	7.66	ns
4 mA	Std.	0.77	6.85	0.05	1.80	2.55	0.50	6.98	5.89	2.93	2.50	8.99	7.90	ns
	–1	0.66	5.83	0.04	1.53	2.17	0.43	5.94	5.01	2.49	2.12	7.65	6.72	ns
6 mA	Std.	0.77	5.81	0.05	1.80	2.55	0.50	5.92	5.13	3.21	3.02	7.93	7.15	ns
	–1	0.66	4.94	0.04	1.53	2.17	0.43	5.03	4.37	2.73	2.57	6.75	6.08	ns
8 mA	Std.	0.77	5.46	0.05	1.80	2.55	0.50	5.56	4.99	3.28	3.17	7.57	7.00	ns
	–1	0.66	4.64	0.04	1.53	2.17	0.43	4.73	4.24	2.79	2.70	6.44	5.95	ns
12 mA	Std.	0.77	5.36	0.05	1.80	2.55	0.50	5.46	4.99	3.37	3.70	7.47	7.01	ns
	–1	0.66	4.56	0.04	1.53	2.17	0.43	4.64	4.25	2.86	3.14	6.35	5.96	ns
16 mA	Std.	0.77	5.36	0.05	1.80	2.55	0.50	5.46	4.99	3.37	3.70	7.47	7.01	ns
	–1	0.66	4.56	0.04	1.53	2.17	0.43	4.64	4.25	2.86	3.14	6.35	5.96	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-89 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.77	3.76	0.05	1.80	2.55	0.50	3.83	3.68	2.50	1.47	5.84	5.70	ns
	–1	0.66	3.20	0.04	1.53	2.17	0.43	3.26	3.13	2.13	1.25	4.97	4.85	ns
4 mA	Std.	0.77	3.05	0.05	1.80	2.55	0.50	3.11	2.73	2.92	2.58	5.12	4.75	ns
	–1	0.66	2.59	0.04	1.53	2.17	0.43	2.64	2.33	2.49	2.19	4.35	4.04	ns
6 mA	Std.	0.77	2.61	0.05	1.80	2.55	0.50	2.66	2.27	3.21	3.12	4.67	4.28	ns
	–1	0.66	2.22	0.04	1.53	2.17	0.43	2.26	1.93	2.73	2.65	3.98	3.64	ns
8 mA	Std.	0.77	2.53	0.05	1.80	2.55	0.50	2.58	2.18	3.27	3.26	4.59	4.19	ns
	–1	0.66	2.15	0.04	1.53	2.17	0.43	2.19	1.85	2.78	2.77	3.90	3.57	ns
12 mA	Std.	0.77	2.52	0.05	1.80	2.55	0.50	2.56	2.07	3.36	3.81	4.58	4.08	ns
	–1	0.66	2.14	0.04	1.53	2.17	0.43	2.18	1.76	2.86	3.24	3.89	3.47	ns
16 mA	Std.	0.77	2.52	0.05	1.80	2.55	0.50	2.56	2.07	3.36	3.81	4.58	4.08	ns
	–1	0.66	2.14	0.04	1.53	2.17	0.43	2.18	1.76	2.86	3.24	3.89	3.47	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-90 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	7.77	0.05	1.18	0.50	7.92	6.80	2.50	1.44	9.93	8.81	ns
	–1	0.60	6.61	0.04	1.00	0.43	6.73	5.78	2.13	1.22	8.45	7.49	ns
4 mA	Std.	0.70	6.38	0.05	1.18	0.50	6.50	5.78	2.91	2.46	8.51	7.79	ns
	–1	0.60	5.43	0.04	1.00	0.43	5.53	4.91	2.47	2.09	7.24	6.63	ns
6 mA	Std.	0.70	5.48	0.05	1.18	0.50	5.58	5.11	3.18	2.94	7.59	7.12	ns
	–1	0.60	4.66	0.04	1.00	0.43	4.75	4.35	2.71	2.51	6.46	6.06	ns
8 mA	Std.	0.70	5.17	0.05	1.18	0.50	5.26	4.97	3.24	3.07	7.27	6.98	ns
	–1	0.60	4.40	0.04	1.00	0.43	4.48	4.23	2.76	2.61	6.19	5.94	ns
12 mA	Std.	0.70	5.06	0.05	1.18	0.50	5.15	5.03	3.34	3.55	7.17	7.04	ns
	–1	0.60	4.30	0.04	1.00	0.43	4.38	4.28	2.84	3.02	6.10	5.99	ns
16 mA	Std.	0.70	5.06	0.05	1.18	0.50	5.15	5.03	3.34	3.55	7.17	7.04	ns
	–1	0.60	4.30	0.04	1.00	0.43	4.38	4.28	2.84	3.02	6.10	5.99	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-91 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	3.60	0.05	1.10	0.50	3.66	3.52	2.49	1.49	5.68	5.53	ns
	–1	0.60	3.06	0.04	0.93	0.43	3.12	3.00	2.12	1.27	4.83	4.71	ns
4 mA	Std.	0.70	2.81	0.05	1.10	0.50	2.87	2.64	2.90	2.55	4.88	4.65	ns
	–1	0.60	2.39	0.04	0.93	0.43	2.44	2.25	2.47	2.17	4.15	3.96	ns
6 mA	Std.	0.70	2.47	0.05	1.10	0.50	2.51	2.21	3.18	3.04	4.53	4.22	ns
	–1	0.60	2.10	0.04	0.93	0.43	2.14	1.88	2.70	2.59	3.85	3.59	ns
8 mA	Std.	0.70	2.40	0.05	1.10	0.50	2.45	2.13	3.24	3.17	4.46	4.14	ns
	–1	0.60	2.04	0.04	0.93	0.43	2.08	1.81	2.76	2.70	3.79	3.52	ns
12 mA	Std.	0.70	2.39	0.05	1.10	0.50	2.44	2.04	3.33	3.67	4.45	4.05	ns
	–1	0.60	2.04	0.04	0.93	0.43	2.08	1.73	2.83	3.12	3.79	3.45	ns
16 mA	Std.	0.70	2.39	0.05	1.10	0.50	2.44	2.04	3.33	3.67	4.45	4.05	ns
	–1	0.60	2.04	0.04	0.93	0.43	2.08	1.73	2.83	3.12	3.79	3.45	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-92 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	7.21	0.05	1.17	0.50	7.35	6.14	2.03	1.32	9.36	8.16	ns
	–1	0.60	6.13	0.04	0.99	0.43	6.25	5.23	1.72	1.12	7.96	6.94	ns
4 mA	Std.	0.70	5.81	0.05	1.17	0.50	5.92	5.26	2.39	2.25	7.93	7.27	ns
	–1	0.60	4.94	0.04	0.99	0.43	5.03	4.47	2.03	1.91	6.74	6.19	ns
6 mA	Std.	0.70	4.96	0.05	1.17	0.50	5.05	4.65	2.64	2.69	7.06	6.66	ns
	–1	0.60	4.22	0.04	0.99	0.43	4.30	3.96	2.25	2.29	6.01	5.67	ns
8 mA	Std.	0.70	4.96	0.05	1.17	0.50	5.05	4.65	2.64	2.69	7.06	6.66	ns
	–1	0.60	4.22	0.04	0.99	0.43	4.30	3.96	2.25	2.29	6.01	5.67	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-93 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	3.22	0.05	1.08	0.50	3.28	3.04	2.02	1.37	5.30	5.06	ns
	–1	0.60	2.74	0.04	0.92	0.43	2.79	2.59	1.72	1.17	4.50	4.30	ns
4 mA	Std.	0.70	2.48	0.05	1.08	0.50	2.53	2.25	2.38	2.34	4.54	4.26	ns
	–1	0.60	2.11	0.04	0.92	0.43	2.15	1.92	2.03	1.99	3.86	3.63	ns
6 mA	Std.	0.70	2.17	0.05	1.08	0.50	2.21	1.86	2.64	2.79	4.22	3.87	ns
	–1	0.60	1.85	0.04	0.92	0.43	1.88	1.58	2.24	2.37	3.59	3.29	ns
8 mA	Std.	0.70	2.17	0.05	1.08	0.50	2.21	1.86	2.64	2.79	4.22	3.87	ns
	–1	0.60	1.85	0.04	0.92	0.43	1.88	1.58	2.24	2.37	3.59	3.29	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-94 • Minimum and Maximum DC Input and Output Levels Applicable to Pro I/Os

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	13	16	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4	25	33	10	10
6 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	6	6	32	39	10	10
8 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	8	8	66	55	10	10
12 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12	66	55	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-95 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	13	16	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4	25	33	10	10
6 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	6	6	32	39	10	10
8 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	8	8	66	55	10	10
12 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12	66	55	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-96 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	13	16	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4	25	33	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

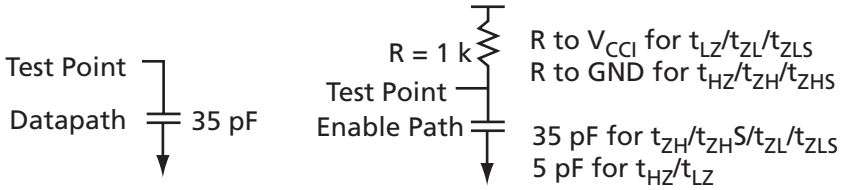


Figure 2-10 • AC Loading

Table 2-97 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.5	0.75	5

* *Measuring point = V_{trip}. See Table 2-26 on page 2-25 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-98 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.59	8.65	0.04	1.99	2.77	0.38	8.81	7.17	3.06	2.41	10.83	9.18	ns
	–1	0.50	7.36	0.03	1.69	2.36	0.33	7.50	6.10	2.61	2.05	9.21	7.81	ns
4 mA	Std.	0.59	7.40	0.04	1.99	2.77	0.38	7.53	6.26	3.39	3.02	9.55	8.27	ns
	–1	0.50	6.29	0.03	1.69	2.36	0.33	6.41	5.33	2.89	2.57	8.12	7.04	ns
6 mA	Std.	0.59	6.94	0.04	1.99	2.77	0.38	7.07	6.09	3.46	3.19	9.08	8.11	ns
	–1	0.50	5.91	0.03	1.69	2.36	0.33	6.01	5.18	2.94	2.72	7.73	6.90	ns
8 mA	Std.	0.59	6.85	0.04	1.99	2.77	0.38	6.98	6.10	3.57	3.80	8.99	8.11	ns
	–1	0.50	5.83	0.03	1.69	2.36	0.33	5.94	5.19	3.04	3.23	7.65	6.90	ns
12 mA	Std.	0.59	6.85	0.04	1.99	2.77	0.38	6.98	6.10	3.57	3.80	8.99	8.11	ns
	–1	0.50	5.83	0.03	1.69	2.36	0.33	5.94	5.19	3.04	3.23	7.65	6.90	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-99 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.59	3.55	0.04	1.99	2.77	0.38	3.62	3.22	3.05	2.51	5.63	5.23	ns
	–1	0.50	3.02	0.03	1.69	2.36	0.33	3.08	2.74	2.60	2.14	4.79	4.45	ns
4 mA	Std.	0.59	3.03	0.04	1.99	2.77	0.38	3.08	2.64	3.38	3.13	5.10	4.65	ns
	–1	0.50	2.58	0.03	1.69	2.36	0.33	2.62	2.25	2.87	2.66	4.34	3.96	ns
6 mA	Std.	0.59	2.93	0.04	1.99	2.77	0.38	2.98	2.53	3.45	3.30	4.99	4.54	ns
	–1	0.50	2.49	0.03	1.69	2.36	0.33	2.54	2.15	2.93	2.81	4.25	3.86	ns
8 mA	Std.	0.59	2.90	0.04	1.99	2.77	0.38	2.95	2.39	3.57	3.94	4.96	4.41	ns
	–1	0.50	2.46	0.03	1.69	2.36	0.33	2.51	2.04	3.03	3.35	4.22	3.75	ns
12 mA	Std.	0.59	2.90	0.04	1.99	2.77	0.38	2.95	2.39	3.57	3.94	4.96	4.41	ns
	–1	0.50	2.46	0.03	1.69	2.36	0.33	2.51	2.04	3.03	3.35	4.22	3.75	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-100 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.54	8.00	0.04	1.18	0.38	8.15	7.01	3.06	2.38	10.16	9.02	ns
	–1	0.46	6.80	0.03	1.00	0.33	6.93	5.96	2.60	2.02	8.64	7.68	ns
4 mA	Std.	0.54	6.91	0.04	1.18	0.38	7.04	6.21	3.37	2.94	9.05	8.22	ns
	–1	0.46	5.88	0.03	1.00	0.33	5.99	5.28	2.87	2.50	7.70	7.00	ns
6 mA	Std.	0.54	6.51	0.04	1.18	0.38	6.63	6.05	3.45	3.09	8.64	8.06	ns
	–1	0.46	5.54	0.03	1.00	0.33	5.64	5.15	2.93	2.63	7.35	6.86	ns
8 mA	Std.	0.54	6.41	0.04	1.18	0.38	6.53	6.11	3.56	3.64	8.54	8.12	ns
	–1	0.46	5.45	0.03	1.00	0.33	5.56	5.20	3.03	3.10	7.27	6.91	ns
12 mA	Std.	0.54	6.41	0.04	1.18	0.38	6.53	6.11	3.56	3.64	8.54	8.12	ns
	–1	0.46	5.45	0.03	1.00	0.33	5.56	5.20	3.03	3.10	7.27	6.91	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-101 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.54	3.60	0.04	1.10	0.38	3.66	3.52	2.49	1.49	5.68	5.53	ns
	–1	0.46	3.06	0.03	0.93	0.33	3.12	3.00	2.12	1.27	4.83	4.71	ns
4 mA	Std.	0.54	2.81	0.04	1.10	0.38	2.87	2.64	2.90	2.55	4.88	4.65	ns
	–1	0.46	2.39	0.03	0.93	0.33	2.44	2.25	2.47	2.17	4.15	3.96	ns
6 mA	Std.	0.54	2.47	0.04	1.10	0.38	2.51	2.21	3.18	3.04	4.53	4.22	ns
	–1	0.46	2.10	0.03	0.93	0.33	2.14	1.88	2.70	2.59	3.85	3.59	ns
8 mA	Std.	0.54	2.40	0.04	1.10	0.38	2.45	2.13	3.24	3.17	4.46	4.14	ns
	–1	0.46	2.04	0.03	0.93	0.33	2.08	1.81	2.76	2.70	3.79	3.52	ns
12 mA	Std.	0.54	2.39	0.04	1.10	0.38	2.44	2.04	3.33	3.67	4.45	4.05	ns
	–1	0.46	2.04	0.03	0.93	0.33	2.08	1.73	2.83	3.12	3.79	3.45	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-102 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.54	7.32	0.04	1.17	0.38	7.45	6.38	2.44	2.18	9.46	8.40	ns
	–1	0.46	6.22	0.03	0.99	0.33	6.34	5.43	2.08	1.86	8.05	7.14	ns
4 mA	Std.	0.54	6.29	0.04	1.17	0.38	6.40	5.65	2.73	2.70	8.42	7.67	ns
	–1	0.46	5.35	0.03	0.99	0.33	5.45	4.81	2.33	2.29	7.16	6.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-103 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.54	2.90	0.04	1.28	0.38	2.95	2.63	2.44	2.29	4.97	4.64	ns
	–1	0.46	2.47	0.03	1.09	0.33	2.51	2.24	2.07	1.95	4.23	3.95	ns
4 mA	Std.	0.54	2.52	0.04	1.28	0.38	2.57	2.14	2.73	2.82	4.58	4.15	ns
	–1	0.46	2.15	0.03	1.09	0.33	2.19	1.82	2.32	2.40	3.90	3.53	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

1.2 V DC Core Voltage

Table 2-104 • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.77	8.65	0.05	1.99	2.77	0.50	8.81	7.17	3.06	2.41	10.83	9.18	ns
	–1	0.66	7.36	0.04	1.69	2.36	0.43	7.50	6.10	2.61	2.05	9.21	7.81	ns
4 mA	Std.	0.77	7.40	0.05	1.99	2.77	0.50	7.53	6.26	3.39	3.02	9.55	8.27	ns
	–1	0.66	6.29	0.04	1.69	2.36	0.43	6.41	5.33	2.89	2.57	8.12	7.04	ns
6 mA	Std.	0.77	6.94	0.05	1.99	2.77	0.50	7.07	6.09	3.46	3.19	9.08	8.11	ns
	–1	0.66	5.91	0.04	1.69	2.36	0.43	6.01	5.18	2.94	2.72	7.73	6.90	ns
8 mA	Std.	0.77	6.85	0.05	1.99	2.77	0.50	6.98	6.10	3.57	3.80	8.99	8.11	ns
	–1	0.66	5.83	0.04	1.69	2.36	0.43	5.94	5.19	3.04	3.23	7.65	6.90	ns
12 mA	Std.	0.77	6.85	0.05	1.99	2.77	0.50	6.98	6.10	3.57	3.80	8.99	8.11	ns
	–1	0.66	5.83	0.04	1.69	2.36	0.43	5.94	5.19	3.04	3.23	7.65	6.90	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-105 • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.77	3.55	0.05	1.99	2.77	0.50	3.62	3.22	3.05	2.51	5.63	5.23	ns
	–1	0.66	3.02	0.04	1.69	2.36	0.43	3.08	2.74	2.60	2.14	4.79	4.45	ns
4 mA	Std.	0.77	3.03	0.05	1.99	2.77	0.50	3.08	2.64	3.38	3.13	5.10	4.65	ns
	–1	0.66	2.58	0.04	1.69	2.36	0.43	2.62	2.25	2.87	2.66	4.34	3.96	ns
6 mA	Std.	0.77	2.93	0.05	1.99	2.77	0.50	2.98	2.53	3.45	3.30	4.99	4.54	ns
	–1	0.66	2.49	0.04	1.69	2.36	0.43	2.54	2.15	2.93	2.81	4.25	3.86	ns
8 mA	Std.	0.77	2.90	0.05	1.99	2.77	0.50	2.95	2.39	3.57	3.94	4.96	4.41	ns
	–1	0.66	2.46	0.04	1.69	2.36	0.43	2.51	2.04	3.03	3.35	4.22	3.75	ns
12 mA	Std.	0.77	2.90	0.05	1.99	2.77	0.50	2.95	2.39	3.57	3.94	4.96	4.41	ns
	–1	0.66	2.46	0.04	1.69	2.36	0.43	2.51	2.04	3.03	3.35	4.22	3.75	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-106 • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	8.00	0.05	1.18	0.50	8.15	7.01	3.06	2.38	10.16	9.02	ns
	–1	0.60	6.80	0.04	1.00	0.43	6.93	5.96	2.60	2.02	8.64	7.68	ns
4 mA	Std.	0.70	6.91	0.05	1.18	0.50	7.04	6.21	3.37	2.94	9.05	8.22	ns
	–1	0.60	5.88	0.04	1.00	0.43	5.99	5.28	2.87	2.50	7.70	7.00	ns
6 mA	Std.	0.70	6.51	0.05	1.18	0.50	6.63	6.05	3.45	3.09	8.64	8.06	ns
	–1	0.60	5.54	0.04	1.00	0.43	5.64	5.15	2.93	2.63	7.35	6.86	ns
8 mA	Std.	0.70	6.41	0.05	1.18	0.50	6.53	6.11	3.56	3.64	8.54	8.12	ns
	–1	0.60	5.45	0.04	1.00	0.43	5.56	5.20	3.03	3.10	7.27	6.91	ns
12 mA	Std.	0.70	6.41	0.05	1.18	0.50	6.53	6.11	3.56	3.64	8.54	8.12	ns
	–1	0.60	5.45	0.04	1.00	0.43	5.56	5.20	3.03	3.10	7.27	6.91	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-107 • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	3.26	0.05	1.30	0.50	3.32	3.11	3.05	2.49	5.33	5.12	ns
	–1	0.60	2.77	0.04	1.10	0.43	2.82	2.64	2.59	2.12	4.53	4.36	ns
4 mA	Std.	0.70	2.84	0.05	1.30	0.50	2.89	2.57	3.37	3.06	4.90	4.59	ns
	–1	0.60	2.41	0.04	1.10	0.43	2.46	2.19	2.86	2.60	4.17	3.90	ns
6 mA	Std.	0.70	2.76	0.05	1.30	0.50	2.81	2.47	3.44	3.21	4.82	4.48	ns
	–1	0.60	2.35	0.04	1.10	0.43	2.39	2.10	2.92	2.73	4.10	3.81	ns
8 mA	Std.	0.70	2.74	0.05	1.30	0.50	2.79	2.36	3.55	3.78	4.80	4.37	ns
	–1	0.60	2.33	0.04	1.10	0.43	2.37	2.01	3.02	3.22	4.08	3.72	ns
12 mA	Std.	0.70	2.74	0.05	1.30	0.50	2.79	2.36	3.55	3.78	4.80	4.37	ns
	–1	0.60	2.33	0.04	1.10	0.43	2.37	2.01	3.02	3.22	4.08	3.72	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-108 • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	7.32	0.05	1.17	0.50	7.45	6.38	2.44	2.18	9.46	8.40	ns
	–1	0.60	6.22	0.04	0.99	0.43	6.34	5.43	2.08	1.86	8.05	7.14	ns
4 mA	Std.	0.70	6.29	0.05	1.17	0.50	6.40	5.65	2.73	2.70	8.42	7.67	ns
	–1	0.60	5.35	0.04	0.99	0.43	5.45	4.81	2.33	2.29	7.16	6.52	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-109 • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	2.90	0.05	1.28	0.50	2.95	2.63	2.44	2.29	4.97	4.64	ns
	–1	0.60	2.47	0.04	1.09	0.43	2.51	2.24	2.07	1.95	4.23	3.95	ns
4 mA	Std.	0.70	2.52	0.05	1.28	0.50	2.57	2.14	2.73	2.82	4.58	4.15	ns
	–1	0.60	2.15	0.04	1.09	0.43	2.19	1.82	2.32	2.40	3.90	3.53	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

Table 2-110 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

1.2 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}[1]	I_{OSL}[1]	I_{IL}[2]	I_{IH}[2]
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA	Max., mA	µA	µA
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.26	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	TBD	TBD	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-111 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

1.2 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}[1]	I_{OSL}[1]	I_{IL}[2]	I_{IH}[2]
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA	Max., mA	µA	µA
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.26	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	TBD	TBD	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-112 • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks

1.2 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}[1]	I_{OSL}[1]	I_{IL}[2]	I_{IH}[2]
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA	Max., mA	µA	µA
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.26	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	TBD	TBD	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

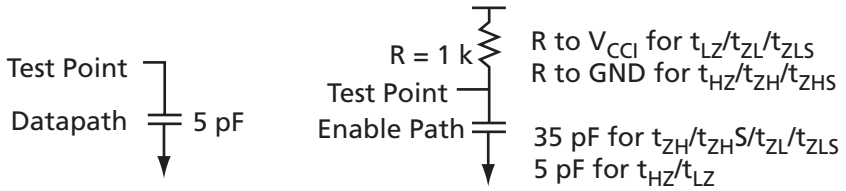


Figure 2-11 • **AC Loading**

Table 2-113 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.2	0.6	5

* *Measuring point = V_{trip}. See Table 2-26 on page 2-25 for a complete table of trip points.*

Timing Characteristics

1.2 V DC Core Voltage

Table 2-114 • 1.2 V LVCMOS Low Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.77	11.80	0.05	2.38	3.52	0.50	10.97	8.61	4.79	4.38	12.91	10.55	ns
	–1	0.66	10.04	0.04	2.02	2.99	0.43	9.33	7.32	4.08	3.72	10.98	8.97	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-115 • 1.2 V LVCMOS High Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Pro I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.77	4.84	0.05	2.38	3.52	0.50	4.50	3.96	4.78	4.51	6.44	5.90	ns
	–1	0.66	4.12	0.04	2.02	2.99	0.43	3.83	3.37	4.06	3.84	5.48	5.02	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-116 • 1.2 V LVCMOS High Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.14 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	8.77	0.05	1.82	0.50	6.17	5.45	2.80	2.77	8.11	7.39	ns
	–1	0.60	7.46	0.04	1.55	0.43	5.25	4.63	2.39	2.35	6.90	6.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-117 • 1.2 V LVCMOS High Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.14 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	3.73	0.05	1.82	0.50	2.48	2.06	2.80	2.89	4.42	4.00	ns
	–1	0.60	3.17	0.04	1.55	0.43	2.11	1.76	2.38	2.46	3.76	3.41	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-118 • 1.2 V LVCMOS High Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.14 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	9.67	0.05	1.83	0.50	6.78	5.99	4.08	4.57	8.72	7.93	ns
	–1	0.60	8.23	0.04	1.56	0.43	5.77	5.09	3.47	3.88	7.42	6.74	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-119 • 1.2 V LVCMOS High Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.14 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.70	4.17	0.05	1.83	0.50	2.79	2.48	4.23	4.55	4.73	4.42	ns
	–1	0.60	3.54	0.04	1.56	0.43	2.37	2.11	3.60	3.87	4.02	3.76	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-120 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA	Max, mA[1]	Max, mA[1]	µA[2]	µA[2]
Per PCI specification	Per PCI curves										10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the database; Actel loadings for enable path characterization are described in Figure 2-12.

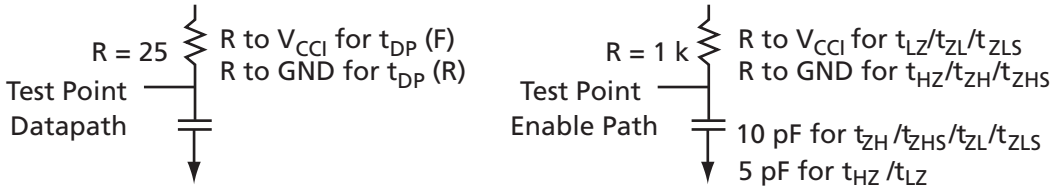


Figure 2-12 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; Actel loading for tristate is described in Table 2-121.

Table 2-121 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	0.285 * V_{CCI} for $t_{DP(R)}$ 0.615 * V_{CCI} for $t_{DP(F)}$	10

** Measuring point = V_{trip}. See Table 2-26 on page 2-25 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-122 • 3.3 V PCI/PCI-X – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	2.52	0.04	2.47	3.33	0.38	2.57	1.80	2.95	3.25	4.58	3.81	ns
–1	0.50	2.15	0.03	2.10	2.84	0.33	2.19	1.53	2.51	2.77	3.90	3.24	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-123 • 3.3 V PCI/PCI-X – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.54	2.41	0.04	0.78	0.38	2.46	1.76	2.89	3.22	4.47	3.77	ns	0.54
–1	0.46	2.05	0.03	0.66	0.33	2.09	1.49	2.46	2.74	3.80	3.21	ns	0.46

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-124 • 3.3 V PCI/PCI-X – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.54	2.08	0.04	0.77	0.38	2.12	1.53	2.51	2.90	4.13	3.55	ns	0.54
–1	0.46	1.77	0.03	0.65	0.33	1.80	1.31	2.14	2.47	3.51	3.02	ns	0.46

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-125 • 3.3 V PCI/PCI-X – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	2.52	0.05	2.47	3.33	0.50	2.57	1.80	2.95	3.25	4.58	3.81	ns
–1	0.66	2.15	0.04	2.10	2.84	0.43	2.19	1.53	2.51	2.77	3.90	3.24	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-126 • 3.3 V PCI/PCI-X – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.70	2.41	0.05	0.78	0.50	2.46	1.76	2.89	3.22	4.47	3.77	0.73	ns
–1	0.60	2.05	0.04	0.66	0.43	2.09	1.49	2.46	2.74	3.80	3.21	0.62	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-127 • 3.3 V PCI/PCI-X – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.70	2.08	0.05	0.77	0.50	2.12	1.53	2.51	2.90	4.13	3.55	0.73	ns
–1	0.60	1.77	0.04	0.65	0.43	1.80	1.31	2.14	2.47	3.51	3.02	0.62	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Voltage-Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 3.3 V.

Table 2-128 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
25 mA[3]	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25	268	181	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

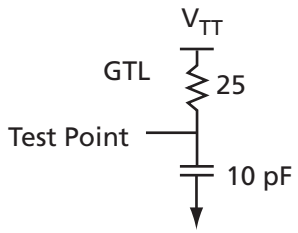


Figure 2-13 • AC Loading

Table 2-129 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.05	V_{REF} + 0.05	0.8	0.8	1.2	10

* *Measuring point = V_{trip}. See Table 2-15 on page 2-12 for a complete table of trip points.*

Timing Characteristics

Table 2-130 • 3.3 V GTL – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 3.0 V V_{REF} = 0.8 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	1.87	0.04	2.12	0.38	1.83	1.87			3.85	3.88	ns
–1	0.50	1.59	0.03	1.80	0.33	1.56	1.59			3.27	3.30	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-131 • 3.3 V GTL – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V,
Worst-Case V_{CCI} = 3.0 V V_{REF} = 0.8 V
Applicable to Pro I/Os

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	1.87	0.05	2.12	0.50	1.83	1.87			3.85	3.88	ns
–1	0.66	1.59	0.04	1.80	0.43	1.56	1.59			3.27	3.30	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 2.5 V

Table 2-132 • Minimum and Maximum DC Input and Output Levels

2.5 GTL	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
25 mA[3]	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	2.7	0.4	–	25	25	169	124	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

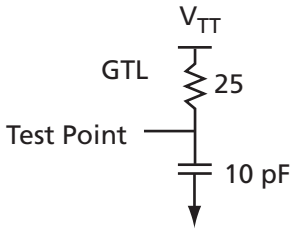


Figure 2-14 • AC Loading

Table 2-133 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.05	V_{REF} + 0.05	0.8	0.8	1.2	10

** Measuring point = V_{trip}. See Table 2-15 on page 2-12 for a complete table of trip points.*

Timing Characteristics

Table 2-134 • 2.5 V GTL – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 3.0 V V_{REF} = 0.8 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	1.92	0.04	2.05	0.38	1.95	1.92			3.96	3.93	ns
–1	0.50	1.63	0.03	1.75	0.33	1.66	1.63			3.37	3.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-135 • 2.5 V GTL – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V,
Worst-Case V_{CCI} = 3.0 V V_{REF} = 0.8 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	1.92	0.05	2.05	0.50	1.95	1.92			3.96	3.93	ns
–1	0.66	1.63	0.04	1.75	0.43	1.66	1.63			3.37	3.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 3.3 V

Table 2-136 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL+	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
35 mA	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	35	35	268	181	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

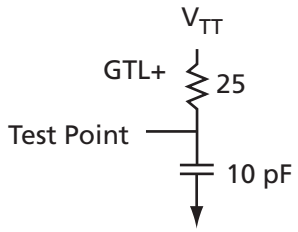


Figure 2-15 • AC Loading

Table 2-137 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	1.0	1.0	1.5	10

* *Measuring point = V_{trip}. See Table 2-15 on page 2-12 for a complete table of trip points.*

Timing Characteristics

Table 2-138 • **3.3 V GTL+ – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 3.0 V V_{REF} = 1.0 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	1.85	0.04	2.12	0.38	1.88	1.85			3.90	3.86	ns
–1	0.50	1.57	0.03	1.80	0.33	1.60	1.57			3.31	3.29	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-139 • **3.3 V GTL+ – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V,
Worst-Case V_{CCI} = 3.0 V V_{REF} = 1.0 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	1.85	0.05	2.12	0.50	1.88	1.85			3.90	3.86	ns
–1	0.66	1.57	0.04	1.80	0.43	1.60	1.57			3.31	3.29	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

Table 2-140 • Minimum and Maximum DC Input and Output Levels

2.5 V GTL+	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
33 mA	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	2.7	0.6	–	33	33	169	124	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

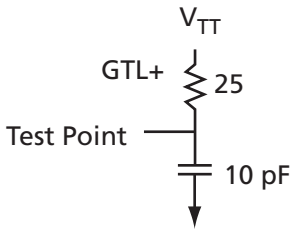


Figure 2-16 • AC Loading

Table 2-141 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	1.0	1.0	1.5	10

* *Measuring point = V_{trip}. See Table 2-15 on page 2-12 for a complete table of trip points.*

Timing Characteristics

Table 2-142 • 2.5 V GTL+ – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 2.3 V V_{REF} = 1.0 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	1.99	0.04	2.05	0.38	2.02	1.89			4.03	3.90	ns
–1	0.50	1.69	0.03	1.75	0.33	1.72	1.61			3.43	3.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-15 on page 2-12 for derating values.

Table 2-143 • 2.5 V GTL+ – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V,
Worst-Case V_{CCI} = 2.3 V V_{REF} = 1.0 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	1.99	0.05	2.05	0.50	2.02	1.89			4.03	3.90	ns
–1	0.66	1.69	0.04	1.75	0.43	1.72	1.61			3.43	3.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-15 on page 2-12 for derating values.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-144 • Minimum and Maximum DC Input and Output Levels

HSTL Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
8 mA	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575	0.4	V_{CCI} – 0.4	8	8	32	39	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

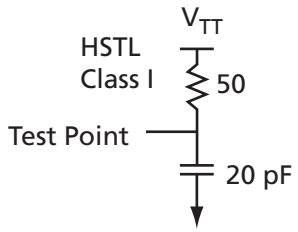


Figure 2-17 • AC Loading

Table 2-145 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	0.75	0.75	0.75	20

** Measuring point = V_{trip}. See Table 2-15 on page 2-12 for a complete table of trip points.*

Timing Characteristics

Table 2-146 • HSTL Class I – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 1.4 V V_{REF} = 0.75 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	2.86	0.04	2.50	0.38	2.91	2.83			4.93	4.84	ns
–1	0.50	2.43	0.03	2.12	0.33	2.48	2.41			4.19	4.12	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-147 • HSTL Class I – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V,
Worst-Case V_{CCI} = 1.4 V V_{REF} = 0.75 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	2.86	0.05	2.50	0.50	2.91	2.83			4.93	4.84	ns
–1	0.66	2.43	0.04	2.12	0.43	2.48	2.41			4.19	4.12	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-148 • Minimum and Maximum DC Input and Output Levels

HSTL Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
15 mA[3]	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	1.575	0.4	V_{CCI} – 0.4	15	15	66	55	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

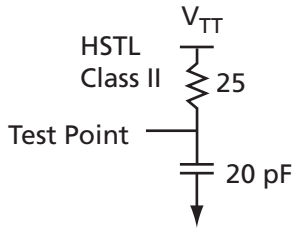


Figure 2-18 • AC Loading

Table 2-149 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	0.75	0.75	0.75	20

* *Measuring point = V_{trip}. See Table 2-15 on page 2-12 for a complete table of trip points.*

Timing Characteristics

Table 2-150 • **HSTL Class II – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 1.4 V V_{REF} = 0.75 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	2.72	0.04	2.50	0.38	2.77	2.44			4.78	4.45	ns
–1	0.50	2.32	0.03	2.12	0.33	2.36	2.08			4.07	3.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-151 • **HSTL Class II – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V,
Worst-Case V_{CCI} = 1.4 V V_{REF} = 0.75 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	2.72	0.05	2.50	0.50	2.77	2.44			4.78	4.45	ns
–1	0.66	2.32	0.04	2.12	0.43	2.36	2.08			4.07	3.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-152 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
15 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	2.7	0.54	V_{CCI} – 0.62	15	15	83	87	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

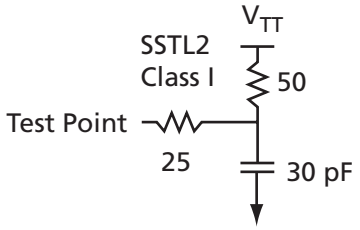


Figure 2-19 • AC Loading

Table 2-153 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.25	1.25	1.25	30

* *Measuring point = V_{trip}. See Table 2-15 on page 2-12 for a complete table of trip points.*

Timing Characteristics

Table 2-154 • SSTL2 Class I – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 2.3 V V_{REF} = 1.25 V
Applicable to Pro I/Os

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	1.91	0.04	1.89	0.38	1.95	1.66			1.95	1.66	ns
–1	0.50	1.63	0.03	1.61	0.33	1.66	1.41			1.66	1.41	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-155 • SSTL2 Class I – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V,
Worst-Case V_{CCI} = 2.3 V V_{REF} = 1.25 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	1.91	0.05	1.89	0.50	1.95	1.66			1.95	1.66	ns
–1	0.66	1.63	0.04	1.61	0.43	1.66	1.41			1.66	1.41	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-156 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
18 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	2.7	0.35	V_{CCI} – 0.43	18	18	169	124	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

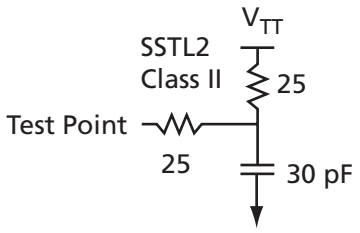


Figure 2-20 • AC Loading

Table 2-157 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.25	1.25	1.25	30

** Measuring point = V_{trip}. See Table 2-15 on page 2-12 for a complete table of trip points.*

Timing Characteristics

Table 2-158 • SSTL2 Class II – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 2.3 V V_{REF} = 1.25 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	1.95	0.04	1.89	0.38	1.99	1.59			1.99	1.59	ns
–1	0.50	1.66	0.03	1.61	0.33	1.69	1.36			1.69	1.36	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-159 • SSTL2 Class II – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V,
Worst-Case V_{CCI} = 2.3 V V_{REF} = 1.25 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	1.95	0.05	1.89	0.50	1.99	1.59			1.99	1.59	ns
–1	0.66	1.66	0.04	1.61	0.43	1.69	1.36			1.69	1.36	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-160 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
14 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCI} – 1.1	14	14	51	54	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

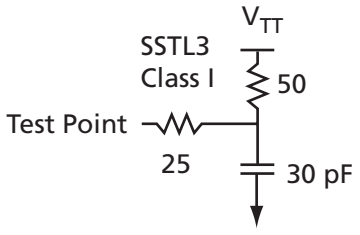


Figure 2-21 • AC Loading

Table 2-161 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.5	1.5	1.485	30

* *Measuring point = V_{trip}. See Table 2-15 on page 2-12 for a complete table of trip points.*

Timing Characteristics

Table 2-162 • SSTL3 Class I – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 3.0 V V_{REF} = 1.5 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	2.08	0.04	1.81	0.38	2.11	1.65			2.11	1.65	ns
–1	0.50	1.77	0.03	1.54	0.33	1.80	1.41			1.80	1.41	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-163 • SSTL3 Class I – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V,
Worst-Case V_{CCI} = 3.0 V V_{REF} = 1.5 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	2.08	0.05	1.81	0.50	2.11	1.65			2.11	1.65	ns
–1	0.66	1.77	0.04	1.54	0.43	1.80	1.41			1.80	1.41	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-164 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
21 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCI} – 0.9	21	21	103	109	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

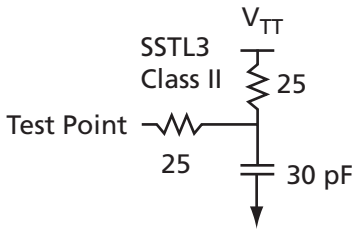


Figure 2-22 • **AC Loading**

Table 2-165 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	V_{TT} (typ.) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.5	1.5	1.485	30

** Measuring point = V_{trip}. See Table 2-15 on page 2-12 for a complete table of trip points.*

Timing Characteristics

Table 2-166 • **SSTL3 Class II – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V,
Worst-Case V_{CCI} = 3.0 V V_{REF} = 1.5 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.59	1.86	0.04	1.81	0.38	1.89	1.50			1.89	1.50	ns
–1	0.50	1.58	0.03	1.54	0.33	1.61	1.28			1.61	1.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-167 • **SSTL3 Class II – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V,
Worst-Case V_{CCI} = 3.0 V V_{REF} = 1.5 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.77	1.86	0.05	1.81	0.50	1.89	1.50			1.89	1.50	ns
–1	0.66	1.58	0.04	1.54	0.43	1.61	1.28			1.61	1.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-23. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

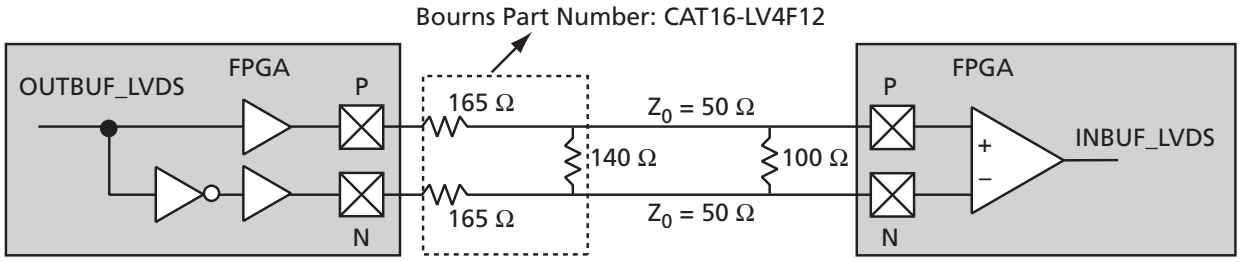


Figure 2-23 • **LVDS Circuit Diagram and Board-Level Implementation**

Table 2-168 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
V_{CCI}	Supply Voltage	2.375	2.5	2.625	V
V_{OL}	Output Low Voltage	0.9	1.075	1.25	V
V_{OH}	Output High Voltage	1.25	1.425	1.6	V
I_{OL} [4]	Output Lower Current	0.65	0.91	1.16	mA
I_{OH} [4]	Output High Current	0.65	0.91	1.16	mA
V_I	Input Voltage	0		2.925	V
I_{IH} [3]	Input High Leakage Current			10	µA
I_{IL} [3]	Input Low Leakage Current			10	µA
V_{ODIFF}	Differential Output Voltage	250	350	450	mV
V_{OCM}	Output Common Mode Voltage	1.125	1.25	1.375	V
V_{ICM}	Input Common Mode Voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input Differential Voltage	100	350		mV

Notes:

1. *± 5%*
2. *Differential input voltage = ±350 mV.*
3. *Currents are measured at 85°C junction temperature.*
4. *I_{OL}/I_{OH} is defined by V_{ODIFF}/(Resistor Network).*

Table 2-169 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)
1.075	1.325	Cross point

* *Measuring point = V_{trip}. See Table 2-26 on page 2-25 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-170 • LVDS – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.59	1.65	0.04	2.18	ns
–1	0.50	1.40	0.03	1.85	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-171 • LVDS – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.54	1.65	0.04	1.44	ns
–1	0.46	1.40	0.03	1.23	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-172 • LVDS – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.77	1.68	0.05	2.18	ns
–1	0.66	1.43	0.04	1.85	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-173 • LVDS – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.70	1.65	0.05	1.44	ns
–1	0.60	1.40	0.04	1.23	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Actel LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-24. The input and output buffer delays are available in the LVDS section in Table 2-168 on page 2-91.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

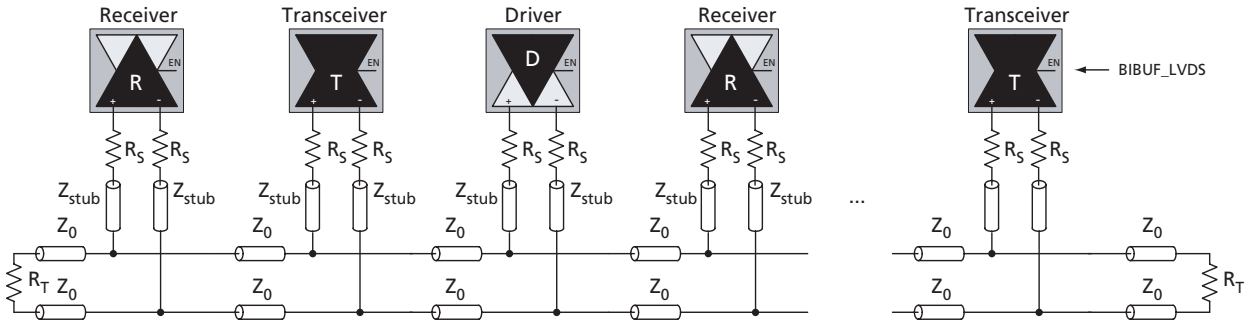


Figure 2-24 • **B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-25. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

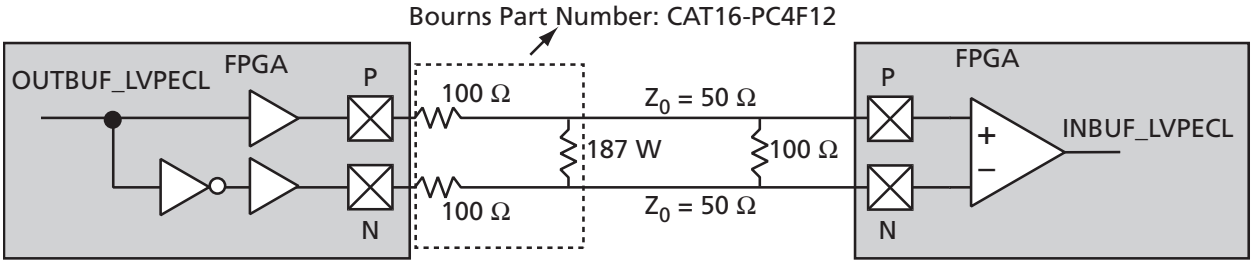


Figure 2-25 • **LVPECL Circuit Diagram and Board-Level Implementation**

Table 2-174 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
V_{CCI}	Supply Voltage	3.0		3.3		3.6		V
V_{OL}	Output LOW Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{OH}	Output HIGH Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{IL}, V_{IH}	Input LOW, Input HIGH Voltages	0	3.3	0	3.6	0	3.9	V
V_{ODIFF}	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V_{OCM}	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V_{ICM}	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V_{IDIFF}	Input Differential Voltage	300		300		300		mV

Table 2-175 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)
1.64	1.94	Cross point

* *Measuring point = V_{trip}. See Table 2-26 on page 2-25 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-176 • LVPECL – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.59	1.64	0.04	1.97	ns
–1	0.50	1.40	0.03	1.67	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-177 • LVPECL – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.54	1.62	0.04	1.26	ns
–1	0.46	1.38	0.03	1.08	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-178 • LVPECL – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Pro I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.77	1.62	0.05	1.97	ns
–1	0.66	1.37	0.04	1.67	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-179 • LVPECL – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.70	1.62	0.05	1.26	ns
–1	0.60	1.38	0.04	1.08	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

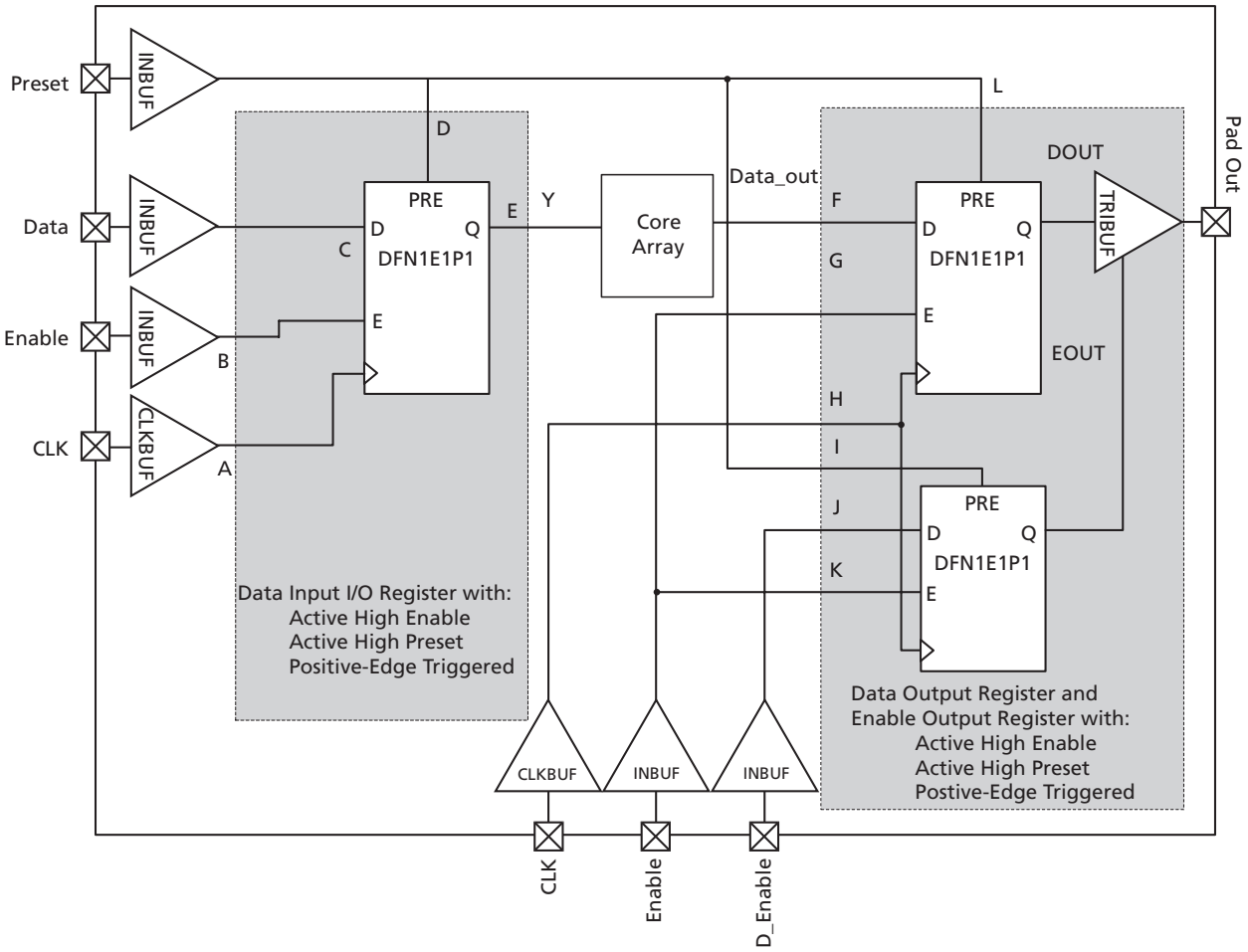


Figure 2-26 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Table 2-180 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

* *See Figure 2-26 on page 2-96 for more information.*

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

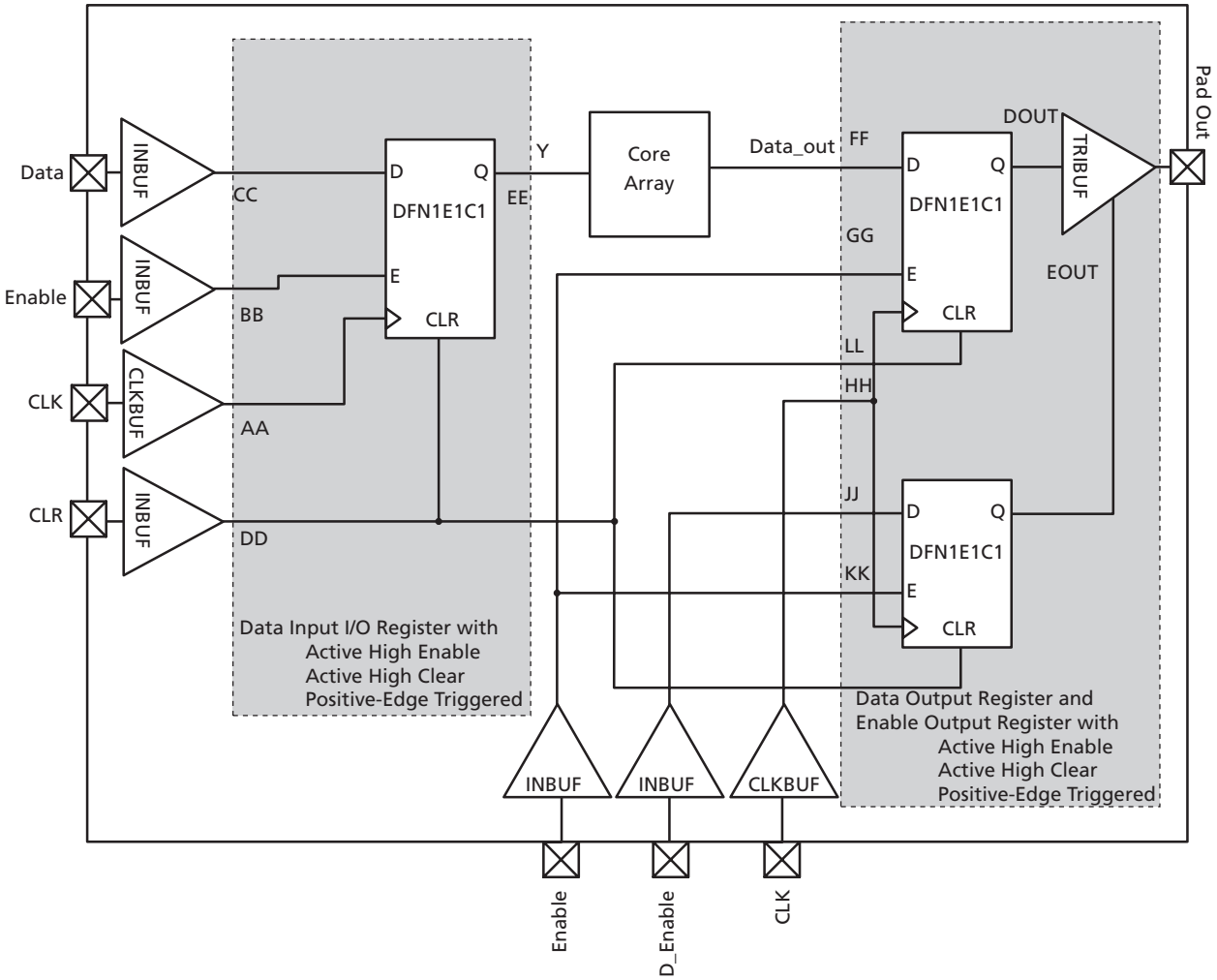


Figure 2-27 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Table 2-181 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

* *See Figure 2-27 on page 2-98 for more information.*

Input Register

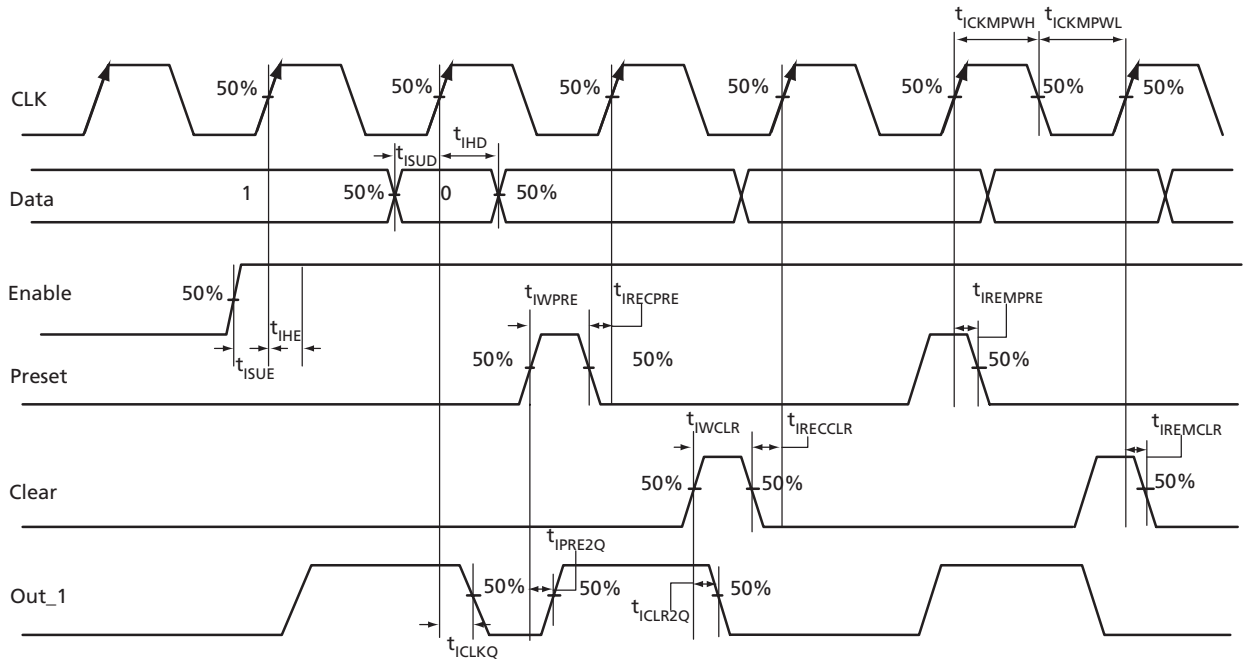


Figure 2-28 • **Input Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-182 • Input Data Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.29	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.27	0.31	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.38	0.45	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.46	0.54	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.46	0.54	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.23	0.27	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.23	0.27	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	0.36	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-183 • Input Data Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.32	0.37	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.35	0.41	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.50	0.58	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.60	0.71	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.60	0.71	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.30	0.35	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.30	0.35	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	0.36	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Output Register

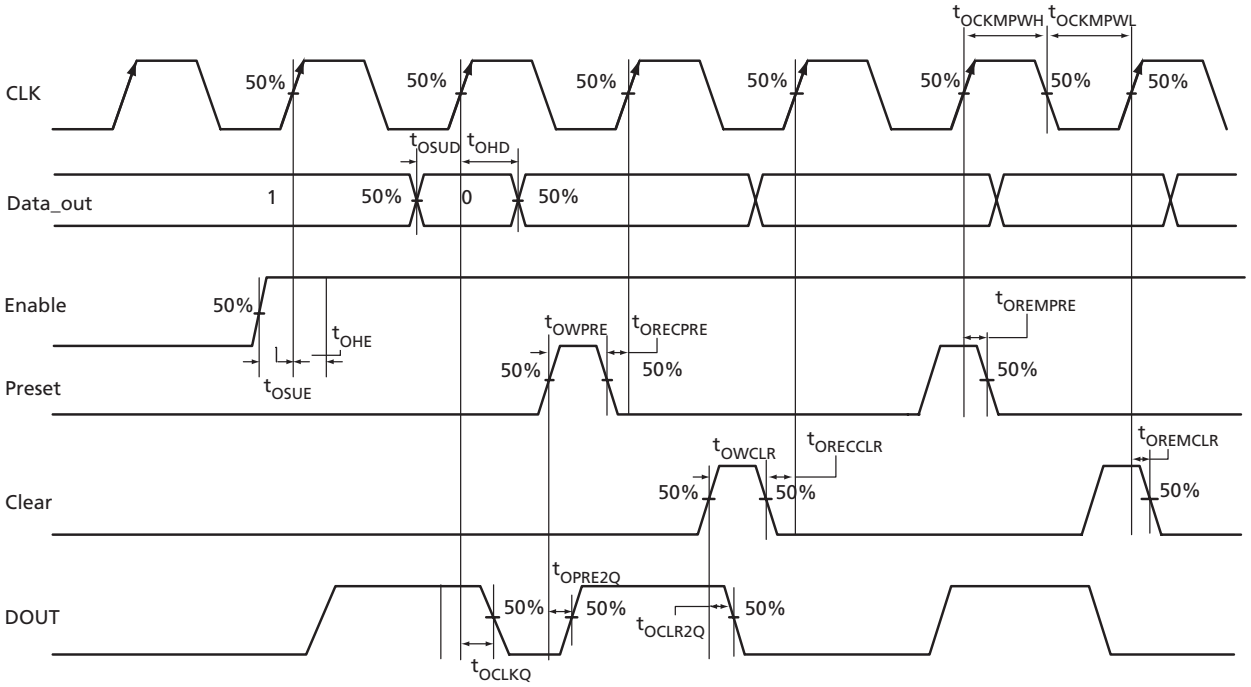


Figure 2-29 • **Output Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-184 • Output Data Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.60	0.71	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.32	0.37	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.45	0.53	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.82	0.96	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.82	0.96	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.23	0.27	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.23	0.27	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	0.22	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	0.22	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	0.36	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-185 • Output Data Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.78	0.92	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.42	0.49	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.58	0.69	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.07	1.26	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.07	1.26	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.30	0.35	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.30	0.35	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	0.22	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	0.22	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	0.36	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Output Enable Register

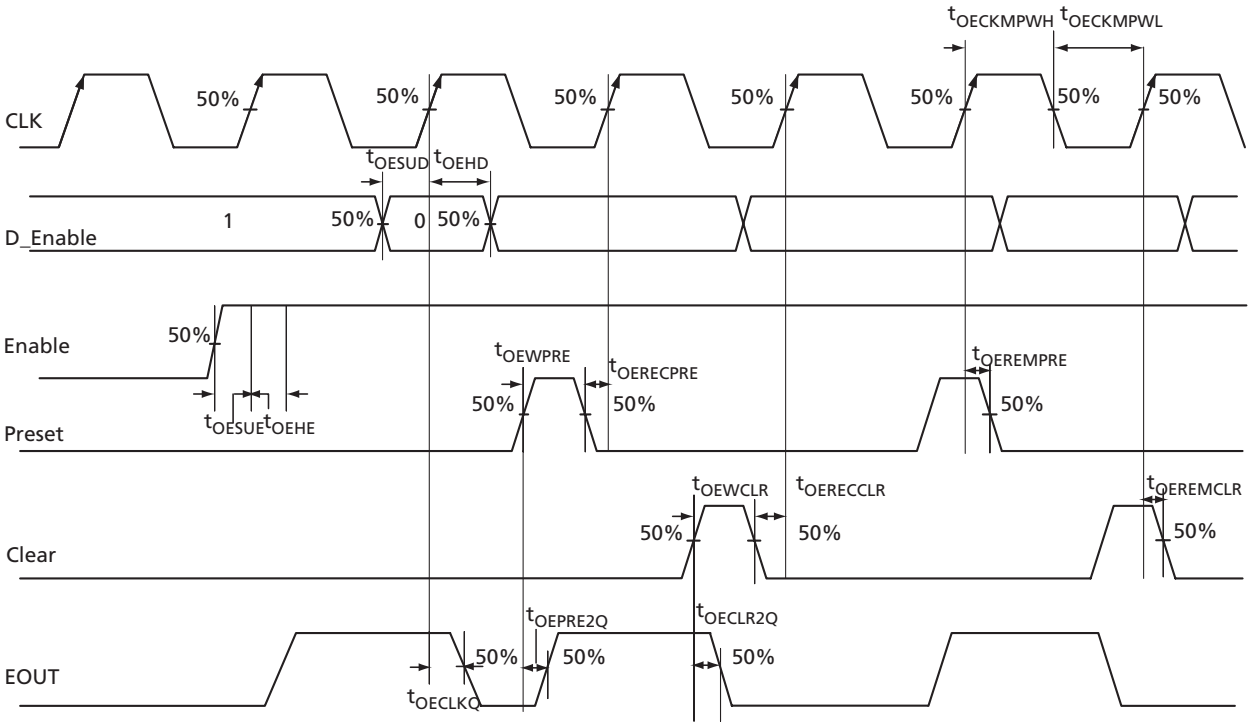


Figure 2-30 • **Output Enable Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-186 • Output Enable Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.45	0.53	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.32	0.37	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.52	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.68	0.80	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.68	0.80	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.23	0.27	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.23	0.27	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-187 • Output Enable Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.59	0.70	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.42	0.49	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.58	0.68	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.89	1.04	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.89	1.04	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.30	0.35	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.30	0.35	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	0.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

DDR Module Specifications

Input DDR Module

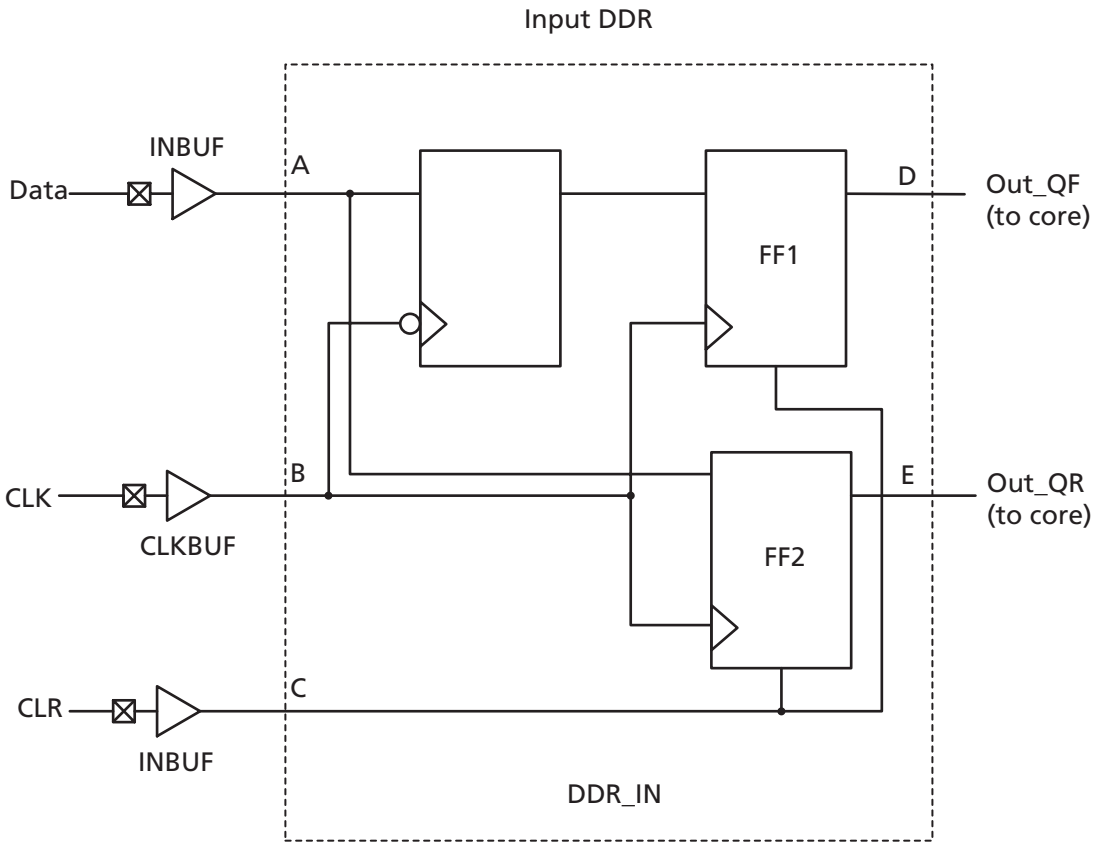


***Figure 2-31* • Input DDR Timing Model**

***Table 2-188* • Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

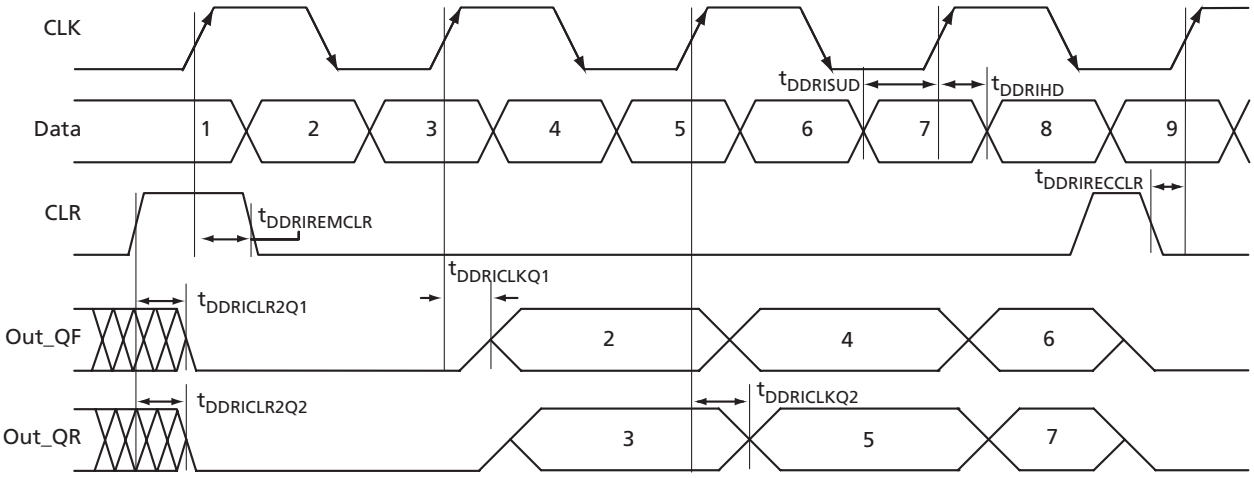


Figure 2-32 • **Input DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-189 • **Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.28	0.33	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.40	0.47	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (fall)	0.29	0.34	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (rise)	0.25	0.29	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (fall)	0.00	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (rise)	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.47	0.55	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.58	0.68	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.23	0.27	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.18	0.22	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	0.36	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	0.32	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR			MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-190 • Input DDR Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.43	0.37	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.61	0.52	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (fall)	0.44	0.38	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (rise)	0.39	0.33	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (fall)	0.00	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (rise)	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.73	0.62	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.89	0.76	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.35	0.30	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.22	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.36	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.32	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	TBD	TBD	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Output DDR Module

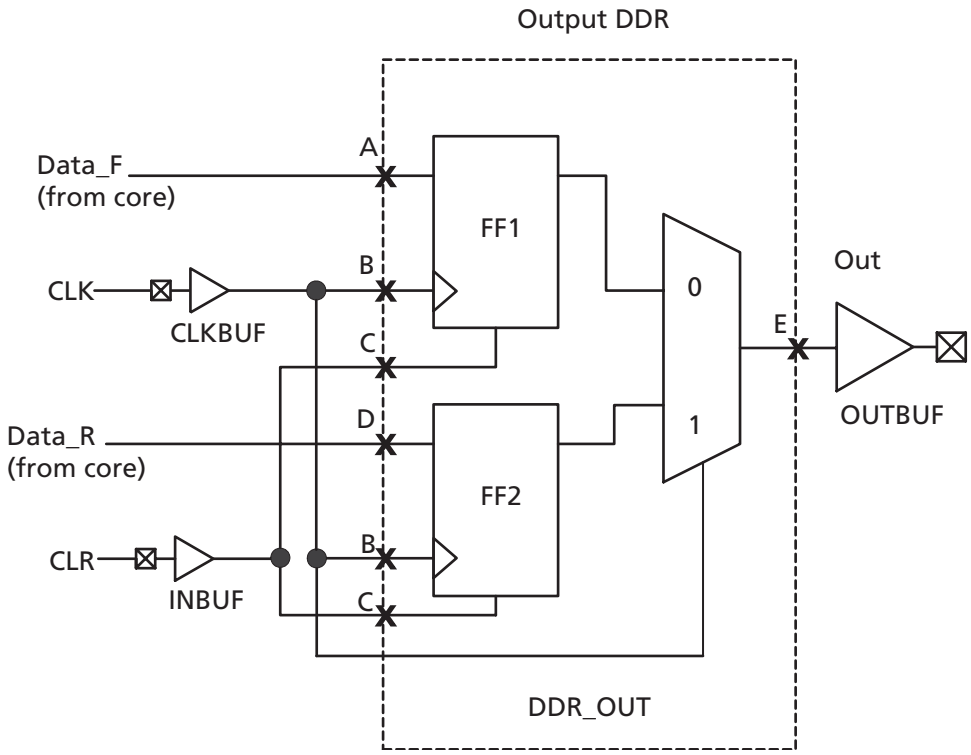


Figure 2-33 • **Output DDR Timing Model**

Table 2-191 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

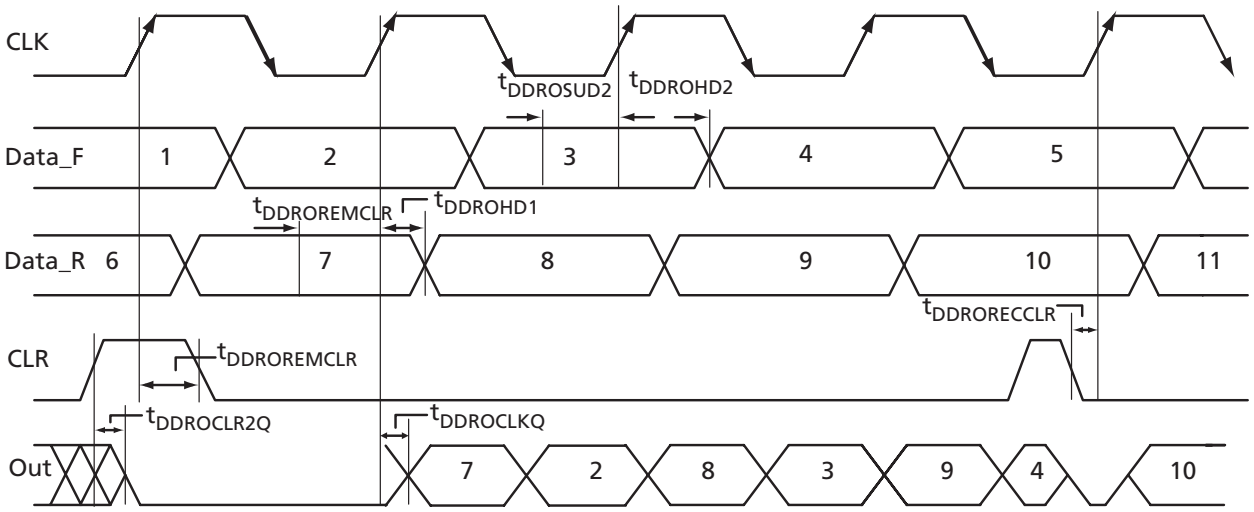


Figure 2-34 • **Output DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-192 • **Output DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.72	0.84	ns
$t_{DDRISUD1}$	Data_F Data Setup for Output DDR	0.39	0.45	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.39	0.45	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.82	0.96	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	0.27	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	0.22	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	0.36	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	0.32	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR			MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-193 • Output DDR Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.10	0.94	ns
$t_{DDRISUD1}$	Data_F Data Setup for Output DDR	0.59	0.50	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.59	0.50	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.26	1.07	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.35	0.30	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.36	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.32	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	TBD	TBD	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO,® Fusion, and ProASIC3 Macro Library Guide*.

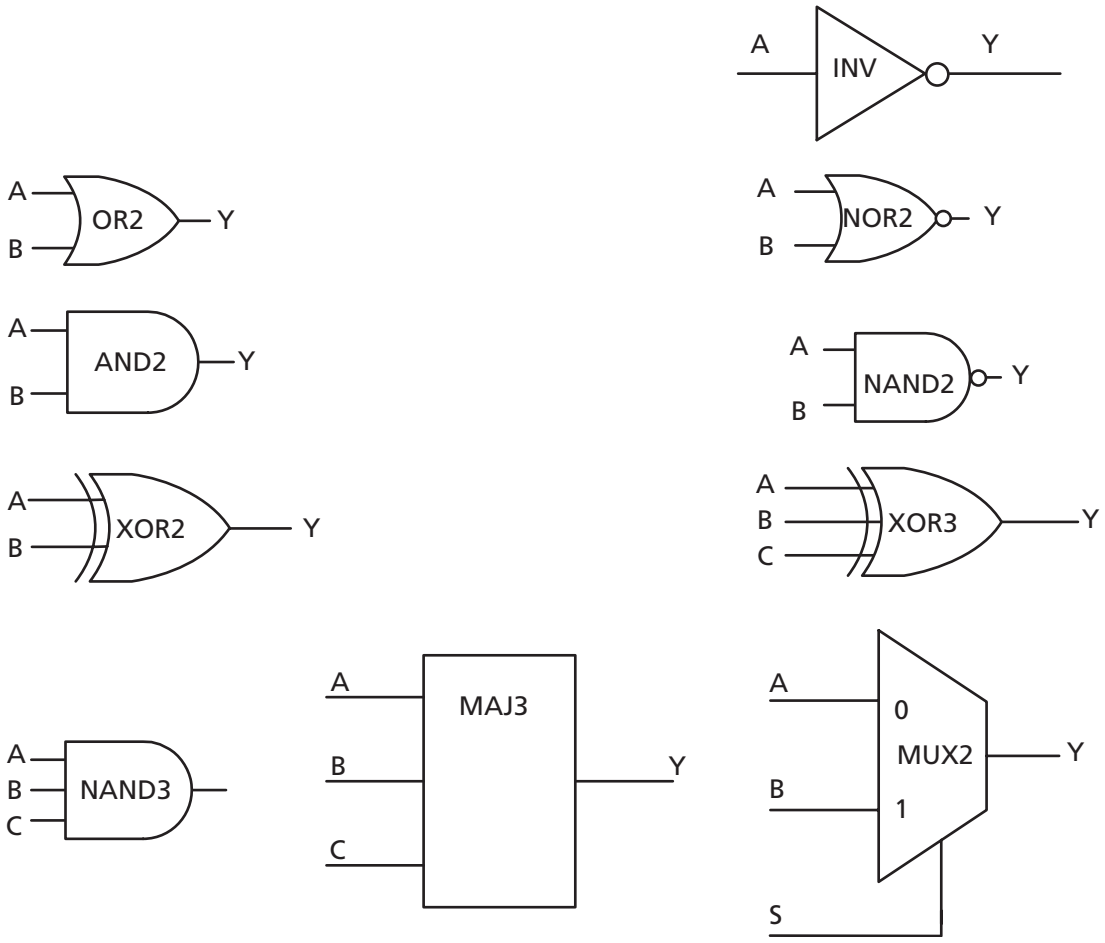


Figure 2-35 • **Sample of Combinatorial Cells**

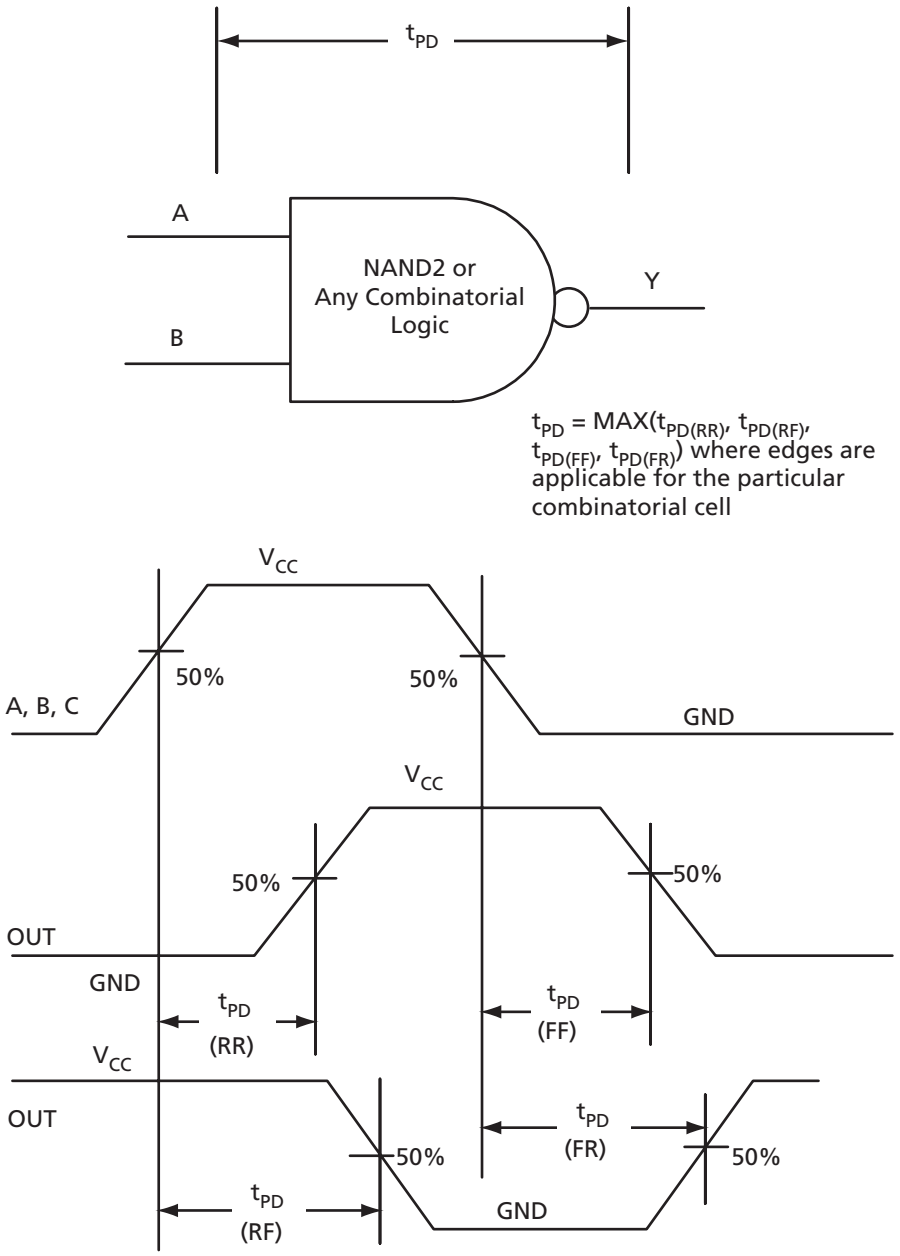


Figure 2-36 • **Timing Model and Waveforms**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-194 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.41	0.48	ns
AND2	Y = A · B	t_{PD}	0.48	0.57	ns
NAND2	Y = !(A · B)	t_{PD}	0.48	0.57	ns
OR2	Y = A + B	t_{PD}	0.50	0.58	ns
NOR2	Y = !(A + B)	t_{PD}	0.50	0.58	ns
XOR2	Y = A ⊕ B	t_{PD}	0.75	0.88	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	0.71	0.84	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.89	1.05	ns
MUX2	Y = A !S + B S	t_{PD}	0.52	0.61	ns
AND3	Y = A · B · C	t_{PD}	0.57	0.67	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-195 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.54	0.63	ns
AND2	Y = A · B	t_{PD}	0.63	0.74	ns
NAND2	Y = !(A · B)	t_{PD}	0.63	0.74	ns
OR2	Y = A + B	t_{PD}	0.65	0.76	ns
NOR2	Y = !(A + B)	t_{PD}	0.65	0.76	ns
XOR2	Y = A ⊕ B	t_{PD}	0.98	1.16	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	0.93	1.09	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.17	1.37	ns
MUX2	Y = A !S + B S	t_{PD}	0.68	0.79	ns
AND3	Y = A · B · C	t_{PD}	0.75	0.88	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

VersaTile Specifications as a Sequential Module

The ProASIC3 library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

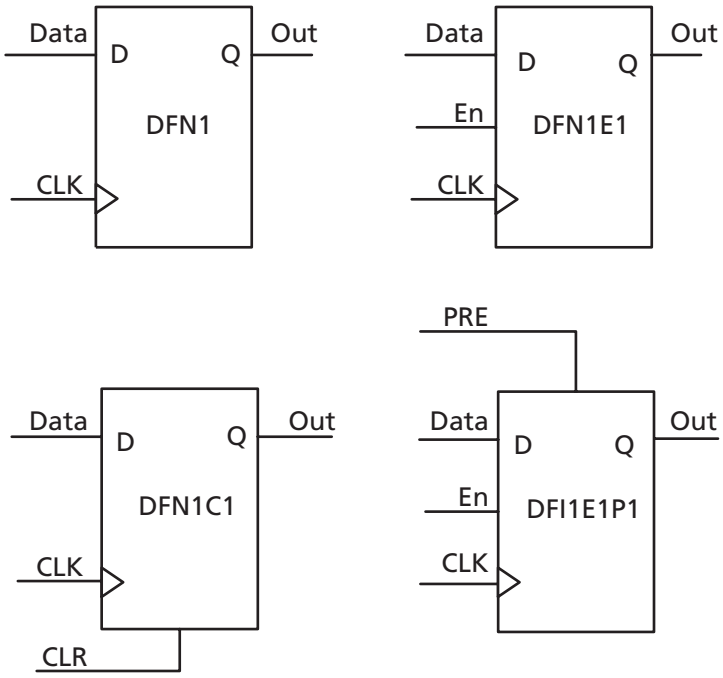


Figure 2-37 • **Sample of Sequential Cells**

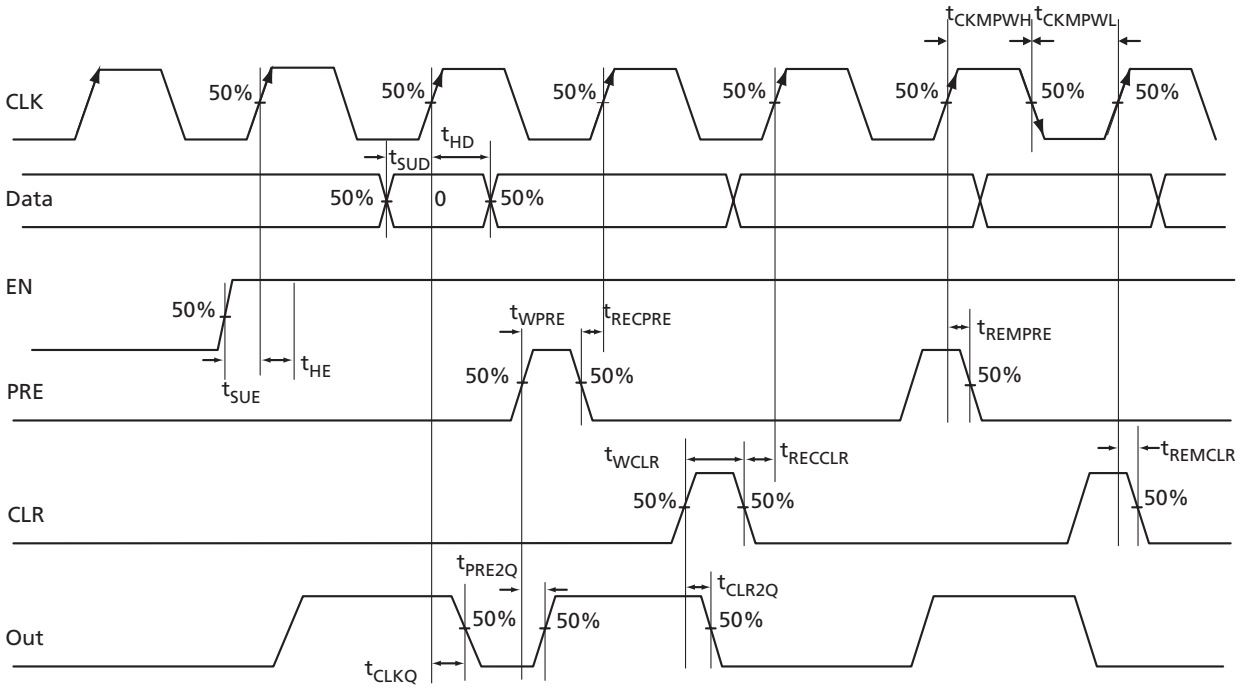


***Figure 2-38* • Timing Model and Waveforms**

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-196* • Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.56	0.66	ns
t_{SUD}	Data Setup Time for the Core Register	0.44	0.51	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.46	0.55	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.41	0.48	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.41	0.48	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.23	0.27	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	0.27	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	0.34	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	0.34	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.56	0.64	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.56	0.64	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-197 • Register Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.73	0.86	ns
t_{SUD}	Data Setup Time for the Core Register	0.57	0.67	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.61	0.71	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.53	0.63	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.53	0.63	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.30	0.35	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.30	0.35	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	0.34	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	0.34	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.56	0.64	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.56	0.64	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Global Resource Characteristics

A3P250L Clock Tree Topology

Clock delays are device-specific. Figure 2-39 is an example of a global tree used for clock routing. The global tree presented in Figure 2-39 is driven by a CCC located on the west side of the A3P250L device. It is used to drive all D-flip-flops in the device.

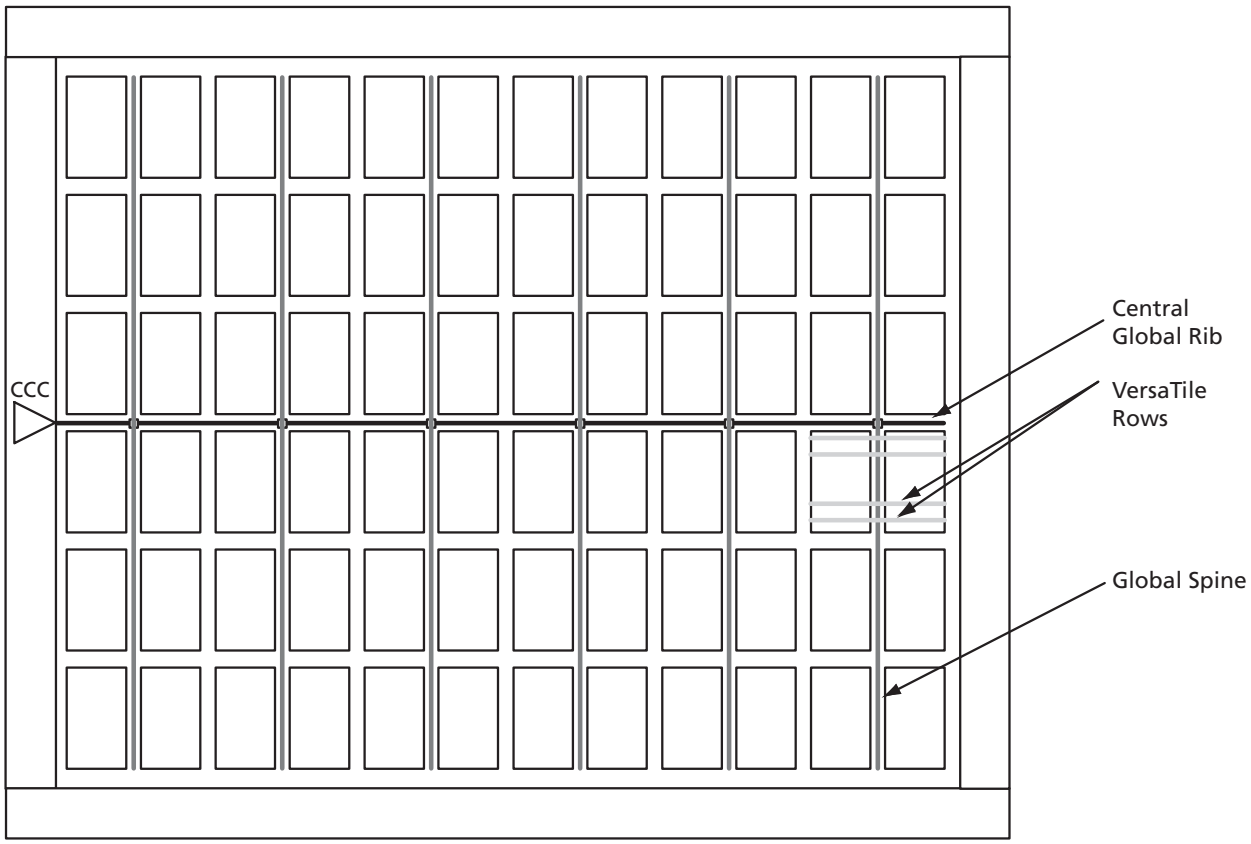


***Figure 2-39* • Example of Global Tree Use in an A3P250L Device for Clock Routing**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-123. Table 2-198 to Table 2-204 on page 2-122 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

***Table 2-198* • A3P250L Global Resource – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	0.82	1.06	0.96	1.25	ns
t_{RCKH}	Input HIGH Delay for Global Clock	0.80	1.09	0.94	1.28	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock					ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.29		0.34	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

***Table 2-199* • A3P250L Global Resource – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.40	1.68	1.64	1.97	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.38	1.71	1.62	2.01	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock					ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.33		0.39	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-200 • A3P600L Global Resource – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	0.90	1.14	1.06	1.34	ns
t_{RCKH}	Input HIGH Delay for Global Clock	0.89	1.17	1.04	1.38	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock					ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.28		0.33	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-201 • A3P600L Global Resource – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.48	1.76	1.74	2.07	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.47	1.80	1.72	2.11	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock					ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.33		0.39	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-202 • A3P1000L Global Resource – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.02	1.26	1.20	1.48	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.01	1.29	1.18	1.52	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock					ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.28		0.33	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-203 • A3P1000L Global Resource – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.61	1.89	1.89	2.22	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.60	1.92	1.88	2.26	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock					ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.33		0.39	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-204 • A3PE3000L Global Resource – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.53	1.75	1.79	2.06	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.51	1.77	1.78	2.08	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock					ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.30	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-205 • A3PE3000L Global Resource – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.52	1.94	1.78	2.28	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.49	1.96	1.76	2.30	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock					ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.47		0.55	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

***Table 2-206* • ProASIC3LP CCC/PLL Specification**
CCC/PLL Operating at 1.2 V

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		270		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL [4]			100	MHz
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Max Peak-to-Peak Period Jitter			
	1 Global Network Used	External FB Used	3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%	0.75%	0.70%	
24 MHz to 100 MHz	1.00%	1.50%	1.20%	
100 MHz to 250 MHz	2.50%	3.75%	2.75%	
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter				
LockControl = 0			2	ns
LockControl = 1			1	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	1.2		15.65	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.025		15.65	ns
Delay Range in Block: Fixed Delay [1, 2]		3.1		ns

Notes:

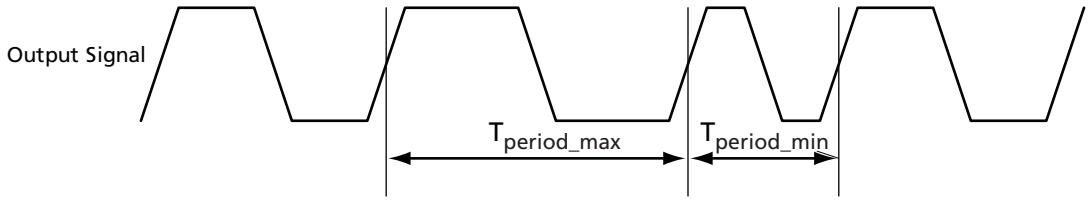
1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-7 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.2 V*
3. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
4. *Maximum value obtained for a –1 speed grade device in worst-case commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-207 • ProASIC3LP CCC/PLL Specification
CCC/PLL Operating at 1.5 V

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350	MHz
Serial Clock (SCLK) for Dynamic PLL [4]			110	
Delay Increments in Programmable Delay Blocks [1, 2]		160		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Max Peak-to-Peak Period Jitter			
	1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%		0.70%	
24 MHz to 100 MHz	1.00%		1.20%	
100 MHz to 250 MHz	1.75%		2.00	
250 MHz to 350 MHz	2.50%		5.60%	
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter				
LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.025		5.56	ns
Delay Range in Block: Fixed Delay [1, 2]		2.2		ns

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-7 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.5 V*
3. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
4. *Maximum value obtained for a –1 speed grade device in worst-case commercial conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

Figure 2-40 • Peak-to-Peak Jitter Definition

Embedded SRAM and FIFO Characteristics

SRAM

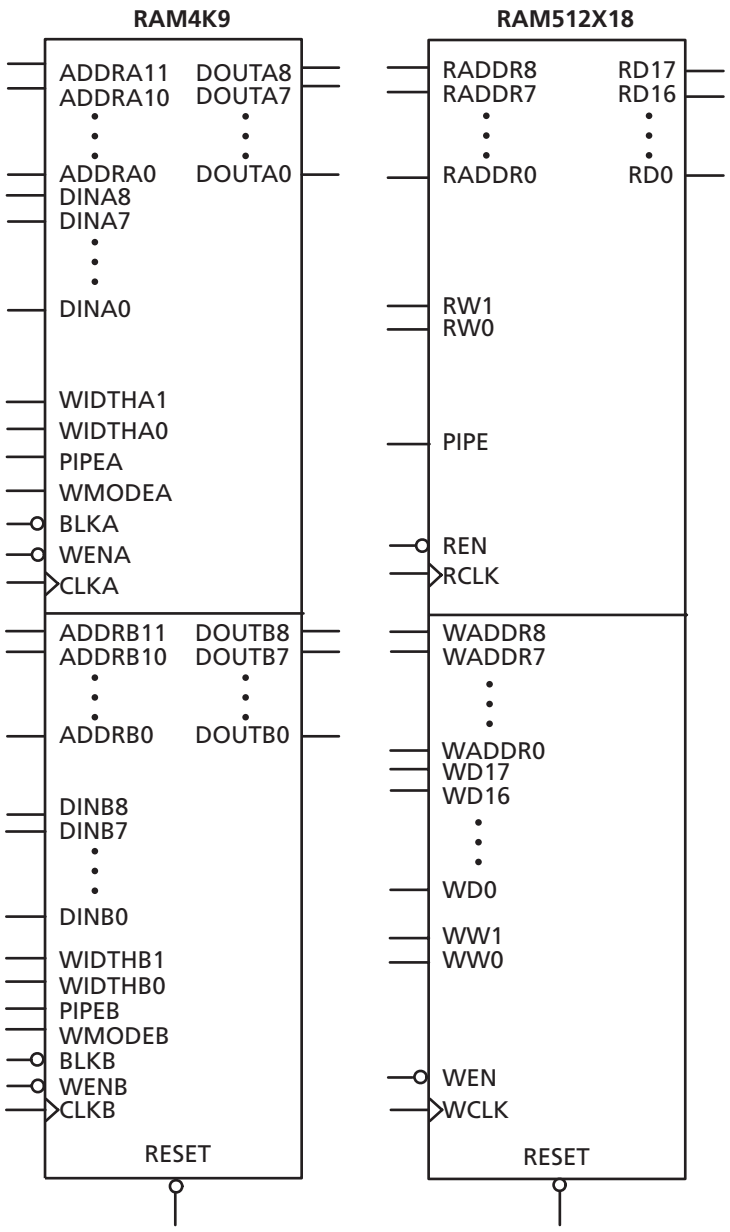


Figure 2-41 • **RAM Models**

Timing Waveforms

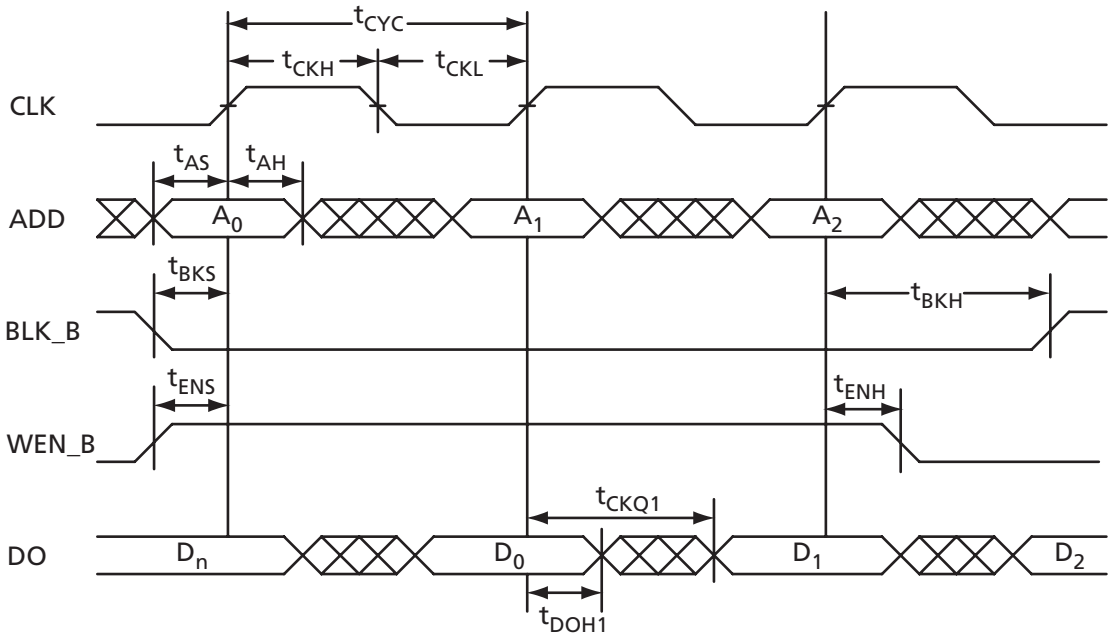


Figure 2-42 • **RAM Read for Pass-Through Output**

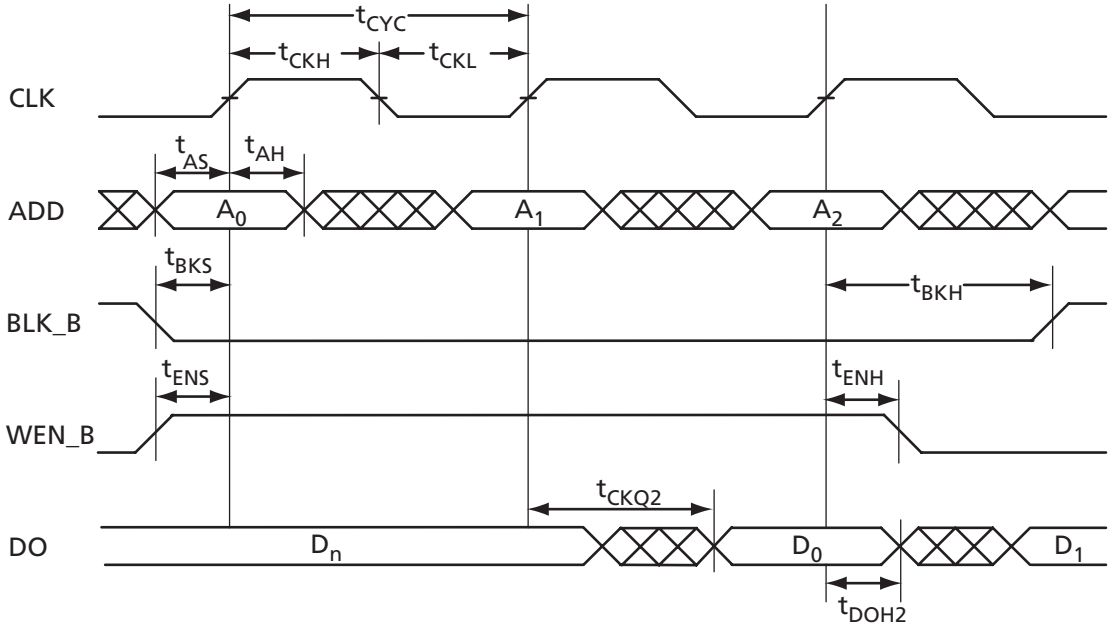


Figure 2-43 • **RAM Read for Pipelined Output**

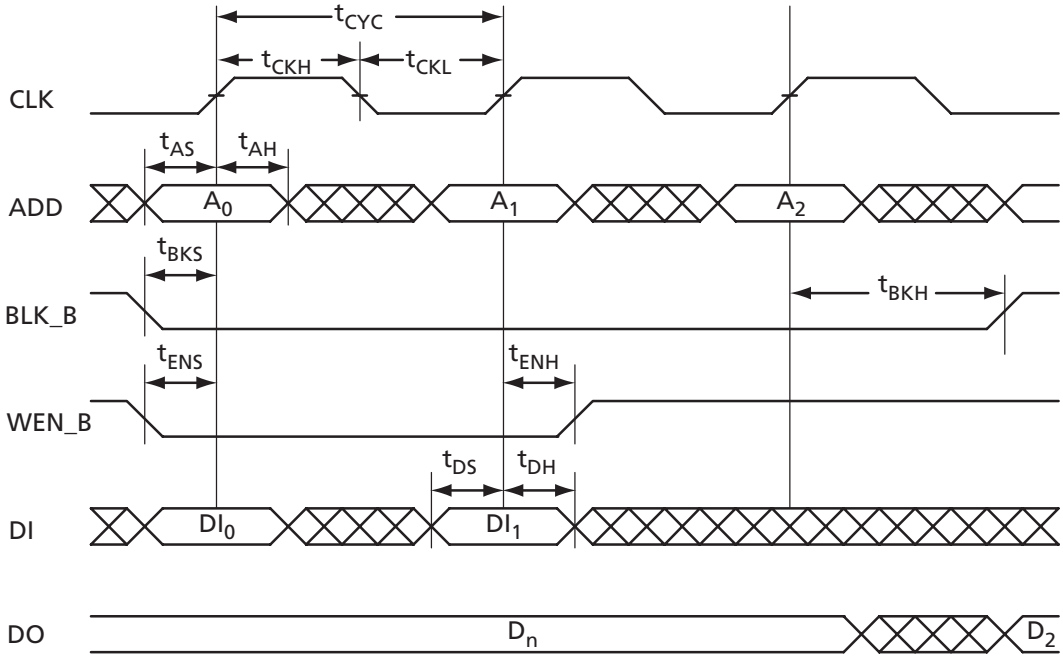


Figure 2-44 • **RAM Write, Output Retained (WMODE = 0)**

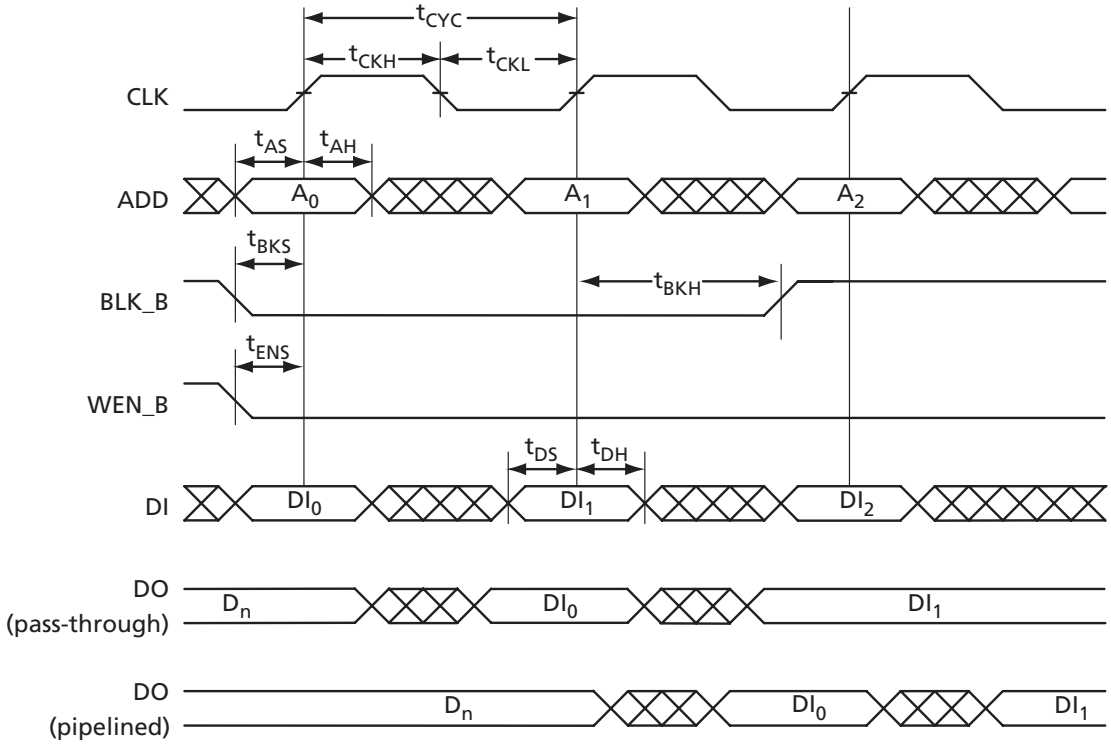


Figure 2-45 • **RAM Write, Output as Write Data (WMODE = 1)**

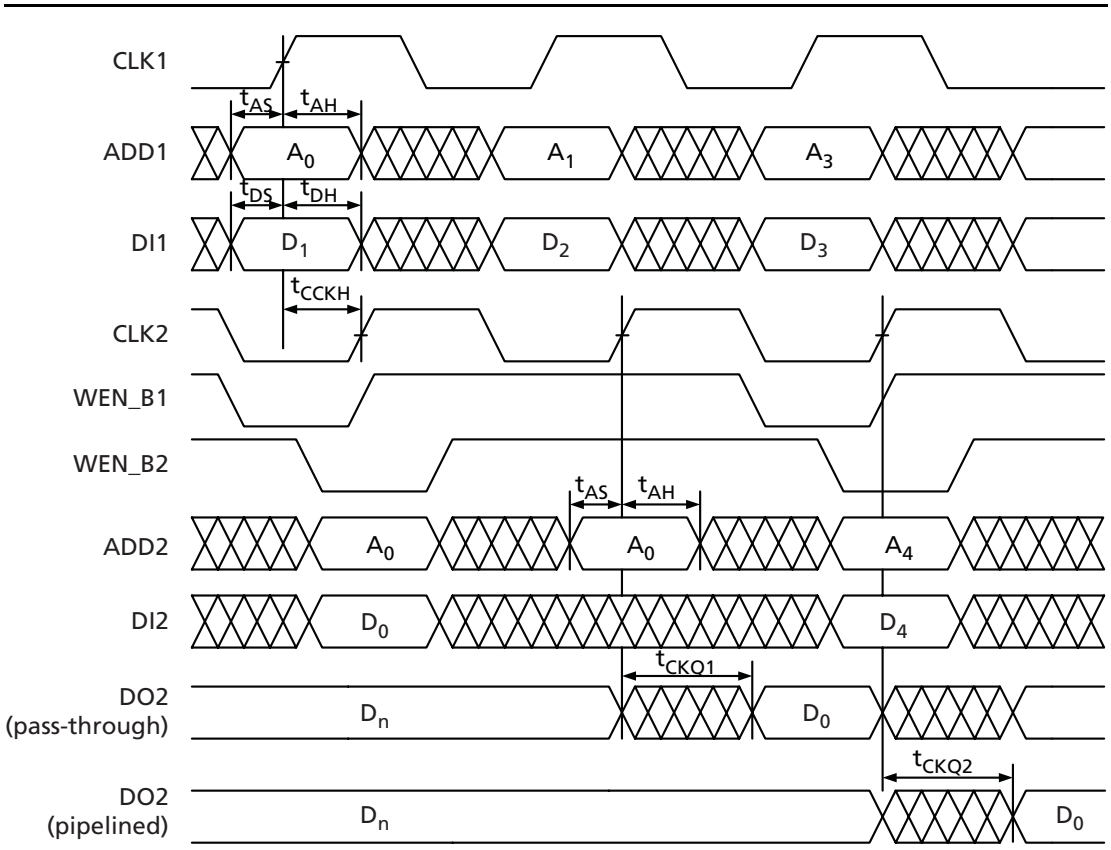


Figure 2-46 • **Write Access after Write onto Same Address**

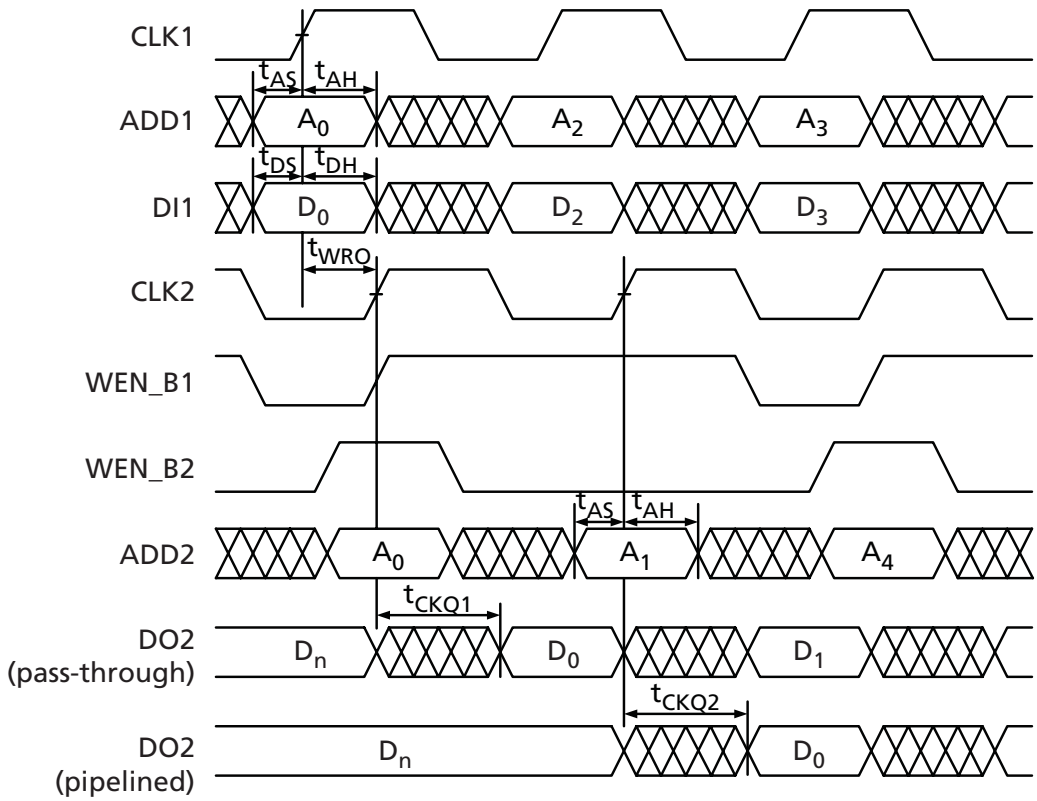


Figure 2-47 • **Read Access after Write onto Same Address**

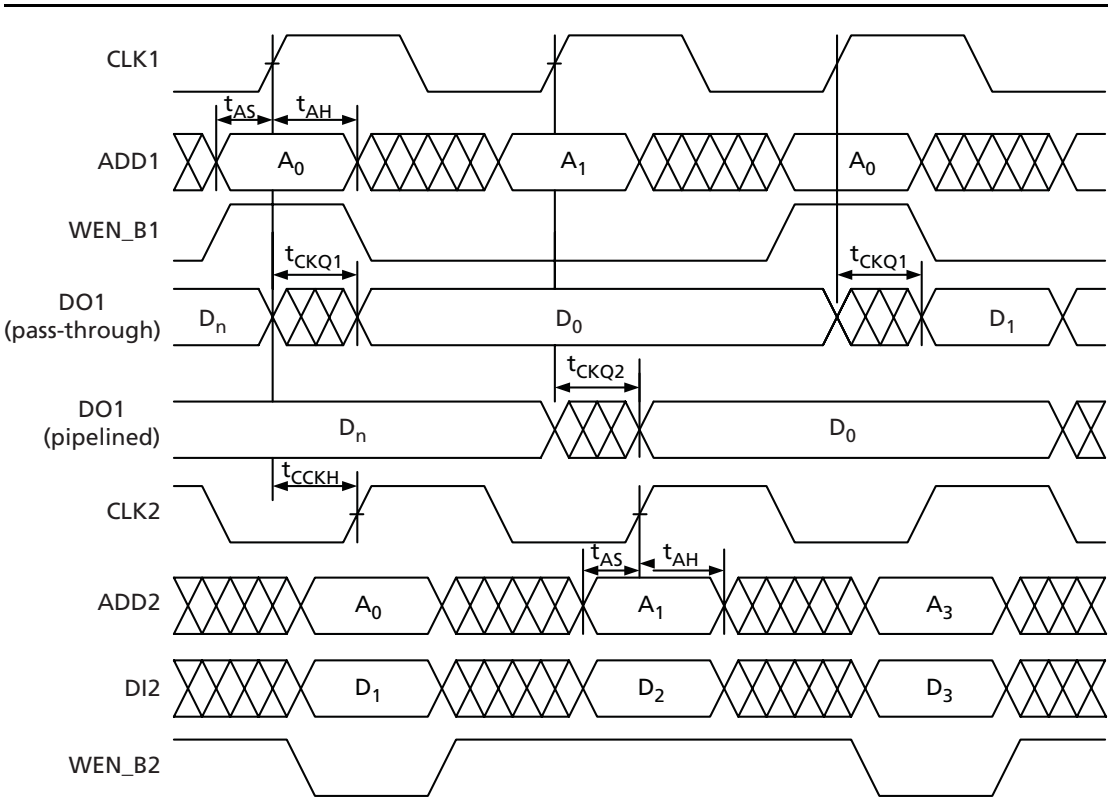


***Figure 2-48* • Write Access after Read onto Same Address**

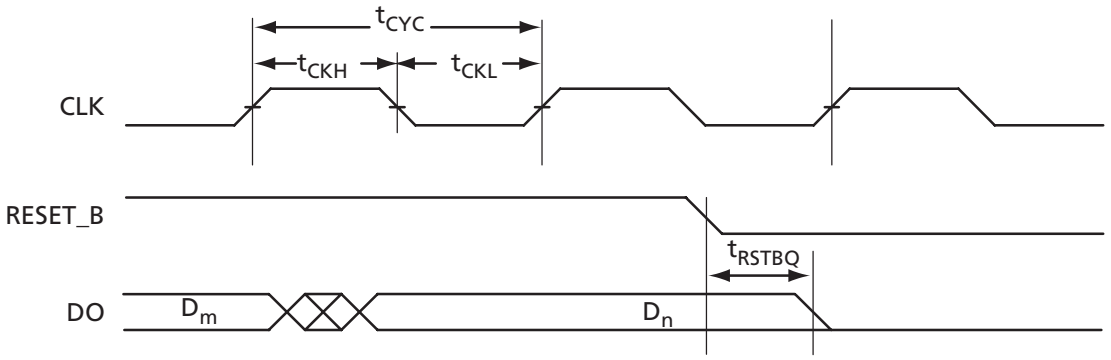


***Figure 2-49* • RAM Reset**

Timing Characteristics

Table 2-208 • RAM4K9 – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.30	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN_B, WEN_B setup time	0.15	0.17	ns
t_{ENH}	REN_B, WEN_B hold time	0.10	0.12	ns
t_{BKS}	BLK_B setup time	0.24	0.28	ns
t_{BKH}	BLK_B hold time	0.02	0.02	ns
t_{DS}	Input data (DI) setup time	0.19	0.22	ns
t_{DH}	Input data (DI) hold time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to new data valid on DO (output retained, WMODE = 0)	1.82	2.14	ns
	Clock HIGH to new data valid on DO (flow-through, WMODE = 1)	2.40	2.83	ns
t_{CKQ2}	Clock HIGH to new data valid on DO (pipelined)	0.91	1.07	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	ns
t_{RSTBQ}	RESET_B LOW to data out LOW on DO (flow-through)	0.94	1.11	ns
	RESET_B LOW to data out LOW on DO (pipelined)	0.94	1.11	ns
$t_{REMRSTB}$	RESET_B removal	0.29	0.34	ns
$t_{RECRSTB}$	RESET_B recovery	1.53	1.80	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.55	0.64	ns
t_{CYC}	Clock cycle time	5.10	5.87	ns
F_{MAX}	Maximum frequency	196	170	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-209 • RAM4K9 – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.33	0.39	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN_B, WEN_B setup time	0.19	0.22	ns
t_{ENH}	REN_B, WEN_B hold time	0.13	0.15	ns
t_{BKS}	BLK_B setup time	0.31	0.36	ns
t_{BKH}	BLK_B hold time	0.02	0.03	ns
t_{DS}	Input data (DI) setup time	0.24	0.29	ns
t_{DH}	Input data (DI) hold time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to new data valid on DO (output retained, WMODE = 0)	2.38	2.80	ns
	Clock HIGH to new data valid on DO (flow-through, WMODE = 1)	3.14	3.69	ns
t_{CKQ2}	Clock HIGH to new data valid on DO (pipelined)	1.19	1.40	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	ns
t_{RSTBQ}	RESET_B LOW to data out LOW on DO (flow-through)	1.23	1.45	ns
	RESET_B LOW to data out LOW on DO (pipelined)	1.23	1.45	ns
$t_{REMRSTB}$	RESET_B removal	0.38	0.45	ns
$t_{RECRSTB}$	RESET_B recovery	2.00	2.35	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.63	0.72	ns
t_{CYC}	Clock cycle time	5.75	6.61	ns
F_{MAX}	Maximum frequency	174	151	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-210 • RAM512X18 – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.30	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN_B, WEN_B setup time	0.09	0.11	ns
t_{ENH}	REN_B, WEN_B hold time	0.06	0.07	ns
t_{DS}	Input data (DI) setup time	0.19	0.22	ns
t_{DH}	Input data (DI) hold time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to new data valid on DO (output retained, WMODE = 0)	2.20	2.59	ns
t_{CKQ2}	Clock HIGH to new data valid on DO (pipelined)	0.91	1.07	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	ns
t_{RSTBQ}	RESET_B LOW to data out LOW on DO (flow through)	0.94	1.11	ns
	RESET_B LOW to data out LOW on DO (pipelined)	0.94	1.11	ns
$t_{REMRSTB}$	RESET_B removal	0.29	0.34	ns
$t_{RECRSTB}$	RESET_B recovery	1.53	1.80	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.55	0.64	ns
t_{CYC}	Clock cycle time	5.10	5.87	ns
F_{MAX}	Maximum frequency	196	170	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-211 • RAM512X18 – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.33	0.39	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN_B, WEN_B setup time	0.12	0.14	ns
t_{ENH}	REN_B, WEN_B hold time	0.08	0.09	ns
t_{DS}	Input data (DI) setup time	0.24	0.29	ns
t_{DH}	Input data (DI) hold time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to new data valid on DO (output retained, WMODE = 0)	2.88	3.39	ns
t_{CKQ2}	Clock HIGH to new data valid on DO (pipelined)	1.19	1.40	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	ns
t_{RSTBQ}	RESET_B LOW to data out LOW on DO (flow-through)	1.23	1.45	ns
	RESET_B LOW to data out LOW on DO (pipelined)	1.23	1.45	ns
$t_{REMRSTB}$	RESET_B removal	0.38	0.45	ns
$t_{RECRSTB}$	RESET_B recovery	2.00	2.35	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.63	0.72	ns
t_{CYC}	Clock cycle time	5.75	6.61	ns
F_{MAX}	Maximum frequency	174	151	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

FIFO

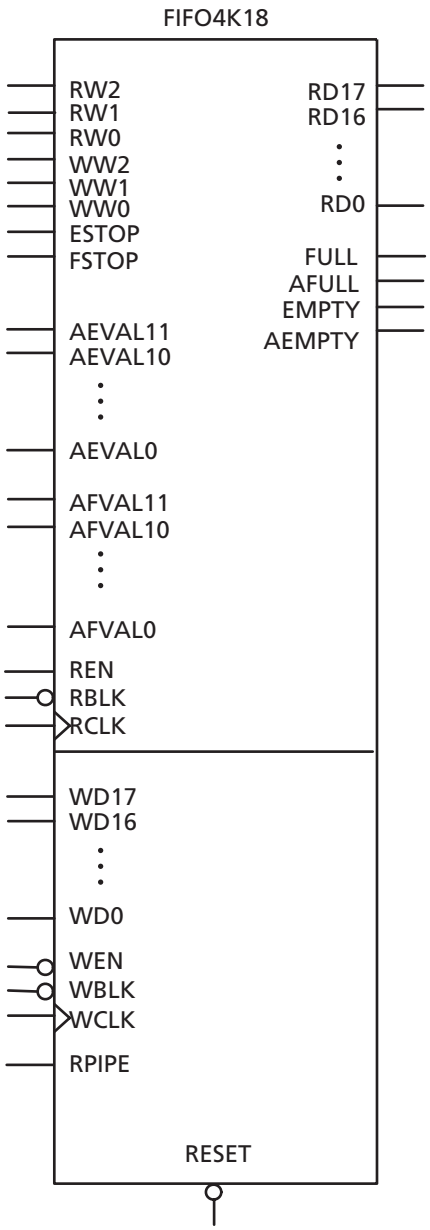


Figure 2-50 • **FIFO Model**

Timing Waveforms

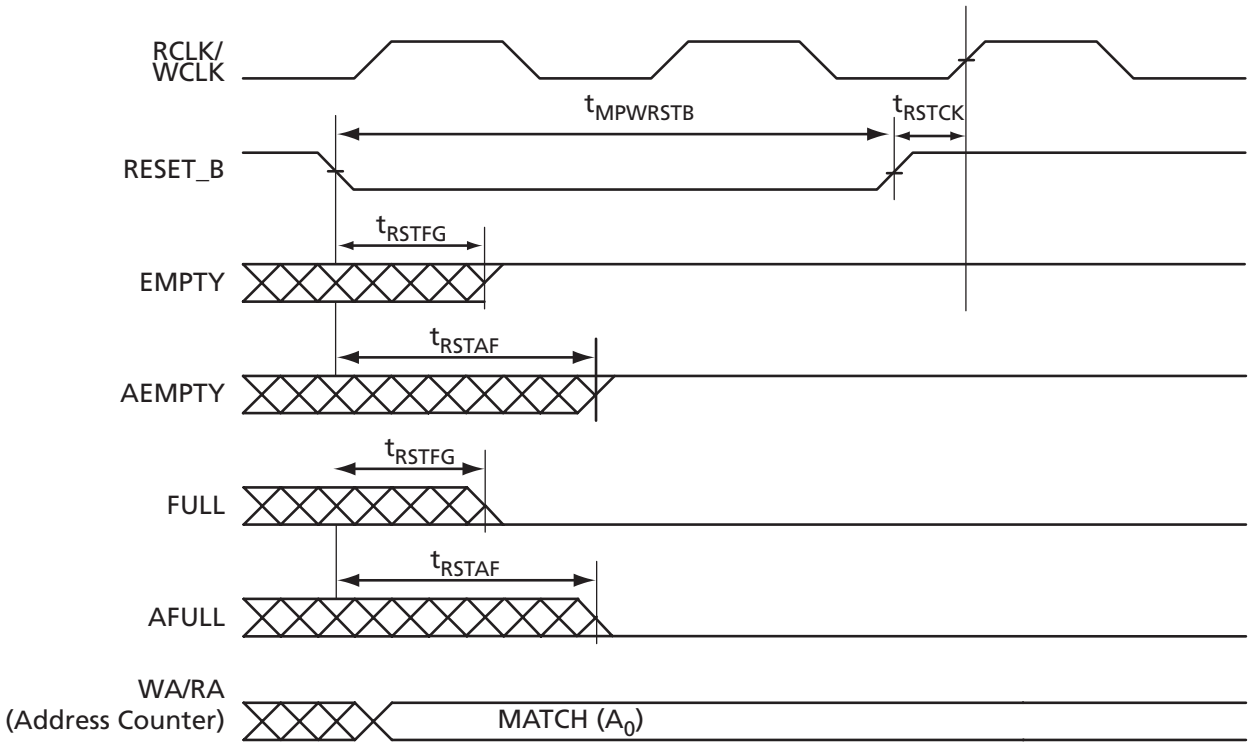


Figure 2-51 • **FIFO Reset**

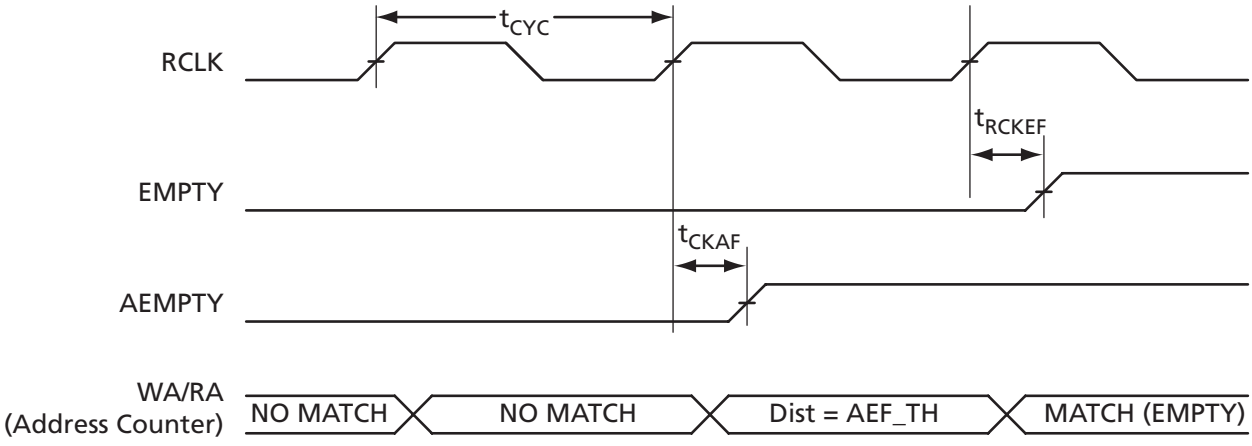


Figure 2-52 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

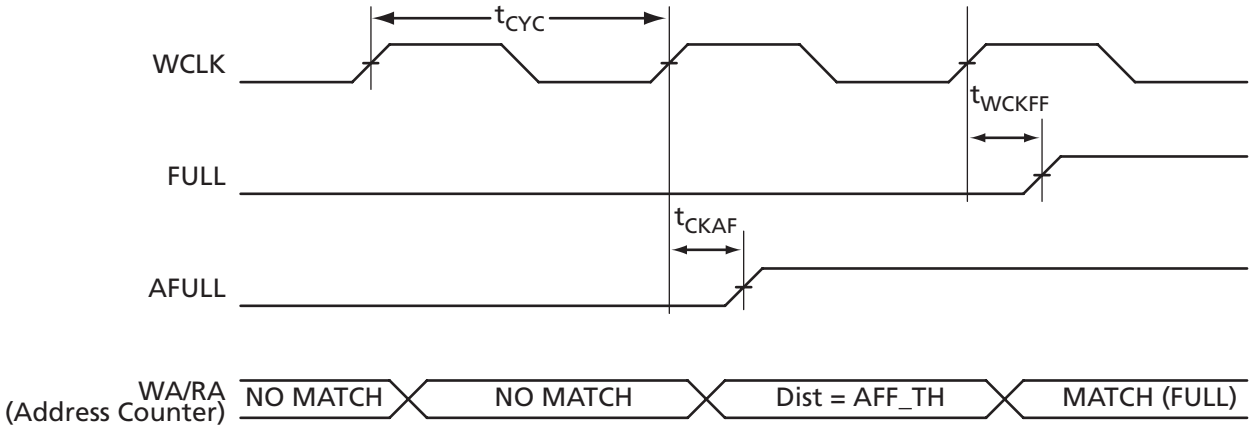


Figure 2-53 • **FIFO FULL Flag and AFULL Flag Assertion**

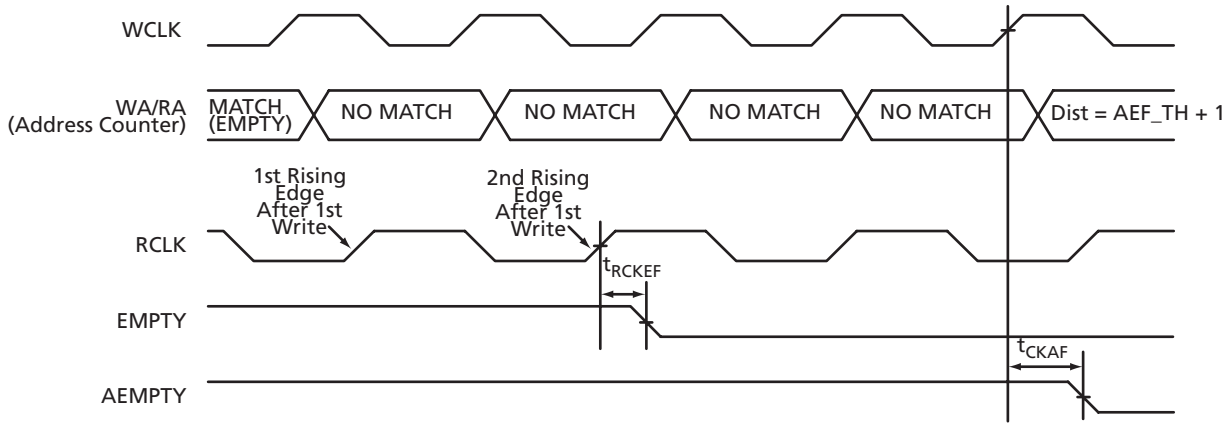


Figure 2-54 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

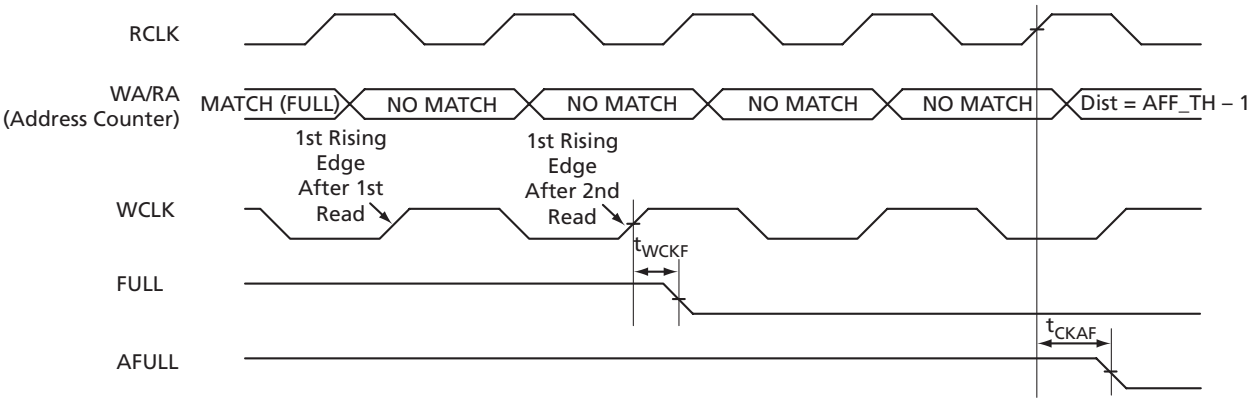


Figure 2-55 • **FIFO FULL Flag and AFULL Flag Deassertion**

Timing Characteristics

Table 2-212 • FIFO – Applies to 1.5 V DC Core Voltage
Worst Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ENS}	REN_B, WEN_B Setup Time	1.40	1.65	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.02	0.02	ns
t_{BKS}	BLK_B Setup Time	0.40	0.47	ns
t_{BKH}	BLK_B Hold Time	0.00	0.00	ns
t_{DS}	Input Data (DI) Setup Time	0.19	0.22	ns
t_{DH}	Input Data (DI) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (flow-through)	2.40	2.83	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	0.91	1.07	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	1.75	2.06	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	1.66	1.96	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	6.31	7.42	ns
t_{RSTFG}	RESET_B LOW to Empty/Full Flag Valid	1.73	2.03	ns
t_{RSTAF}	RESET_B LOW to Almost Empty/Full Flag Valid	6.25	7.35	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (flow-through)	0.94	1.11	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	0.94	1.11	ns
$t_{REMRSTB}$	RESET_B Removal	0.29	0.34	ns
$t_{RECRSTB}$	RESET_B Recovery	1.53	1.80	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.55	0.64	ns
t_{CYC}	Clock Cycle Time	5.10	5.87	ns
F_{MAX}	Maximum Frequency for FIFO	196	170	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-213 • FIFO – Applies to 1.2 V DC Core Voltage
Worst Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	–1	Std.	Units
t_{ENS}	REN_B, WEN_B Setup Time	1.84	2.16	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.02	0.03	ns
t_{BKS}	BLK_B Setup Time	0.40	0.47	ns
t_{BKH}	BLK_B Hold Time	0.00	0.00	ns
t_{DS}	Input Data (DI) Setup Time	0.24	0.29	ns
t_{DH}	Input Data (DI) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (flow-through)	3.14	3.69	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	1.19	1.40	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	2.29	2.69	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	2.18	2.56	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	8.25	9.70	ns
t_{RSTFG}	RESET_B LOW to Empty/Full Flag Valid	2.26	2.65	ns
t_{RSTAF}	RESET_B LOW to Almost Empty/Full Flag Valid	8.17	9.60	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (flow-through)	1.23	1.45	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	1.23	1.45	ns
$t_{REMRSTB}$	RESET_B Removal	0.38	0.45	ns
$t_{RECRSTB}$	RESET_B Recovery	2.00	2.35	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.63	0.72	ns
t_{CYC}	Clock Cycle Time	5.75	6.61	ns
F_{MAX}	Maximum Frequency for FIFO	174	151	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Embedded FlashROM Characteristics

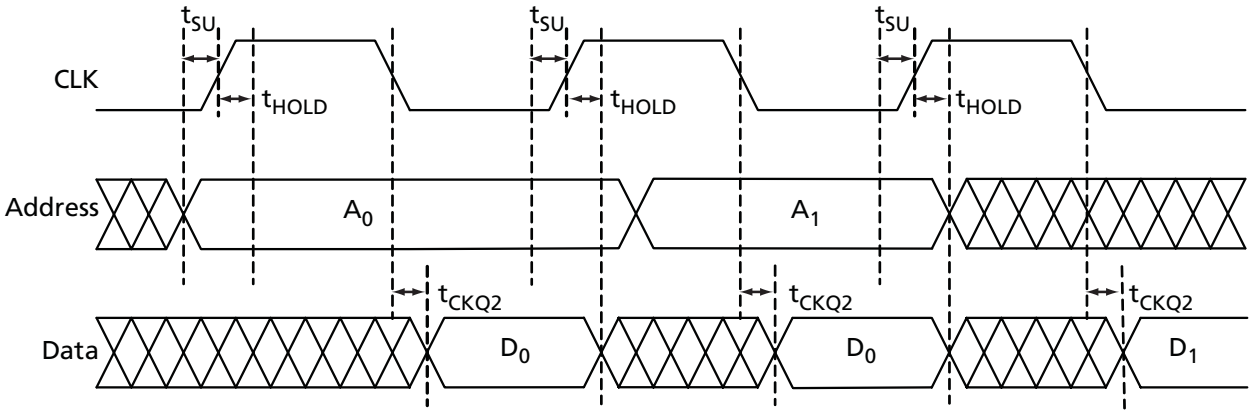


Figure 2-56 • **Timing Diagram**

Timing Characteristics

Table 2-214 • **Embedded FlashROM Access Time – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–1	Std.	Units
t_{SU}	Address Setup Time	0.54	0.64	ns
t_{HOLD}	Address Hold Time	0.00	0.00	ns
t_{CK2Q}	Clock to Out	16.55	19.46	ns
F_{MAX}	Maximum Clock Frequency	15	15	MHz

Table 2-215 • **Embedded FlashROM Access Time– Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	–1	Std.	Units
t_{SU}	Address Setup Time	0.71	0.83	ns
t_{HOLD}	Address Hold Time	0.00	0.00	ns
t_{CK2Q}	Clock to Out	21.64	25.44	ns
F_{MAX}	Maximum Clock Frequency	15	15	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-18 for more details.

Timing Characteristics

Table 2-216 • JTAG 1532 – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.57	0.67	ns
t_{DIHD}	Test Data Input Hold Time	1.13	1.33	ns
t_{TMSSU}	Test Mode Select Setup Time	0.57	0.67	ns
t_{TMDHD}	Test Mode Select Hold Time	1.13	1.33	ns
t_{TCK2Q}	Clock to Q (data out)	5.67	6.67	ns
t_{RSTB2Q}	Reset to Q (data out)	22.67	26.67	ns
F_{TCKMAX}	TCK Maximum Frequency	24.00	21.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.00	0.00	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.23	0.27	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-217 • JTAG 1532 – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.75	0.88	ns
t_{DIHD}	Test Data Input Hold Time	1.50	1.76	ns
t_{TMSSU}	Test Mode Select Setup Time	0.75	0.88	ns
t_{TMDHD}	Test Mode Select Hold Time	1.50	1.76	ns
t_{TCK2Q}	Clock to Q (data out)	6.00	7.06	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	29.41	ns
F_{TCKMAX}	TCK Maximum Frequency	20.00	17.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.45	0.53	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Part Number and Revision Date

Part Number 51700100-002-5
Revised August 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (Advance v0.6)	Page
Advance v0.5 (August 2008)	3.0 V LVCMOS wide range support data was added to Table 2-2 · Recommended Operating Conditions [1].	2-2
	3.3 V LVCMOS wide range support data was added to Table 2-22 · Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings to Table 2-24 · Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings.	2-22 to 2-23
	3.3 V LVCMOS wide range support data was added to Table 2-26 · Summary of AC Memory Points.	2-25
	3.3 V LVCMOS wide range support text was added to "3.3 V LVTTL / 3.3 V LVCMOS".	2-39
	Table 2-48 · Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range is new.	2-40
Advance v0.4 (July 2008)	Table 2-6 · Temperature and Voltage Derating Factors for Timing Delays was updated to add several new rows of values.	2-7
	Table 2-7 · Quiescent Supply Current (I_{DD}) Characteristics, ProASIC3L Flash*Freeze Mode* through Table 2-10 · Quiescent Supply Current (I_{DD}), No ProASIC3L Flash*Freeze Mode1 were updated to add 1.5 V core voltage.	2-7 to 2-8
	Table 2-18 · Different Components Contributing to Dynamic Power Consumption in ProASIC3L Devices at 1.5 V V_{CC} is new.	2-14
	Table 2-19 · Different Components Contributing to the Static Power Consumption in ProASIC3L Devices was updated to add the static PLL contribution at 1.5 V core operation.	2-14
	Timing tables were updated to include tables for 1.5 V core voltage.	N/A
	Table 2-206 · ProASIC3LP CCC/PLL Specification was updated for core voltage 1.2 V and Table 2-207 · ProASIC3LP CCC/PLL Specification for 1.5 V is new.	2-123, 2-124
Advance v0.3 (June 2008)	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
Advance v0.2 (February 2008)	Tables have been updated to include the LVCMOS 1.2 V I/O set. DDR Tables have two additional data points added to reflect both edges for Input DDR setup and hold time. Power data table has been updated to match SmartPower data rather then simulation values.	N/A
	Table 2-1 · Absolute Maximum Ratings was updated to add VMV to the V_{CCI} parameter row and to remove the word "output" from the parameter description for V_{CCI}. Table note 3 was added.	2-1

Previous Version	Changes in Current Version (Advance v0.6)	Page
Advance v0.2 (continued)	Table 2-2 · Recommended Operating Conditions [1] was updated to add table note references and rearrange the order of notes. VMV was added to the V_{CCI} parameter row. A new row was added for V_{CC}, 1.5 V DC core supply voltage. The table note stating that 1.5 V data will be released at a later date is new. The table note on VMV pins is new.	2-2
	Table 2-4 · Overshoot and Undershoot Limits [1]. The title was revised to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was revised to remove "refers only to overshoot/undershoot limits for simultaneous switching I/Os."	2-3
	EQ 2-2 was updated. The temperature was changed to 100°C, and therefore the end result changed.	2-6
	The table notes for Table 2-7 · Quiescent Supply Current (I_{DD}) Characteristics, ProASIC3L Flash*Freeze Mode* and Table 2-8 · Quiescent Supply Current (I_{DD}) Characteristics, ProASIC3L Sleep Mode (V_{CC} = 0 V)* were updated to remove VMV and include P_{DC6} and P_{DC7}. The table note for Table 2-7 · Quiescent Supply Current (I_{DD}) Characteristics, ProASIC3L Flash*Freeze Mode* was updated to include V_{JTAG}.	2-7
	Table 2-9 · Quiescent Supply Current (I_{DD}) Characteristics, Shutdown Mode (V_{CC}, V_{CCI} = 0 V) is new.	2-7
	Note 2 of Table 2-10 · Quiescent Supply Current (I_{DD}), No ProASIC3L Flash*Freeze Mode1 was updated to include V_{CCPLL}. Note 4 was updated to include P_{DC6} and P_{DC7}.	2-8
	Table 2-11 · Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings through Table 2-16 · Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1]were updated to change P_{DC2} to P_{DC6} and P_{DC3} to P_{DC7}. The table notes were updated to reflect that power was measured on V_{CCI}. The subtitle of the table was changed from "Applicable to Advanced I/O Banks" to "Applicable to Pro I/O Banks."	2-9 through 2-12
	The word "input" in the titles of Table 2-14 · Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1] and Table 2-15 · Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1], was changed to "output."	2-11, 2-12
	The value of C_{LOAD} for single-ended 3.3 V PCI was changed to 10 from 5 in Table 2-14 · Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1] through Table 2-16 · Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings [1].	2-11 through 2-12
	The last section of Table 2-17 · Different Components Contributing to Dynamic Power Consumption in ProASIC3L Devices at 1.2 V V_{CC} was made into a new table: Table 2-19 · Different Components Contributing to the Static Power Consumption in ProASIC3L Devices. The table numbers referenced for device-specific dynamic power for P_{AC9} and P_{AC10} were changed in Table 2-17 · Different Components Contributing to Dynamic Power Consumption in ProASIC3L Devices at 1.2 V V_{CC}. The definition of P_{DC5} was updated and parameters P_{DC6} and P_{DC7} were added to Table 2-19 · Different Components Contributing to the Static Power Consumption in ProASIC3L Devices.	2-13
	The "Total Static Power Consumption—P_{STAT}" section was updated to revise the calculation of P_{STAT}, including P_{DC6} and P_{DC7}.	2-15
	Footnote 1 was updated to include information about P_{AC13}.	2-16

Previous Version	Changes in Current Version (Advance v0.6)	Page
Advance v0.2 (continued)	Table 2-42 · Schmitt Trigger Input Hysteresis, Hysteresis Voltage Value (Typ) for Schmitt Mode Input Buffers was updated to include the hysteresis value for 1.2 V LVCMOS.	2-37
	The "1.2 V LVCMOS (JESD8-12A)" section is new.	2-71
Advance v0.1 (January 2008)	The "PLL Behavior at Brownout Condition" section is new.	2-4
	Table 2-198 · A3P250L Global Resource – Applies to 1.5 V DC Core Voltage, Table 2-200 · A3P600L Global Resource – Applies to 1.5 V DC Core Voltage, Table 2-202 · A3P1000L Global Resource – Applies to 1.5 V DC Core Voltage, and Table 2-204 · A3PE3000L Global Resource – Applies to 1.5 V DC Core Voltage were updated with values for t_{RCKL}, t_{RCKH}, and t_{RCKSW}.	2-119 – 2-121
	The worst-case commercial conditions were added to Table 2-215 · Embedded FlashROM Access Time– Applies to 1.2 V DC Core Voltage.	2-140
	Table 2-17 · Different Components Contributing to Dynamic Power Consumption in ProASIC3L Devices at 1.2 V V_{CC} was updated to revise the value for P_{AC14} and add parameters P_{DC1} through P_{DC5} to the table.	2-13

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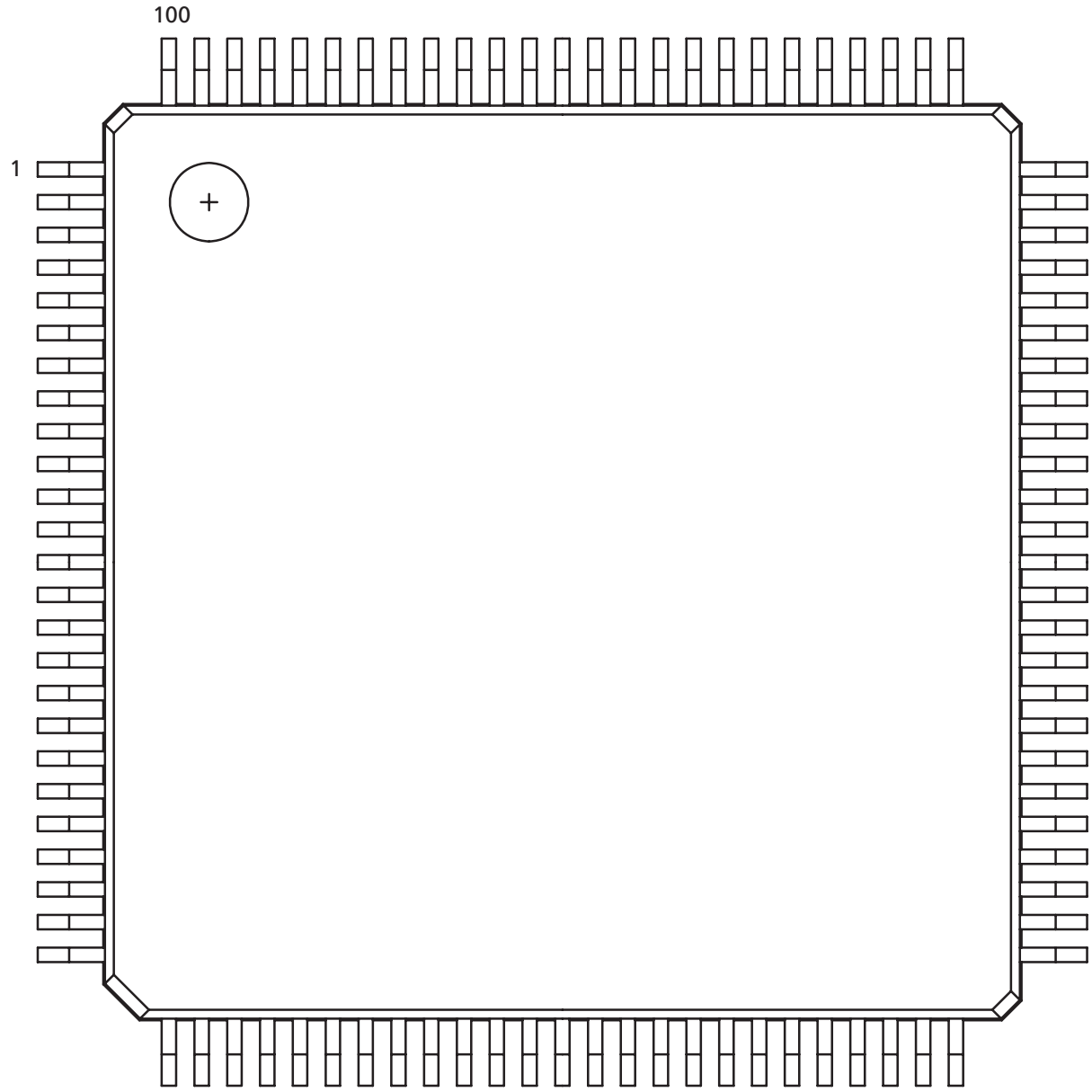
3 – Package Pin Assignments

100-Pin VQFP



Note: This is the top view of the package.

Figure 3-1 •

Note

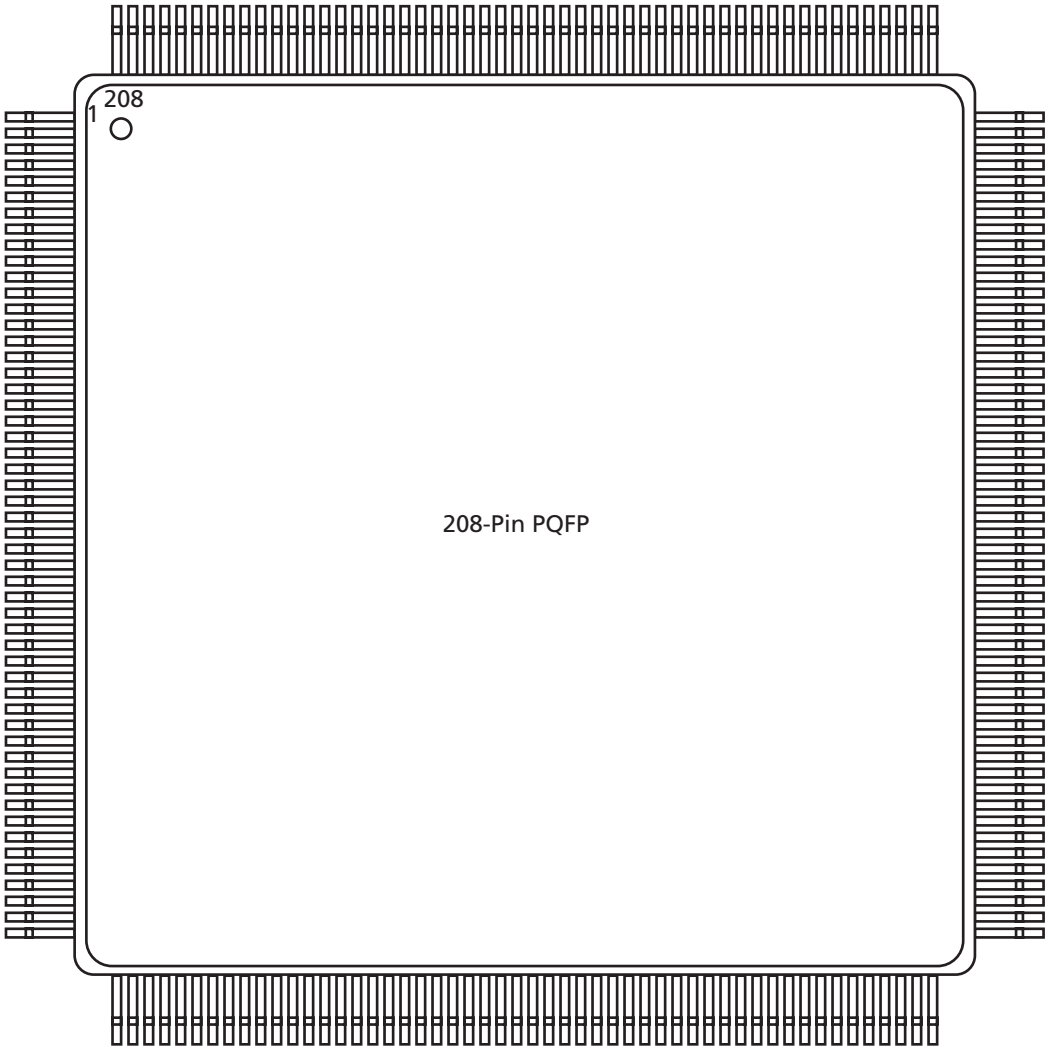
For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

100-Pin VQFP	
Pin Number	A3P250L Function
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO112PSB3
9	GND
10	GFB1/IO109PDB3
11	GFB0/IO109NDB3
12	V_{COMPLF}
13	GFA0/IO108NPB3
14	V_{CCPLF}
15	GFA1/IO108PPB3
16	GFA2/IO107PSB3
17	V_{CC}
18	V_{CCI}B3
19	GFC2/IO105PSB3
20	GEC1/IO100PDB3
21	GEC0/IO100NDB3
22	GEA1/IO98PDB3
23	GEA0/IO98NDB3
24	VMV3
25	GNDQ
26	GEA2/IO97RSB2
27	FF/GEB2/IO96RSB2
28	GEC2/IO95RSB2
29	IO93RSB2
30	IO92RSB2
31	IO91RSB2
32	IO90RSB2
33	IO88RSB2
34	IO86RSB2
35	IO85RSB2
36	IO84RSB2

100-Pin VQFP	
Pin Number	A3P250L Function
37	V_{CC}
38	GND
39	V_{CCI}B2
40	IO77RSB2
41	IO74RSB2
42	IO71RSB2
43	GDC2/IO63RSB2
44	GDB2/IO62RSB2
45	GDA2/IO61RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	V_{PUMP}
53	NC
54	TDO
55	TRST
56	V_{JTAG}
57	GDA1/IO60USB1
58	GDC0/IO58VDB1
59	GDC1/IO58UDB1
60	IO52NDB1
61	GCB2/IO52PDB1
62	GCA1/IO50PDB1
63	GCA0/IO50NDB1
64	GCC0/IO48NDB1
65	GCC1/IO48PDB1
66	V_{CCI}B1
67	GND
68	V_{CC}
69	IO43NDB1
70	GBC2/IO43PDB1
71	GBB2/IO42PSB1
72	IO41NDB1

100-Pin VQFP	
Pin Number	A3P250L Function
73	GBA2/IO41PDB1
74	VMV1
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO29RSB0
83	IO27RSB0
84	IO25RSB0
85	IO23RSB0
86	IO21RSB0
87	V_{CCI}B0
88	GND
89	V_{CC}
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

208-Pin PQFP



Note: This is the top view of the package.

Figure 3-2 •

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

208-Pin PQFP	
Pin Number	A3PL600 Function
1	GND
2	GAA2/IO174PDB3
3	IO174NDB3
4	GAB2/IO173PDB3
5	IO173NDB3
6	GAC2/IO172PDB3
7	IO172NDB3
8	IO171PDB3
9	IO171NDB3
10	IO170PDB3
11	IO170NDB3
12	IO169PDB3
13	IO169NDB3
14	IO168PDB3
15	IO168NDB3
16	V_{CC}
17	GND
18	V_{CCI}B3
19	IO166PDB3
20	IO166NDB3
21	GFC1/IO164PDB3
22	GFC0/IO164NDB3
23	GFB1/IO163PDB3
24	GFB0/IO163NDB3
25	V_{COMPLF}
26	GFA0/IO162NPB3
27	V_{CCPLF}
28	GFA1/IO162PPB3
29	GND
30	GFA2/IO161PDB3
31	IO161NDB3
32	GFB2/IO160PDB3
33	IO160NDB3
34	GFC2/IO159PDB3
35	IO159NDB3
36	V_{CC}

208-Pin PQFP	
Pin Number	A3PL600 Function
37	IO152PDB3
38	IO152NDB3
39	IO150PSB3
40	V_{CCI}B3
41	GND
42	IO147PDB3
43	IO147NDB3
44	GEC1/IO146PDB3
45	GEC0/IO146NDB3
46	GEB1/IO145PDB3
47	GEB0/IO145NDB3
48	GEA1/IO144PDB3
49	GEA0/IO144NDB3
50	VMV3
51	GNDQ
52	GND
53	VMV2
54	GEA2/IO143RSB2
55	FF/GEB2/IO142RSB2
56	GEC2/IO141RSB2
57	IO140RSB2
58	IO139RSB2
59	IO138RSB2
60	IO137RSB2
61	IO136RSB2
62	V_{CCI}B2
63	IO135RSB2
64	IO133RSB2
65	GND
66	IO131RSB2
67	IO129RSB2
68	IO127RSB2
69	IO125RSB2
70	IO123RSB2
71	V_{CC}
72	V_{CCI}B2

208-Pin PQFP	
Pin Number	A3PL600 Function
73	IO120RSB2
74	IO119RSB2
75	IO118RSB2
76	IO117RSB2
77	IO116RSB2
78	IO115RSB2
79	IO114RSB2
80	IO112RSB2
81	GND
82	IO111RSB2
83	IO110RSB2
84	IO109RSB2
85	IO108RSB2
86	IO107RSB2
87	IO106RSB2
88	V_{CC}
89	V_{CCI}B2
90	IO104RSB2
91	IO102RSB2
92	IO100RSB2
93	IO98RSB2
94	IO96RSB2
95	IO92RSB2
96	GDC2/IO91RSB2
97	GND
98	GDB2/IO90RSB2
99	GDA2/IO89RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	V_{PUMP}
107	GNDQ
108	TDO

208-Pin PQFP	
Pin Number	A3PL600 Function
109	TRST
110	V_{JTAG}
111	GDA0/IO88NDB1
112	GDA1/IO88PDB1
113	GDB0/IO87NDB1
114	GDB1/IO87PDB1
115	GDC0/IO86NDB1
116	GDC1/IO86PDB1
117	IO84NDB1
118	IO84PDB1
119	IO82NDB1
120	IO82PDB1
121	IO81PSB1
122	GND
123	V_{CCI}B1
124	IO77NDB1
125	IO77PDB1
126	NC
127	IO74NDB1
128	GCC2/IO74PDB1
129	GCB2/IO73PSB1
130	GND
131	GCA2/IO72PSB1
132	GCA1/IO71PDB1
133	GCA0/IO71NDB1
134	GCB0/IO70NDB1
135	GCB1/IO70PDB1
136	GCC0/IO69NDB1
137	GCC1/IO69PDB1
138	IO67NDB1
139	IO67PDB1
140	V_{CCI}B1
141	GND
142	V_{CC}
143	IO65PSB1
144	IO64NDB1

208-Pin PQFP	
Pin Number	A3PL600 Function
145	IO64PDB1
146	IO63NDB1
147	IO63PDB1
148	IO62NDB1
149	GBC2/IO62PDB1
150	IO61NDB1
151	GBB2/IO61PDB1
152	IO60NDB1
153	GBA2/IO60PDB1
154	VMV1
155	GNDQ
156	GND
157	VMV0
158	GBA1/IO59RSB0
159	GBA0/IO58RSB0
160	GBB1/IO57RSB0
161	GBB0/IO56RSB0
162	GND
163	GBC1/IO55RSB0
164	GBC0/IO54RSB0
165	IO52RSB0
166	IO50RSB0
167	IO48RSB0
168	IO46RSB0
169	IO44RSB0
170	V_{CCI}B0
171	V_{CC}
172	IO36RSB0
173	IO35RSB0
174	IO34RSB0
175	IO33RSB0
176	IO32RSB0
177	IO31RSB0
178	GND
179	IO29RSB0
180	IO28RSB0

208-Pin PQFP	
Pin Number	A3PL600 Function
181	IO27RSB0
182	IO26RSB0
183	IO25RSB0
184	IO24RSB0
185	IO23RSB0
186	V_{CCI}B0
187	V_{CC}
188	IO20RSB0
189	IO19RSB0
190	IO18RSB0
191	IO17RSB0
192	IO16RSB0
193	IO14RSB0
194	IO12RSB0
195	GND
196	IO10RSB0
197	IO09RSB0
198	IO08RSB0
199	IO07RSB0
200	V_{CCI}B0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

208-Pin PQFP	
Pin Number	A3PL250 Function
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO115UDB3
9	IO115VDB3
10	IO114UDB3
11	IO114VDB3
12	IO113PDB3
13	IO113NDB3
14	IO112PDB3
15	IO112NDB3
16	V_{CC}
17	GND
18	V_{CCI}B3
19	IO111PDB3
20	IO111NDB3
21	GFC1/IO110PDB3
22	GFC0/IO110NDB3
23	GFB1/IO109PDB3
24	GFB0/IO109NDB3
25	V_{COMPLF}
26	GFA0/IO108NPB3
27	V_{CCPLF}
28	GFA1/IO108PPB3
29	GND
30	GFA2/IO107PDB3
31	IO107NDB3
32	GFB2/IO106PDB3
33	IO106NDB3
34	GFC2/IO105PDB3
35	IO105NDB3
36	NC

208-Pin PQFP	
Pin Number	A3PL250 Function
37	IO104PDB3
38	IO104NDB3
39	IO103PSB3
40	V_{CCI}B3
41	GND
42	IO101PDB3
43	IO101NDB3
44	GEC1/IO100PDB3
45	GEC0/IO100NDB3
46	GEB1/IO99PDB3
47	GEB0/IO99NDB3
48	GEA1/IO98PDB3
49	GEA0/IO98NDB3
50	VMV3
51	GNDQ
52	GND
53	NC
54	NC
55	GEA2/IO97RSB2
56	FF/GEB2/IO96RSB2
57	GEC2/IO95RSB2
58	IO94RSB2
59	IO93RSB2
60	IO92RSB2
61	IO91RSB2
62	V_{CCI}B2
63	IO90RSB2
64	IO89RSB2
65	GND
66	IO88RSB2
67	IO87RSB2
68	IO86RSB2
69	IO85RSB2
70	IO84RSB2
71	V_{CC}
72	V_{CCI}B2

208-Pin PQFP	
Pin Number	A3PL250 Function
73	IO83RSB2
74	IO82RSB2
75	IO81RSB2
76	IO80RSB2
77	IO79RSB2
78	IO78RSB2
79	IO77RSB2
80	IO76RSB2
81	GND
82	IO75RSB2
83	IO74RSB2
84	IO73RSB2
85	IO72RSB2
86	IO71RSB2
87	IO70RSB2
88	V_{CC}
89	V_{CCI}B2
90	IO69RSB2
91	IO68RSB2
92	IO67RSB2
93	IO66RSB2
94	IO65RSB2
95	IO64RSB2
96	GDC2/IO63RSB2
97	GND
98	GDB2/IO62RSB2
99	GDA2/IO61RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	V_{PUMP}
107	NC
108	TDO

208-Pin PQFP	
Pin Number	A3PL250 Function
109	TRST
110	V_{JTAG}
111	GDA0/IO60VDB1
112	GDA1/IO60UDB1
113	GDB0/IO59VDB1
114	GDB1/IO59UDB1
115	GDC0/IO58VDB1
116	GDC1/IO58UDB1
117	IO57VDB1
118	IO57UDB1
119	IO56NDB1
120	IO56PDB1
121	IO55RSB1
122	GND
123	V_{CCI}B1
124	NC
125	NC
126	V_{CC}
127	IO53NDB1
128	GCC2/IO53PDB1
129	GCB2/IO52PSB1
130	GND
131	GCA2/IO51PSB1
132	GCA1/IO50PDB1
133	GCA0/IO50NDB1
134	GCB0/IO49NDB1
135	GCB1/IO49PDB1
136	GCC0/IO48NDB1
137	GCC1/IO48PDB1
138	IO47NDB1
139	IO47PDB1
140	V_{CCI}B1
141	GND
142	V_{CC}
143	IO46RSB1
144	IO45NDB1

208-Pin PQFP	
Pin Number	A3PL250 Function
145	IO45PDB1
146	IO44NDB1
147	IO44PDB1
148	IO43NDB1
149	GBC2/IO43PDB1
150	IO42NDB1
151	GBB2/IO42PDB1
152	IO41NDB1
153	GBA2/IO41PDB1
154	VMV1
155	GNDQ
156	GND
157	NC
158	GBA1/IO40RSB0
159	GBA0/IO39RSB0
160	GBB1/IO38RSB0
161	GBB0/IO37RSB0
162	GND
163	GBC1/IO36RSB0
164	GBC0/IO35RSB0
165	IO34RSB0
166	IO33RSB0
167	IO32RSB0
168	IO31RSB0
169	IO30RSB0
170	V_{CCI}B0
171	V_{CC}
172	IO29RSB0
173	IO28RSB0
174	IO27RSB0
175	IO26RSB0
176	IO25RSB0
177	IO24RSB0
178	GND
179	IO23RSB0
180	IO22RSB0

208-Pin PQFP	
Pin Number	A3PL250 Function
181	IO21RSB0
182	IO20RSB0
183	IO19RSB0
184	IO18RSB0
185	IO17RSB0
186	V_{CCI}B0
187	V_{CC}
188	IO16RSB0
189	IO15RSB0
190	IO14RSB0
191	IO13RSB0
192	IO12RSB0
193	IO11RSB0
194	IO10RSB0
195	GND
196	IO09RSB0
197	IO08RSB0
198	IO07RSB0
199	IO06RSB0
200	V_{CCI}B0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

208-Pin PQFP	
Pin Number	APL1000 Function
1	GND
2	GAA2/IO225PDB3
3	IO225NDB3
4	GAB2/IO224PDB3
5	IO224NDB3
6	GAC2/IO223PDB3
7	IO223NDB3
8	IO222PDB3
9	IO222NDB3
10	IO220PDB3
11	IO220NDB3
12	IO218PDB3
13	IO218NDB3
14	IO216PDB3
15	IO216NDB3
16	V_{CC}
17	GND
18	V_{CCI}B3
19	IO212PDB3
20	IO212NDB3
21	GFC1/IO209PDB3
22	GFC0/IO209NDB3
23	GFB1/IO208PDB3
24	GFB0/IO208NDB3
25	V_{COMPLF}
26	GFA0/IO207NPB3
27	V_{CCPLF}
28	GFA1/IO207PPB3
29	GND
30	GFA2/IO206PDB3
31	IO206NDB3
32	GFB2/IO205PDB3
33	IO205NDB3
34	GFC2/IO204PDB3
35	IO204NDB3
36	V_{CC}

208-Pin PQFP	
Pin Number	APL1000 Function
37	IO199PDB3
38	IO199NDB3
39	IO197PSB3
40	V_{CCI}B3
41	GND
42	IO191PDB3
43	IO191NDB3
44	GEC1/IO190PDB3
45	GEC0/IO190NDB3
46	GEB1/IO189PDB3
47	GEB0/IO189NDB3
48	GEA1/IO188PDB3
49	GEA0/IO188NDB3
50	VMV3
51	GNDQ
52	GND
53	VMV2
54	GEA2/IO187RSB2
55	FF/GEB2/IO186RSB2
56	GEC2/IO185RSB2
57	IO184RSB2
58	IO183RSB2
59	IO182RSB2
60	IO181RSB2
61	IO180RSB2
62	V_{CCI}B2
63	IO178RSB2
64	IO176RSB2
65	GND
66	IO174RSB2
67	IO172RSB2
68	IO170RSB2
69	IO168RSB2
70	IO166RSB2
71	V_{CC}
72	V_{CCI}B2

208-Pin PQFP	
Pin Number	APL1000 Function
73	IO162RSB2
74	IO160RSB2
75	IO158RSB2
76	IO156RSB2
77	IO154RSB2
78	IO152RSB2
79	IO150RSB2
80	IO148RSB2
81	GND
82	IO143RSB2
83	IO141RSB2
84	IO139RSB2
85	IO137RSB2
86	IO135RSB2
87	IO133RSB2
88	V_{CC}
89	V_{CCI}B2
90	IO128RSB2
91	IO126RSB2
92	IO124RSB2
93	IO122RSB2
94	IO120RSB2
95	IO118RSB2
96	GDC2/IO116RSB2
97	GND
98	GDB2/IO115RSB2
99	GDA2/IO114RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	V_{PUMP}
107	GNDQ
108	TDO

208-Pin PQFP	
Pin Number	APL1000 Function
109	TRST
110	V_{JTAG}
111	GDA0/IO113NDB1
112	GDA1/IO113PDB1
113	GDB0/IO112NDB1
114	GDB1/IO112PDB1
115	GDC0/IO111NDB1
116	GDC1/IO111PDB1
117	IO109NDB1
118	IO109PDB1
119	IO106NDB1
120	IO106PDB1
121	IO104PSB1
122	GND
123	V_{CCI}B1
124	IO99NDB1
125	IO99PDB1
126	NC
127	IO96NDB1
128	GCC2/IO96PDB1
129	GCB2/IO95PSB1
130	GND
131	GCA2/IO94PSB1
132	GCA1/IO93PDB1
133	GCA0/IO93NDB1
134	GCB0/IO92NDB1
135	GCB1/IO92PDB1
136	GCC0/IO91NDB1
137	GCC1/IO91PDB1
138	IO88NDB1
139	IO88PDB1
140	V_{CCI}B1
141	GND
142	V_{CC}
143	IO86PSB1
144	IO84NDB1

208-Pin PQFP	
Pin Number	APL1000 Function
145	IO84PDB1
146	IO82NDB1
147	IO82PDB1
148	IO80NDB1
149	GBC2/IO80PDB1
150	IO79NDB1
151	GBB2/IO79PDB1
152	IO78NDB1
153	GBA2/IO78PDB1
154	VMV1
155	GNDQ
156	GND
157	VMV0
158	GBA1/IO77RSB0
159	GBA0/IO76RSB0
160	GBB1/IO75RSB0
161	GBB0/IO74RSB0
162	GND
163	GBC1/IO73RSB0
164	GBC0/IO72RSB0
165	IO70RSB0
166	IO67RSB0
167	IO63RSB0
168	IO60RSB0
169	IO57RSB0
170	V_{CCI}B0
171	V_{CC}
172	IO54RSB0
173	IO51RSB0
174	IO48RSB0
175	IO45RSB0
176	IO42RSB0
177	IO40RSB0
178	GND
179	IO38RSB0
180	IO35RSB0

208-Pin PQFP	
Pin Number	APL1000 Function
181	IO33RSB0
182	IO31RSB0
183	IO29RSB0
184	IO27RSB0
185	IO25RSB0
186	V_{CCI}B0
187	V_{CC}
188	IO22RSB0
189	IO20RSB0
190	IO18RSB0
191	IO16RSB0
192	IO15RSB0
193	IO14RSB0
194	IO13RSB0
195	GND
196	IO12RSB0
197	IO11RSB0
198	IO10RSB0
199	IO09RSB0
200	V_{CCI}B0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

208-Pin PQFP	
Pin Number	A3PE3000L Function
1	GND
2	GNDQ
3	VMV7
4	GAB2/IO308PSB7V4
5	GAA2/IO309PDB7V4
6	IO309NDB7V4
7	GAC2/IO307PDB7V4
8	IO307NDB7V4
9	IO303PDB7V3
10	IO303NDB7V3
11	IO299PDB7V3
12	IO299NDB7V3
13	IO295PDB7V2
14	IO295NDB7V2
15	IO291PSB7V2
16	V_{CC}
17	GND
18	V_{CCI}B7
19	IO285PDB7V1
20	IO285NDB7V1
21	IO279PSB7V0
22	GFC1/IO275PSB7V0
23	GFB1/IO274PDB7V0
24	GFB0/IO274NDB7V0
25	V_{COMPLF}
26	GFA0/IO273NPB6V4
27	V_{CCPLF}
28	GFA1/IO273PPB6V4
29	GND
30	GFA2/IO272PDB6V4
31	IO272NDB6V4
32	GFB2/IO271PPB6V4
33	GFC2/IO270PPB6V4
34	IO271NPB6V4
35	IO270NPB6V4
36	V_{CC}
36	V_{CC}

208-Pin PQFP	
Pin Number	A3PE3000L Function
37	IO252PDB6V2
38	IO252NDB6V2
39	IO248PSB6V1
40	V_{CCI}B6
41	GND
42	IO244PDB6V1
43	IO244NDB6V1
44	GEC1/IO236PDB6V0
45	GEC0/IO236NDB6V0
46	GEB1/IO235PPB6V0
47	GEA1/IO234PPB6V0
48	GEB0/IO235NPB6V0
49	GEA0/IO234NPB6V0
50	VMV6
51	GNDQ
52	GND
53	VMV5
54	GNDQ
55	IO233NDB5V4
56	GEA2/IO233PDB5V4
57	IO232NDB5V4
58	FF/GEB2/IO232PDB5V4
59	IO231NDB5V4
60	GEC2/IO231PDB5V4
61	IO230PSB5V4
62	V_{CCI}B5
62	V_{CCI}B5
63	IO218NDB5V3
64	IO218PDB5V3
65	GND
66	IO214PSB5V2
67	IO212NDB5V2
68	IO212PDB5V2
69	IO208NDB5V1
70	IO208PDB5V1
71	V_{CC}

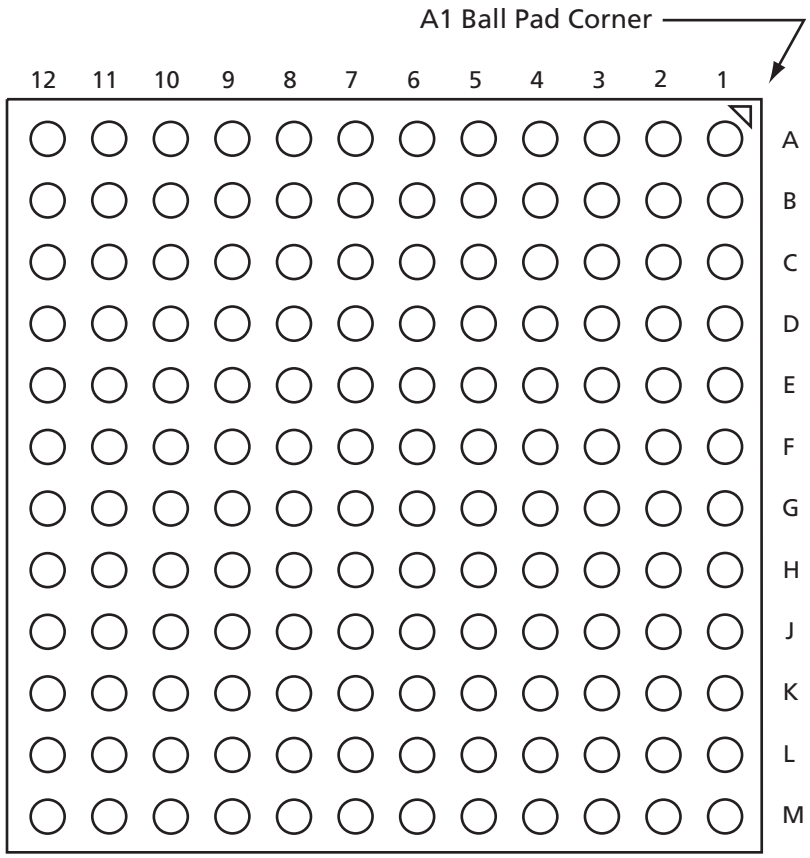
208-Pin PQFP	
Pin Number	A3PE3000L Function
72	V_{CCI}B5
73	IO202NDB5V1
74	IO202PDB5V1
75	IO198NDB5V0
76	IO198PDB5V0
77	IO197NDB5V0
78	IO197PDB5V0
79	IO194NDB5V0
80	IO194PDB5V0
81	GND
82	IO184NDB4V3
83	IO184PDB4V3
84	IO180NDB4V3
85	IO180PDB4V3
86	IO176NDB4V2
87	IO176PDB4V2
88	V_{CC}
89	V_{CCI}B4
90	IO170NDB4V2
91	IO170PDB4V2
92	IO166NDB4V1
93	IO166PDB4V1
94	IO156NDB4V0
95	GDC2/IO156PDB4V0
96	IO154NPB4V0
97	GND
98	GDB2/IO155PSB4V0
99	GDA2/IO154PPB4V0
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV4
105	GND
106	V_{PUMP}
107	GNDQ
108	TDO

208-Pin PQFP	
Pin Number	A3PE3000L Function
109	TRST
110	V_{JTAG}
111	VMV3
112	GDA0/IO153NPB3V4
113	GDB0/IO152NPB3V4
114	GDA1/IO153PPB3V4
115	GDB1/IO152PPB3V4
116	GDC0/IO151NDB3V4
117	GDC1/IO151PDB3V4
118	IO134NDB3V2
119	IO134PDB3V2
120	IO132NDB3V2
121	IO132PDB3V2
122	GND
123	V_{CCI}B3
124	GCC2/IO117PSB3V0
125	GCB2/IO116PSB3V0
126	NC
127	IO115NDB3V0
128	GCA2/IO115PDB3V0
129	GCA1/IO114PPB3V0
130	GND
131	V_{CCPLC}
132	GCA0/IO114NPB3V0
133	V_{COMPLC}
134	GCB0/IO113NDB2V3
135	GCB1/IO113PDB2V3
136	GCC1/IO112PSB2V3
137	IO110NDB2V3
138	IO110PDB2V3
139	IO106PSB2V3
140	V_{CCI}B2
141	GND
142	V_{CC}
143	IO99NDB2V2
144	IO99PDB2V2
145	IO96NDB2V1

208-Pin PQFP	
Pin Number	A3PE3000L Function
146	IO96PDB2V1
147	IO91NDB2V1
148	IO91PDB2V1
149	IO88NDB2V0
150	IO88PDB2V0
151	GBC2/IO84PSB2V0
152	GBA2/IO82PSB2V0
153	GBB2/IO83PSB2V0
154	VMV2
155	GNDQ
156	GND
157	VMV1
158	GNDQ
159	GBA1/IO81PDB1V4
160	GBA0/IO81NDB1V4
161	GBB1/IO80PDB1V4
162	GND
163	GBB0/IO80NDB1V4
164	GBC1/IO79PDB1V4
165	GBC0/IO79NDB1V4
166	IO74PDB1V4
167	IO74NDB1V4
168	IO70PDB1V3
169	IO70NDB1V3
170	V_{CCI}B1
171	V_{CC}
171	V_{CC}
172	IO56PSB1V1
173	IO55PDB1V1
174	IO55NDB1V1
175	IO54PDB1V1
176	IO54NDB1V1
177	IO40PDB0V4
178	GND
179	IO40NDB0V4
180	IO37PDB0V4
181	IO37NDB0V4

208-Pin PQFP	
Pin Number	A3PE3000L Function
182	IO35PDB0V4
183	IO35NDB0V4
184	IO32PDB0V3
185	IO32NDB0V3
186	V_{CCI}B0
187	V_{CC}
188	IO28PDB0V3
189	IO28NDB0V3
190	IO24PDB0V2
191	IO24NDB0V2
192	IO21PSB0V2
193	IO16PDB0V1
194	IO16NDB0V1
195	GND
196	IO11PDB0V1
197	IO11NDB0V1
198	IO08PDB0V0
199	IO08NDB0V0
200	V_{CCI}B0
201	GAC1/IO02PDB0V0
202	GAC0/IO02NDB0V0
203	GAB1/IO01PDB0V0
204	GAB0/IO01NDB0V0
205	GAA1/IO00PDB0V0
206	GAA0/IO00NDB0V0
207	GNDQ
208	VMV0

144-Pin FBGA



Note: This is the bottom view of the package.

Figure 3-3 •

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

144-Pin FBGA	
Pin Number	A3P250L Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO16RSB0
A6	GND
A7	IO29RSB0
A8	V_{CC}
A9	IO33RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO117UDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO14RSB0
B6	IO19RSB0
B7	IO22RSB0
B8	IO30RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV1
C1	IO117VDB3
C2	GFA2/IO107PPB3
C3	GAC2/IO116UDB3
C4	V_{CC}
C5	IO12RSB0
C6	IO17RSB0
C7	IO24RSB0
C8	IO31RSB0
C9	IO34RSB0
C10	GBA2/IO41PDB1
C11	IO41NDB1
C12	GBC2/IO43PPB1

144-Pin FBGA	
Pin Number	A3P250L Function
D1	IO112NDB3
D2	IO112PDB3
D3	IO116VDB3
D4	GAA2/IO118UPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO42PDB1
D10	IO42NDB1
D11	IO43NPB1
D12	GCB1/IO49PPB1
E1	V_{CC}
E2	GFC0/IO110NDB3
E3	GFC1/IO110PDB3
E4	V_{CCI}B3
E5	IO118VPB3
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	GCC1/IO48PDB1
E9	V_{CCI}B1
E10	V_{CC}
E11	GCA0/IO50NDB1
E12	IO51NDB1
F1	GFB0/IO109NPB3
F2	V_{COMPLF}
F3	GFB1/IO109PPB3
F4	IO107NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO48NDB1
F9	GCB0/IO49NPB1
F10	GND
F11	GCA1/IO50PDB1
F12	GCA2/IO51PDB1

144-Pin FBGA	
Pin Number	A3P250L Function
G1	GFA1/IO108PPB3
G2	GND
G3	V_{CCPLF}
G4	GFA0/IO108NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO58UPB1
G9	IO53NDB1
G10	GCC2/IO53PDB1
G11	IO52NDB1
G12	GCB2/IO52PDB1
H1	V_{CC}
H2	GFB2/IO106PDB3
H3	GFC2/IO105PSB3
H4	GEC1/IO100PDB3
H5	V_{CC}
H6	IO79RSB2
H7	IO65RSB2
H8	GDB2/IO62RSB2
H9	GDC0/IO58VPB1
H10	V_{CCI}B1
H11	IO54PSB1
H12	V_{CC}
J1	GEB1/IO99PDB3
J2	IO106NDB3
J3	V_{CCI}B3
J4	GEC0/IO100NDB3
J5	IO88RSB2
J6	IO81RSB2
J7	V_{CC}
J8	TCK
J9	GDA2/IO61RSB2
J10	TDO
J11	GDA1/IO60UDB1
J12	GDB1/IO59UDB1

144-Pin FBGA	
Pin Number	**A3P250L Function**
K1	GEB0/IO99NDB3
K2	GEA1/IO98PDB3
K3	GEA0/IO98NDB3
K4	GEA2/IO97RSB2
K5	IO90RSB2
K6	IO84RSB2
K7	GND
K8	IO66RSB2
K9	GDC2/IO63RSB2
K10	GND
K11	GDA0/IO60VDB1
K12	GDB0/IO59VDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO96RSB2
L4	IO91RSB2
L5	V_{CCI}B2
L6	IO82RSB2
L7	IO80RSB2
L8	IO72RSB2
L9	TMS
L10	V_{JTAG}
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO95RSB2
M3	IO92RSB2
M4	IO89RSB2
M5	IO87RSB2
M6	IO85RSB2
M7	IO78RSB2
M8	IO76RSB2
M9	TDI
M10	V_{CCI}B2
M11	V_{PUMP}
M12	GNDQ

144-Pin FBGA	
Pin Number	A3P600L Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO34RSB0
A8	V_{CC}
A9	IO50RSB0
A10	GBA0/IO58RSB0
A11	GBA1/IO59RSB0
A12	GNDQ
B1	GAB2/IO173PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO19RSB0
B7	IO31RSB0
B8	IO39RSB0
B9	GBB0/IO56RSB0
B10	GBB1/IO57RSB0
B11	GND
B12	VMV1
C1	IO173NDB3
C2	GFA2/IO161PPB3
C3	GAC2/IO172PDB3
C4	V_{CC}
C5	IO16RSB0
C6	IO25RSB0
C7	IO28RSB0
C8	IO42RSB0
C9	IO45RSB0
C10	GBA2/IO60PDB1
C11	IO60NDB1
C12	GBC2/IO62PPB1

144-Pin FBGA	
Pin Number	A3P600L Function
D1	IO169PDB3
D2	IO169NDB3
D3	IO172NDB3
D4	GAA2/IO174PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO54RSB0
D8	GBC1/IO55RSB0
D9	GBB2/IO61PDB1
D10	IO61NDB1
D11	IO62NPB1
D12	GCB1/IO70PPB1
E1	V_{CC}
E2	GFC0/IO164NDB3
E3	GFC1/IO164PDB3
E4	V_{CCI}B3
E5	IO174NPB3
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	GCC1/IO69PDB1
E9	V_{CCI}B1
E10	V_{CC}
E11	GCA0/IO71NDB1
E12	IO72NDB1
F1	GFB0/IO163NPB3
F2	V_{COMPLF}
F3	GFB1/IO163PPB3
F4	IO161NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO69NDB1
F9	GCB0/IO70NPB1
F10	GND
F11	GCA1/IO71PDB1
F12	GCA2/IO72PDB1

144-Pin FBGA	
Pin Number	A3P600L Function
G1	GFA1/IO162PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO162NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO86PPB1
G9	IO74NDB1
G10	GCC2/IO74PDB1
G11	IO73NDB1
G12	GCB2/IO73PDB1
H1	V_{CC}
H2	GFB2/IO160PDB3
H3	GFC2/IO159PSB3
H4	GEC1/IO146PDB3
H5	V_{CC}
H6	IO80PDB1
H7	IO80NDB1
H8	GDB2/IO90RSB2
H9	GDC0/IO86NPB1
H10	V_{CCI}B1
H11	IO84PSB1
H12	V_{CC}
J1	GEB1/IO145PDB3
J2	IO160NDB3
J3	V_{CCI}B3
J4	GEC0/IO146NDB3
J5	IO129RSB2
J6	IO131RSB2
J7	V_{CC}
J8	TCK
J9	GDA2/IO89RSB2
J10	TDO
J11	GDA1/IO88PDB1
J12	GDB1/IO87PDB1

144-Pin FBGA	
Pin Number	**A3P600L Function**
K1	GEB0/IO145NDB3
K2	GEA1/IO144PDB3
K3	GEA0/IO144NDB3
K4	GEA2/IO143RSB2
K5	IO119RSB2
K6	IO111RSB2
K7	GND
K8	IO94RSB2
K9	GDC2/IO91RSB2
K10	GND
K11	GDA0/IO88NDB1
K12	GDB0/IO87NDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO142RSB2
L4	IO136RSB2
L5	V_{CCI}B2
L6	IO115RSB2
L7	IO103RSB2
L8	IO97RSB2
L9	TMS
L10	V_{JTAG}
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO141RSB2
M3	IO138RSB2
M4	IO123RSB2
M5	IO126RSB2
M6	IO134RSB2
M7	IO108RSB2
M8	IO99RSB2
M9	TDI
M10	V_{CCI}B2
M11	V_{PUMP}
M12	GNDQ

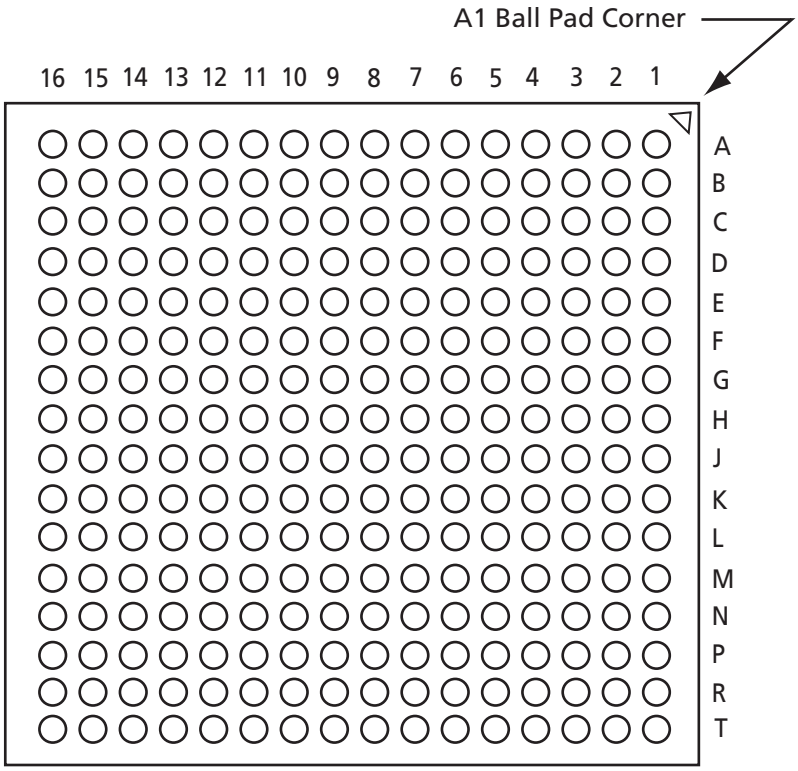
144-Pin FBGA	
Pin Number	A3P1000L Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO44RSB0
A8	V_{CC}
A9	IO69RSB0
A10	GBA0/IO76RSB0
A11	GBA1/IO77RSB0
A12	GNDQ
B1	GAB2/IO224PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO26RSB0
B7	IO35RSB0
B8	IO60RSB0
B9	GBB0/IO74RSB0
B10	GBB1/IO75RSB0
B11	GND
B12	VMV1
C1	IO224NDB3
C2	GFA2/IO206PPB3
C3	GAC2/IO223PDB3
C4	V_{CC}
C5	IO16RSB0
C6	IO29RSB0
C7	IO32RSB0
C8	IO63RSB0
C9	IO66RSB0
C10	GBA2/IO78PDB1
C11	IO78NDB1
C12	GBC2/IO80PPB1

144-Pin FBGA	
Pin Number	A3P1000L Function
D1	IO213PDB3
D2	IO213NDB3
D3	IO223NDB3
D4	GAA2/IO225PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO72RSB0
D8	GBC1/IO73RSB0
D9	GBB2/IO79PDB1
D10	IO79NDB1
D11	IO80NPB1
D12	GCB1/IO92PPB1
E1	V_{CC}
E2	GFC0/IO209NDB3
E3	GFC1/IO209PDB3
E4	V_{CCI}B3
E5	IO225NPB3
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	GCC1/IO91PDB1
E9	V_{CCI}B1
E10	V_{CC}
E11	GCA0/IO93NDB1
E12	IO94NDB1
F1	GFB0/IO208NPB3
F2	V_{COMPLF}
F3	GFB1/IO208PPB3
F4	IO206NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO91NDB1
F9	GCB0/IO92NPB1
F10	GND
F11	GCA1/IO93PDB1
F12	GCA2/IO94PDB1

144-Pin FBGA	
Pin Number	A3P1000L Function
G1	GFA1/IO207PPB3
G2	GND
G3	V_{CCPLF}
G4	GFA0/IO207NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO111PPB1
G9	IO96NDB1
G10	GCC2/IO96PDB1
G11	IO95NDB1
G12	GCB2/IO95PDB1
H1	V_{CC}
H2	GFB2/IO205PDB3
H3	GFC2/IO204PSB3
H4	GEC1/IO190PDB3
H5	V_{CC}
H6	IO105PDB1
H7	IO105NDB1
H8	GDB2/IO115RSB2
H9	GDC0/IO111NPB1
H10	V_{CCI}B1
H11	IO101PSB1
H12	V_{CC}
J1	GEB1/IO189PDB3
J2	IO205NDB3
J3	V_{CCI}B3
J4	GEC0/IO190NDB3
J5	IO160RSB2
J6	IO157RSB2
J7	V_{CC}
J8	TCK
J9	GDA2/IO114RSB2
J10	TDO
J11	GDA1/IO113PDB1
J12	GDB1/IO112PDB1

144-Pin FBGA	
Pin Number	**A3P1000L Function**
K1	GEB0/IO189NDB3
K2	GEA1/IO188PDB3
K3	GEA0/IO188NDB3
K4	GEA2/IO187RSB2
K5	IO169RSB2
K6	IO152RSB2
K7	GND
K8	IO117RSB2
K9	GDC2/IO116RSB2
K10	GND
K11	GDA0/IO113NDB1
K12	GDB0/IO112NDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO186RSB2
L4	IO172RSB2
L5	V_{CCI}B2
L6	IO153RSB2
L7	IO144RSB2
L8	IO140RSB2
L9	TMS
L10	V_{JTAG}
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO185RSB2
M3	IO173RSB2
M4	IO168RSB2
M5	IO161RSB2
M6	IO156RSB2
M7	IO145RSB2
M8	IO141RSB2
M9	TDI
M10	V_{CCI}B2
M11	V_{PUMP}
M12	GNDQ

256-Pin FBGA



Note: This is the bottom view of the package.

Figure 3-4 •

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

256-Pin FBGA	
Pin Number	A3P250L Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO07RSB0
A6	IO10RSB0
A7	IO11RSB0
A8	IO15RSB0
A9	IO20RSB0
A10	IO25RSB0
A11	IO29RSB0
A12	IO33RSB0
A13	GBB1/IO38RSB0
A14	GBA0/IO39RSB0
A15	GBA1/IO40RSB0
A16	GND
B1	GAB2/IO117UDB3
B2	GAA2/IO118UDB3
B3	NC
B4	GAB1/IO03RSB0
B5	IO06RSB0
B6	IO09RSB0
B7	IO12RSB0
B8	IO16RSB0
B9	IO21RSB0
B10	IO26RSB0
B11	IO30RSB0
B12	GBC1/IO36RSB0
B13	GBB0/IO37RSB0
B14	NC
B15	GBA2/IO41PDB1
B16	IO41NDB1
C1	IO117VDB3
C2	IO118VDB3
C3	NC
C4	NC

256-Pin FBGA	
Pin Number	A3P250L Function
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO13RSB0
C8	IO17RSB0
C9	IO22RSB0
C10	IO27RSB0
C11	IO31RSB0
C12	GBC0/IO35RSB0
C13	IO34RSB0
C14	NC
C15	IO42NPB1
C16	IO44PDB1
D1	IO114VDB3
D2	IO114UDB3
D3	GAC2/IO116UDB3
D4	NC
D5	GNDQ
D6	IO08RSB0
D7	IO14RSB0
D8	IO18RSB0
D9	IO23RSB0
D10	IO28RSB0
D11	IO32RSB0
D12	GNDQ
D13	NC
D14	GBB2/IO42PPB1
D15	NC
D16	IO44NDB1
E1	IO113PDB3
E2	NC
E3	IO116VDB3
E4	IO115UDB3
E5	VMV0
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	IO19RSB0

256-Pin FBGA	
Pin Number	A3P250L Function
E9	IO24RSB0
E10	V_{CCI}B0
E11	V_{CCI}B0
E12	VMV1
E13	GBC2/IO43PDB1
E14	IO46RSB1
E15	NC
E16	IO45PDB1
F1	IO113NDB3
F2	IO112PPB3
F3	NC
F4	IO115VDB3
F5	V_{CCI}B3
F6	GND
F7	V_{CC}
F8	V_{CC}
F9	V_{CC}
F10	V_{CC}
F11	GND
F12	V_{CCI}B1
F13	IO43NDB1
F14	NC
F15	IO47PPB1
F16	IO45NDB1
G1	IO111NDB3
G2	IO111PDB3
G3	IO112NPB3
G4	GFC1/IO110PPB3
G5	V_{CCI}B3
G6	V_{CC}
G7	GND
G8	GND
G9	GND
G10	GND
G11	V_{CC}
G12	V_{CCI}B1

256-Pin FBGA	
Pin Number	A3P250L Function
G13	GCC1/IO48PPB1
G14	IO47NPB1
G15	IO54PDB1
G16	IO54NDB1
H1	GFB0/IO109NPB3
H2	GFA0/IO108NDB3
H3	GFB1/IO109PPB3
H4	V_{COMPLF}
H5	GFC0/IO110NPB3
H6	V_{CC}
H7	GND
H8	GND
H9	GND
H10	GND
H11	V_{CC}
H12	GCC0/IO48NPB1
H13	GCB1/IO49PPB1
H14	GCA0/IO50NPB1
H15	NC
H16	GCB0/IO49NPB1
J1	GFA2/IO107PPB3
J2	GFA1/IO108PDB3
J3	V_{CCPLF}
J4	IO106NDB3
J5	GFB2/IO106PDB3
J6	V_{CC}
J7	GND
J8	GND
J9	GND
J10	GND
J11	V_{CC}
J12	GCB2/IO52PPB1
J13	GCA1/IO50PPB1
J14	GCC2/IO53PPB1
J15	NC
J16	GCA2/IO51PDB1

256-Pin FBGA	
Pin Number	A3P250L Function
K1	GFC2/IO105PDB3
K2	IO107NPB3
K3	IO104PPB3
K4	NC
K5	$V_{CCI}B3$
K6	V_{CC}
K7	GND
K8	GND
K9	GND
K10	GND
K11	V_{CC}
K12	$V_{CCI}B1$
K13	IO52NPB1
K14	IO55RSB1
K15	IO53NPB1
K16	IO51NDB1
L1	IO105NDB3
L2	IO104NPB3
L3	NC
L4	IO102RSB3
L5	$V_{CCI}B3$
L6	GND
L7	V_{CC}
L8	V_{CC}
L9	V_{CC}
L10	V_{CC}
L11	GND
L12	$V_{CCI}B1$
L13	GDB0/IO59VPB1
L14	IO57VDB1
L15	IO57UDB1
L16	IO56PDB1
M1	IO103PDB3
M2	NC
M3	IO101NPB3
M4	GEC0/IO100NPB3

256-Pin FBGA	
Pin Number	A3P250L Function
M5	VMV3
M6	$V_{CCI}B2$
M7	$V_{CCI}B2$
M8	NC
M9	IO74RSB2
M10	$V_{CCI}B2$
M11	$V_{CCI}B2$
M12	VMV2
M13	NC
M14	GDB1/IO59UPB1
M15	GDC1/IO58UDB1
M16	IO56NDB1
N1	IO103NDB3
N2	IO101PPB3
N3	GEC1/IO100PPB3
N4	NC
N5	GNDQ
N6	GEA2/IO97RSB2
N7	IO86RSB2
N8	IO82RSB2
N9	IO75RSB2
N10	IO69RSB2
N11	IO64RSB2
N12	GNDQ
N13	NC
N14	V_{JTAG}
N15	GDC0/IO58VDB1
N16	GDA1/IO60UDB1
P1	GEB1/IO99PDB3
P2	GEB0/IO99NDB3
P3	NC
P4	NC
P5	IO92RSB2
P6	IO89RSB2
P7	IO85RSB2
P8	IO81RSB2

256-Pin FBGA	
Pin Number	**A3P250L Function**
P9	IO76RSB2
P10	IO71RSB2
P11	IO66RSB2
P12	NC
P13	TCK
P14	V_{PUMP}
P15	TRST
P16	GDA0/IO60VDB1
R1	GEA1/IO98PDB3
R2	GEA0/IO98NDB3
R3	NC
R4	GEC2/IO95RSB2
R5	IO91RSB2
R6	IO88RSB2
R7	IO84RSB2
R8	IO80RSB2
R9	IO77RSB2
R10	IO72RSB2
R11	IO68RSB2
R12	IO65RSB2
R13	GDB2/IO62RSB2
R14	TDI
R15	NC
R16	TDO
T1	GND
T2	IO94RSB2
T3	FF/GEB2/IO96RSB2
T4	IO93RSB2
T5	IO90RSB2
T6	IO87RSB2
T7	IO83RSB2
T8	IO79RSB2
T9	IO78RSB2
T10	IO73RSB2
T11	IO70RSB2
T12	GDC2/IO63RSB2

256-Pin FBGA	
Pin Number	**A3P250L Function**
T13	IO67RSB2
T14	GDA2/IO61RSB2
T15	TMS
T16	GND

256-Pin FBGA	
Pin Number	A3P600L Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO11RSB0
A6	IO16RSB0
A7	IO18RSB0
A8	IO28RSB0
A9	IO34RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO43RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO173PDB3
B2	GAA2/IO174PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO13RSB0
B6	IO14RSB0
B7	IO21RSB0
B8	IO27RSB0
B9	IO32RSB0
B10	IO38RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO52RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO173NDB3
C2	IO174NDB3
C3	VMV3
C4	IO07RSB0

256-Pin FBGA	
Pin Number	A3P600L Function
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO20RSB0
C8	IO24RSB0
C9	IO33RSB0
C10	IO39RSB0
C11	IO44RSB0
C12	GBC0/IO54RSB0
C13	IO51RSB0
C14	VMV0
C15	IO61NPB1
C16	IO63PDB1
D1	IO171NDB3
D2	IO171PDB3
D3	GAC2/IO172PDB3
D4	IO06RSB0
D5	GNDQ
D6	IO10RSB0
D7	IO19RSB0
D8	IO26RSB0
D9	IO30RSB0
D10	IO40RSB0
D11	IO45RSB0
D12	GNDQ
D13	IO50RSB0
D14	GBB2/IO61PPB1
D15	IO53RSB0
D16	IO63NDB1
E1	IO166PDB3
E2	IO167NPB3
E3	IO172NDB3
E4	IO169NDB3
E5	VMV0
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	IO25RSB0

256-Pin FBGA	
Pin Number	A3P600L Function
E9	IO31RSB0
E10	V_{CCI}B0
E11	V_{CCI}B0
E12	VMV1
E13	GBC2/IO62PDB1
E14	IO67PPB1
E15	IO64PPB1
E16	IO66PDB1
F1	IO166NDB3
F2	IO168NPB3
F3	IO167PPB3
F4	IO169PDB3
F5	V_{CCI}B3
F6	GND
F7	V_{CC}
F8	V_{CC}
F9	V_{CC}
F10	V_{CC}
F11	GND
F12	V_{CCI}B1
F13	IO62NDB1
F14	IO64NPB1
F15	IO65PPB1
F16	IO66NDB1
G1	IO165NDB3
G2	IO165PDB3
G3	IO168PPB3
G4	GFC1/IO164PPB3
G5	V_{CCI}B3
G6	V_{CC}
G7	GND
G8	GND
G9	GND
G10	GND
G11	V_{CC}
G12	V_{CCI}B1

256-Pin FBGA	
Pin Number	A3P600L Function
G13	GCC1/IO69PPB1
G14	IO65NPB1
G15	IO75PDB1
G16	IO75NDB1
H1	GFB0/IO163NPB3
H2	GFA0/IO162NDB3
H3	GFB1/IO163PPB3
H4	V_{COMPLF}
H5	GFC0/IO164NPB3
H6	V_{CC}
H7	GND
H8	GND
H9	GND
H10	GND
H11	V_{CC}
H12	GCC0/IO69NPB1
H13	GCB1/IO70PPB1
H14	GCA0/IO71NPB1
H15	IO67NPB1
H16	GCB0/IO70NPB1
J1	GFA2/IO161PPB3
J2	GFA1/IO162PDB3
J3	VCCPLF
J4	IO160NDB3
J5	GFB2/IO160PDB3
J6	V_{CC}
J7	GND
J8	GND
J9	GND
J10	GND
J11	V_{CC}
J12	GCB2/IO73PPB1
J13	GCA1/IO71PPB1
J14	GCC2/IO74PPB1
J15	IO80PPB1
J16	GCA2/IO72PDB1

256-Pin FBGA	
Pin Number	A3P600L Function
K1	GFC2/IO159PDB3
K2	IO161NPB3
K3	IO156PPB3
K4	IO129RSB2
K5	V_{CCI}B3
K6	V_{CC}
K7	GND
K8	GND
K9	GND
K10	GND
K11	V_{CC}
K12	V_{CCI}B1
K13	IO73NPB1
K14	IO80NPB1
K15	IO74NPB1
K16	IO72NDB1
L1	IO159NDB3
L2	IO156NPB3
L3	IO151PPB3
L4	IO158PSB3
L5	V_{CCI}B3
L6	GND
L7	V_{CC}
L8	V_{CC}
L9	V_{CC}
L10	V_{CC}
L11	GND
L12	V_{CCI}B1
L13	GDB0/IO87NPB1
L14	IO85NDB1
L15	IO85PDB1
L16	IO84PDB1
M1	IO150PDB3
M2	IO151NPB3
M3	IO147NPB3
M4	GEC0/IO146NPB3

256-Pin FBGA	
Pin Number	A3P600L Function
M5	VMV3
M6	V_{CCI}B2
M7	V_{CCI}B2
M8	IO117RSB2
M9	IO110RSB2
M10	V_{CCI}B2
M11	V_{CCI}B2
M12	VMV2
M13	IO94RSB2
M14	GDB1/IO87PPB1
M15	GDC1/IO86PDB1
M16	IO84NDB1
N1	IO150NDB3
N2	IO147PPB3
N3	GEC1/IO146PPB3
N4	IO140RSB2
N5	GNDQ
N6	GEA2/IO143RSB2
N7	IO126RSB2
N8	IO120RSB2
N9	IO108RSB2
N10	IO103RSB2
N11	IO99RSB2
N12	GNDQ
N13	IO92RSB2
N14	V_{JTAG}
N15	GDC0/IO86NDB1
N16	GDA1/IO88PDB1
P1	GEB1/IO145PDB3
P2	GEB0/IO145NDB3
P3	VMV2
P4	IO138RSB2
P5	IO136RSB2
P6	IO131RSB2
P7	IO124RSB2
P8	IO119RSB2

256-Pin FBGA	
Pin Number	**A3P600L Function**
P9	IO107RSB2
P10	IO104RSB2
P11	IO97RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO88NDB1
R1	GEA1/IO144PDB3
R2	GEA0/IO144NDB3
R3	IO139RSB2
R4	GEC2/IO141RSB2
R5	IO132RSB2
R6	IO127RSB2
R7	IO121RSB2
R8	IO114RSB2
R9	IO109RSB2
R10	IO105RSB2
R11	IO98RSB2
R12	IO96RSB2
R13	GDB2/IO90RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO137RSB2
T3	FF/GEB2/IO142RSB2
T4	IO134RSB2
T5	IO125RSB2
T6	IO123RSB2
T7	IO118RSB2
T8	IO115RSB2
T9	IO111RSB2
T10	IO106RSB2
T11	IO102RSB2
T12	GDC2/IO91RSB2

256-Pin FBGA	
Pin Number	**A3P600L Function**
T13	IO93RSB2
T14	GDA2/IO89RSB2
T15	TMS
T16	GND

256-Pin FBGA	
Pin Number	A3P1000L Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO22RSB0
A7	IO28RSB0
A8	IO35RSB0
A9	IO45RSB0
A10	IO50RSB0
A11	IO55RSB0
A12	IO61RSB0
A13	GBB1/IO75RSB0
A14	GBA0/IO76RSB0
A15	GBA1/IO77RSB0
A16	GND
B1	GAB2/IO224PDB3
B2	GAA2/IO225PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO17RSB0
B6	IO21RSB0
B7	IO27RSB0
B8	IO34RSB0
B9	IO44RSB0
B10	IO51RSB0
B11	IO57RSB0
B12	GBC1/IO73RSB0
B13	GBB0/IO74RSB0
B14	IO71RSB0
B15	GBA2/IO78PDB1
B16	IO81PDB1
C1	IO224NDB3
C2	IO225NDB3
C3	VMV3
C4	IO11RSB0

256-Pin FBGA	
Pin Number	A3P1000L Function
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO25RSB0
C8	IO36RSB0
C9	IO42RSB0
C10	IO49RSB0
C11	IO56RSB0
C12	GBC0/IO72RSB0
C13	IO62RSB0
C14	VMV0
C15	IO78NDB1
C16	IO81NDB1
D1	IO222NDB3
D2	IO222PDB3
D3	GAC2/IO223PDB3
D4	IO223NDB3
D5	GNDQ
D6	IO23RSB0
D7	IO29RSB0
D8	IO33RSB0
D9	IO46RSB0
D10	IO52RSB0
D11	IO60RSB0
D12	GNDQ
D13	IO80NDB1
D14	GBB2/IO79PDB1
D15	IO79NDB1
D16	IO82NSB1
E1	IO217PDB3
E2	IO218PDB3
E3	IO221NDB3
E4	IO221PDB3
E5	VMV0
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	IO38RSB0

256-Pin FBGA	
Pin Number	A3P1000L Function
E9	IO47RSB0
E10	V_{CCI}B0
E11	V_{CCI}B0
E12	VMV1
E13	GBC2/IO80PDB1
E14	IO83PPB1
E15	IO86PPB1
E16	IO87PDB1
F1	IO217NDB3
F2	IO218NDB3
F3	IO216PDB3
F4	IO216NDB3
F5	V_{CCI}B3
F6	GND
F7	V_{CC}
F8	V_{CC}
F9	V_{CC}
F10	V_{CC}
F11	GND
F12	V_{CCI}B1
F13	IO83NPB1
F14	IO86NPB1
F15	IO90PPB1
F16	IO87NDB1
G1	IO210PSB3
G2	IO213NDB3
G3	IO213PDB3
G4	GFC1/IO209PPB3
G5	V_{CCI}B3
G6	V_{CC}
G7	GND
G8	GND
G9	GND
G10	GND
G11	V_{CC}
G12	V_{CCI}B1

256-Pin FBGA	
Pin Number	A3P1000L Function
G13	GCC1/IO91PPB1
G14	IO90NPB1
G15	IO88PDB1
G16	IO88NDB1
H1	GFB0/IO208NPB3
H2	GFA0/IO207NDB3
H3	GFB1/IO208PPB3
H4	V_{COMPLF}
H5	GFC0/IO209NPB3
H6	V_{CC}
H7	GND
H8	GND
H9	GND
H10	GND
H11	V_{CC}
H12	GCC0/IO91NPB1
H13	GCB1/IO92PPB1
H14	GCA0/IO93NPB1
H15	IO96NPB1
H16	GCB0/IO92NPB1
J1	GFA2/IO206PSB3
J2	GFA1/IO207PDB3
J3	V_{CCPLF}
J4	IO205NDB3
J5	GFB2/IO205PDB3
J6	V_{CC}
J7	GND
J8	GND
J9	GND
J10	GND
J11	V_{CC}
J12	GCB2/IO95PPB1
J13	GCA1/IO93PPB1
J14	GCC2/IO96PPB1
J15	IO100PPB1
J16	GCA2/IO94PSB1

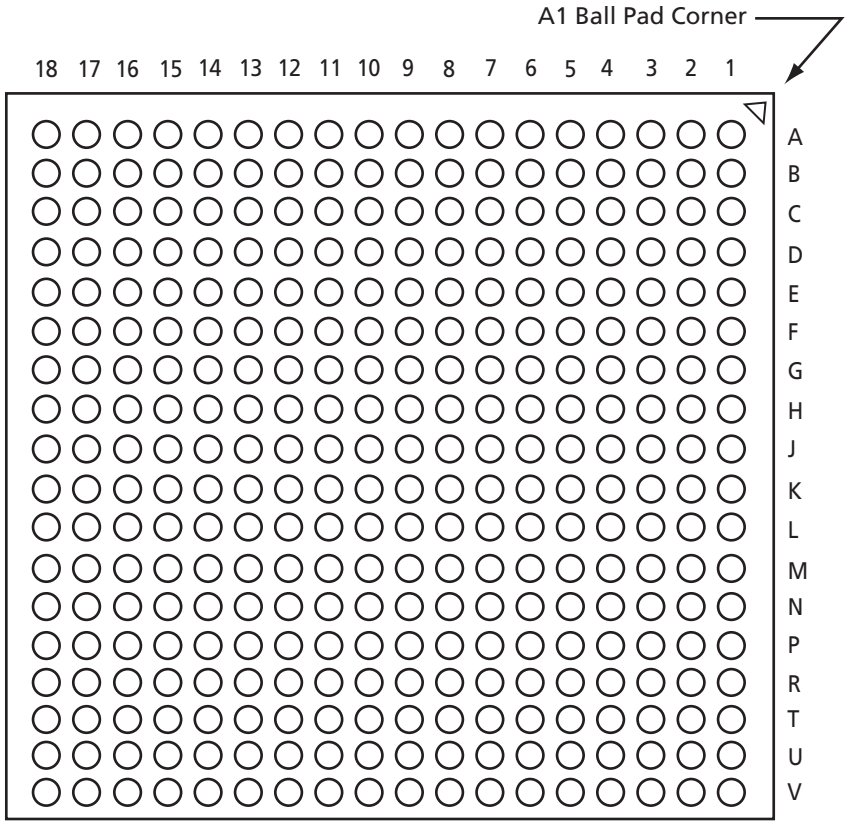
256-Pin FBGA	
Pin Number	A3P1000L Function
K1	GFC2/IO204PDB3
K2	IO204NDB3
K3	IO203NDB3
K4	IO203PDB3
K5	V_{CCI}B3
K6	V_{CC}
K7	GND
K8	GND
K9	GND
K10	GND
K11	V_{CC}
K12	V_{CCI}B1
K13	IO95NPB1
K14	IO100NPB1
K15	IO102NDB1
K16	IO102PDB1
L1	IO202NDB3
L2	IO202PDB3
L3	IO196PPB3
L4	IO193PPB3
L5	V_{CCI}B3
L6	GND
L7	V_{CC}
L8	V_{CC}
L9	V_{CC}
L10	V_{CC}
L11	GND
L12	V_{CCI}B1
L13	GDB0/IO112NPB1
L14	IO106NDB1
L15	IO106PDB1
L16	IO107PDB1
M1	IO197NSB3
M2	IO196NPB3
M3	IO193NPB3
M4	GEC0/IO190NPB3

256-Pin FBGA	
Pin Number	A3P1000L Function
M5	VMV3
M6	V_{CCI}B2
M7	V_{CCI}B2
M8	IO147RSB2
M9	IO136RSB2
M10	V_{CCI}B2
M11	V_{CCI}B2
M12	VMV2
M13	IO110NDB1
M14	GDB1/IO112PPB1
M15	GDC1/IO111PDB1
M16	IO107NDB1
N1	IO194PSB3
N2	IO192PPB3
N3	GEC1/IO190PPB3
N4	IO192NPB3
N5	GNDQ
N6	GEA2/IO187RSB2
N7	IO161RSB2
N8	IO155RSB2
N9	IO141RSB2
N10	IO129RSB2
N11	IO124RSB2
N12	GNDQ
N13	IO110PDB1
N14	V_{JTAG}
N15	GDC0/IO111NDB1
N16	GDA1/IO113PDB1
P1	GEB1/IO189PDB3
P2	GEB0/IO189NDB3
P3	VMV2
P4	IO179RSB2
P5	IO171RSB2
P6	IO165RSB2
P7	IO159RSB2
P8	IO151RSB2

256-Pin FBGA	
Pin Number	**A3P1000L Function**
P9	IO137RSB2
P10	IO134RSB2
P11	IO128RSB2
P12	VMV1
P13	TCK
P14	V_{PUMP}
P15	TRST
P16	GDA0/IO113NDB1
R1	GEA1/IO188PDB3
R2	GEA0/IO188NDB3
R3	IO184RSB2
R4	GEC2/IO185RSB2
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	FF/GEB2/IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2

256-Pin FBGA	
Pin Number	**A3P1000L Function**
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

324-Pin FBGA



Note: This is the bottom view of the package.

Figure 3-5 •

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

324-Pin FBGA	
Pin Number	A3PE3000L Function
A1	GND
A2	IO08NDB0V0
A3	IO08PDB0V0
A4	IO10NDB0V1
A5	IO10PDB0V1
A6	IO12PDB0V1
A7	GND
A8	IO32NDB0V3
A9	IO32PDB0V3
A10	IO42PPB1V0
A11	IO52NPB1V1
A12	GND
A13	IO66NDB1V3
A14	IO72NDB1V3
A15	IO72PDB1V3
A16	IO74NDB1V4
A17	IO74PDB1V4
A18	GND
B1	IO305PDB7V3
B2	GAB2/IO308PDB7V4
B3	GAA0/IO00NPB0V0
B4	V_{CCI}B0
B5	GNDQ
B6	IO12NDB0V1
B7	IO18NDB0V2
B8	V_{CCI}B0
B9	IO42NPB1V0
B10	IO44NDB1V0
B11	V_{CCI}B1
B12	IO52PPB1V1
B13	IO66PDB1V3
B14	GNDQ
B15	V_{CCI}B1
B16	GBA0/IO81NDB1V4
B17	GBA1/IO81PDB1V4
B18	IO88PDB2V0

324-Pin FBGA	
Pin Number	A3PE3000L Function
C1	IO305NDB7V3
C2	IO308NDB7V4
C3	GAA2/IO309PPB7V4
C4	GAA1/IO00PPB0V0
C5	VMV0
C6	IO14NDB0V1
C7	IO18PDB0V2
C8	IO40NDB0V4
C9	IO40PDB0V4
C10	IO44PDB1V0
C11	IO56NDB1V1
C12	IO64NDB1V2
C13	IO64PDB1V2
C14	VMV1
C15	GBC0/IO79NDB1V4
C16	GBC1/IO79PDB1V4
C17	GBB2/IO83PPB2V0
C18	IO88NDB2V0
D1	IO303PDB7V3
D2	V_{CCI}B7
D3	GAC2/IO307PPB7V4
D4	IO309NPB7V4
D5	GAB1/IO01PPB0V0
D6	IO14PDB0V1
D7	IO24NDB0V2
D8	IO24PDB0V2
D9	IO28PDB0V3
D10	IO48NDB1V0
D11	IO56PDB1V1
D12	IO60PPB1V2
D13	GBB0/IO80NDB1V4
D14	GBB1/IO80PDB1V4
D15	GBA2/IO82PDB2V0
D16	IO83NPB2V0
D17	V_{CCI}B2
D18	IO90PDB2V1

324-Pin FBGA	
Pin Number	A3PE3000L Function
E1	IO303NDB7V3
E2	GNDQ
E2	GNDQ
E3	VMV7
E3	VMV7
E4	IO307NPB7V4
E5	V_{CCPLA}
E6	GAB0/IO01NPB0V0
E7	V_{CCI}B0
E8	GND
E9	IO28NDB0V3
E10	IO48PDB1V0
E11	GND
E12	V_{CCI}B1
E13	IO60NPB1V2
E14	V_{CCPLB}
E15	IO82NDB2V0
E16	VMV2
E16	VMV2
E17	GNDQ
E17	GNDQ
E18	IO90NDB2V1
F1	IO299NDB7V3
F2	IO299PDB7V3
F3	IO295PDB7V2
F4	IO295NDB7V2
F5	V_{COMPLA}
F6	IO291PPB7V2
F7	GAC0/IO02NDB0V0
F8	GAC1/IO02PDB0V0
F9	IO26PDB0V3
F10	IO34PDB0V4
F11	IO58NDB1V2
F12	IO58PDB1V2
F13	IO94PPB2V1
F14	V_{COMPLB}

324-Pin FBGA	
Pin Number	A3PE3000L Function
F15	GBC2/IO84PDB2V0
F16	IO84NDB2V0
F17	IO92NDB2V1
F18	IO92PDB2V1
G1	GND
G2	IO287PDB7V1
G3	IO287NDB7V1
G4	IO283PPB7V1
G5	V_{CCI}B7
G6	IO279PDB7V0
G7	IO291NPB7V2
G8	V_{CC}
G9	IO26NDB0V3
G10	IO34NDB0V4
G11	V_{CC}
G12	IO94NPB2V1
G13	IO98PDB2V2
G14	V_{CCI}B2
G15	GCC0/IO112NPB2V3
G16	IO104PDB2V2
G17	IO104NDB2V2
G18	GND
H1	IO267PDB6V4
H2	V_{CCI}B7
H3	IO283NPB7V1
H4	GFB1/IO274PPB7V0
H5	GND
H6	IO279NDB7V0
H7	V_{CC}
H8	V_{CC}
H9	GND
H10	GND
H11	V_{CC}
H12	V_{CC}
H13	IO98NDB2V2
H14	GND

324-Pin FBGA	
Pin Number	A3PE3000L Function
H15	GCB1/IO113PDB2V3
H16	GCC1/IO112PPB2V3
H17	V_{CCI}B2
H18	IO108PDB2V3
J1	IO267NDB6V4
J2	GFA0/IO273NDB6V4
J3	V_{COMPLF}
J4	GFA2/IO272PDB6V4
J5	GFB0/IO274NPB7V0
J6	GFC0/IO275NDB7V0
J7	GFC1/IO275PDB7V0
J8	GND
J9	GND
J10	GND
J11	GND
J12	GCA2/IO115PDB3V0
J13	GCA1/IO114PDB3V0
J14	GCA0/IO114NDB3V0
J15	GCB0/IO113NDB2V3
J16	V_{COMPLC}
J17	IO120NPB3V0
J18	IO108NDB2V3
K1	IO263PDB6V3
K2	GFA1/IO273PDB6V4
K3	V_{CCPLF}
K4	IO272NDB6V4
K5	GFC2/IO270PPB6V4
K6	GFB2/IO271PDB6V4
K7	IO271NDB6V4
K8	GND
K9	GND
K10	GND
K11	GND
K12	IO115NDB3V0
K13	GCB2/IO116PDB3V0
K14	IO116NDB3V0

324-Pin FBGA	
Pin Number	A3PE3000L Function
K15	GCC2/IO117PDB3V0
K16	V_{CCPLC}
K17	IO124NPB3V1
K18	IO120PPB3V0
L1	IO263NDB6V3
L2	V_{CCI}B6
L3	IO259PDB6V3
L4	IO259NDB6V3
L5	GND
L6	IO270NPB6V4
L7	V_{CC}
L8	V_{CC}
L9	GND
L10	GND
L11	V_{CC}
L12	V_{CC}
L13	IO132PDB3V2
L14	GND
L15	IO117NDB3V0
L16	IO128NPB3V1
L17	V_{CCI}B3
L18	IO124PPB3V1
M1	GND
M2	IO255PDB6V2
M3	IO255NDB6V2
M4	IO251PPB6V2
M5	V_{CCI}B6
M6	GEB0/IO235NDB6V0
M7	GEB1/IO235PDB6V0
M8	V_{CC}
M9	IO192PPB4V4
M10	IO154NPB4V0
M11	V_{CC}
M12	GDA0/IO153NPB3V4
M13	IO132NDB3V2
M14	V_{CCI}B3

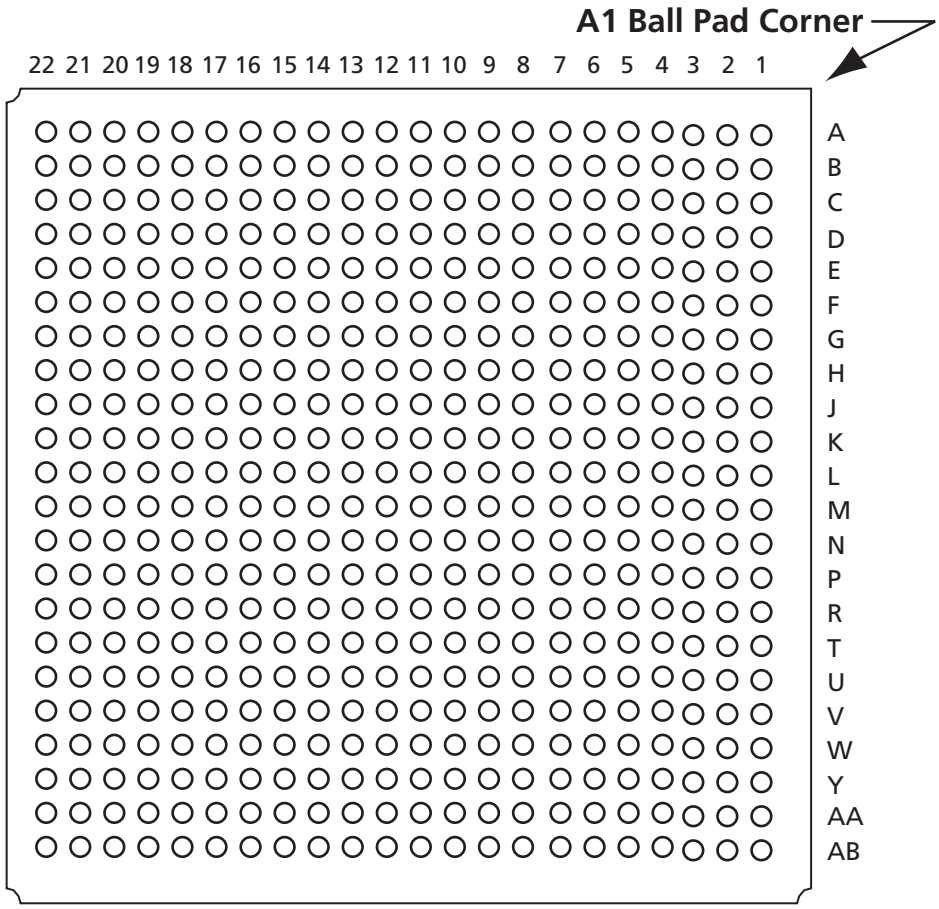
324-Pin FBGA	
Pin Number	A3PE3000L Function
M15	IO134NDB3V2
M16	IO134PDB3V2
M17	IO128PPB3V1
M18	GND
N1	IO247NDB6V1
N2	IO247PDB6V1
N3	IO251NPB6V2
N4	GEC0/IO236NDB6V0
N5	V_{COMPLE}
N6	IO212NDB5V2
N7	IO212PDB5V2
N8	IO192NPB4V4
N9	IO174PDB4V2
N10	IO170PDB4V2
N11	GDA2/IO154PPB4V0
N12	GDB2/IO155PPB4V0
N13	GDA1/IO153PPB3V4
N14	V_{COMPLD}
N15	GDB0/IO152NDB3V4
N16	GDB1/IO152PDB3V4
N17	IO138NDB3V3
N18	IO138PDB3V3
P1	IO245PDB6V1
P2	GNDQ
P2	GNDQ
P3	VMV6
P3	VMV6
P4	GEC1/IO236PDB6V0
P5	V_{CCPLE}
P6	IO214PDB5V2
P7	V_{CCI}B5
P8	GND
P9	IO174NDB4V2
P10	IO170NDB4V2
P11	GND
P12	V_{CCI}B4

324-Pin FBGA	
Pin Number	A3PE3000L Function
P13	IO155NPB4V0
P14	V_{CCPLD}
P15	V_{JTAG}
P16	GDC0/IO151NDB3V4
P17	GDC1/IO151PDB3V4
P18	IO142PDB3V3
R1	IO245NDB6V1
R2	V_{CCI}B6
R3	GEA1/IO234PPB6V0
R4	IO232NDB5V4
R5	FF/GEB2/IO232PDB5V4
R6	IO214NDB5V2
R7	IO202PDB5V1
R8	IO194PDB5V0
R9	IO186PDB4V4
R10	IO178PDB4V3
R11	IO168NSB4V1
R12	IO164PDB4V1
R13	GDC2/IO156PDB4V0
R14	TCK
R15	V_{PUMP}
R16	TRST
R17	V_{CCI}B3
R18	IO142NDB3V3
T1	IO241PDB6V0
T2	GEA0/IO234NPB6V0
T3	IO233NPB5V4
T4	IO231NPB5V4
T5	VMV5
T6	IO208NDB5V1
T7	IO202NDB5V1
T8	IO194NDB5V0
T9	IO186NDB4V4
T10	IO178NDB4V3
T11	IO166NPB4V1

324-Pin FBGA	
Pin Number	A3PE3000L Function
T12	IO164NDB4V1
T13	IO156NDB4V0
T14	VMV4
T15	TDI
T16	GNDQ
T16	GNDQ
T17	TDO
T18	IO146PDB3V4
U1	IO241NDB6V0
U2	GEA2/IO233PPB5V4
U3	GEC2/IO231PPB5V4
U4	V_{CCI}B5
U5	GNDQ
U6	IO208PDB5V1
U7	IO198PPB5V0
U8	V_{CCI}B5
U9	IO182NPB4V3
U10	IO180NPB4V3
U11	V_{CCI}B4
U12	IO166PPB4V1
U13	IO162PDB4V1
U14	GNDQ
U15	V_{CCI}B4
U16	TMS
U17	VMV3
U17	VMV3
U18	IO146NDB3V4
V1	GND
V2	IO218NDB5V3
V3	IO218PDB5V3
V4	IO206NDB5V1
V5	IO206PDB5V1
V6	IO198NPB5V0
V7	GND
V8	IO190NDB4V4
V9	IO190PDB4V4

324-Pin FBGA	
Pin Number	**A3PE3000L Function**
V10	IO182PPB4V3
V11	IO180PPB4V3
V12	GND
V13	IO162NDB4V1
V14	IO160NDB4V0
V15	IO160PDB4V0
V16	IO158NDB4V0
V17	IO158PDB4V0
V18	GND

484-Pin FBGA



Note: This is the bottom view of the package.

Figure 3-6 •

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

484-Pin FBGA	
Pin Number	A3P600L Function
A1	GND
A2	GND
A3	V_{CCI}B0
A4	NC
A5	NC
A6	IO09RSB0
A7	IO15RSB0
A8	NC
A9	NC
A10	IO22RSB0
A11	IO23RSB0
A12	IO29RSB0
A13	IO35RSB0
A14	NC
A15	NC
A16	IO46RSB0
A17	IO48RSB0
A18	NC
A19	NC
A20	V_{CCI}B0
A21	GND
A22	GND
AA1	GND
AA2	V_{CCI}B3
AA3	NC
AA4	NC
AA5	NC
AA6	IO135RSB2
AA7	IO133RSB2
AA8	NC
AA9	NC
AA10	NC
AA11	NC
AA12	NC
AA13	NC
AA14	NC

484-Pin FBGA	
Pin Number	A3P600L Function
AA15	NC
AA16	IO101RSB2
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	V_{CCI}B1
AA22	GND
AB1	GND
AB2	GND
AB3	V_{CCI}B2
AB4	NC
AB5	NC
AB6	IO130RSB2
AB7	IO128RSB2
AB8	IO122RSB2
AB9	IO116RSB2
AB10	NC
AB11	NC
AB12	IO113RSB2
AB13	IO112RSB2
AB14	NC
AB15	NC
AB16	IO100RSB2
AB17	IO95RSB2
AB18	NC
AB19	NC
AB20	V_{CCI}B2
AB21	GND
AB22	GND
B1	GND
B2	V_{CCI}B3
B3	NC
B4	NC
B5	NC
B6	IO08RSB0

484-Pin FBGA	
Pin Number	A3P600L Function
B7	IO12RSB0
B8	NC
B9	NC
B10	IO17RSB0
B11	NC
B12	NC
B13	IO36RSB0
B14	NC
B15	NC
B16	IO47RSB0
B17	IO49RSB0
B18	NC
B19	NC
B20	NC
B21	V_{CCI}B1
B22	GND
C1	V_{CCI}B3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	V_{CC}
C9	V_{CC}
C10	NC
C11	NC
C12	NC
C13	NC
C14	V_{CC}
C15	V_{CC}
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

484-Pin FBGA	
Pin Number	A3P600L Function
C21	NC
C22	V_{CCI}B1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO11RSB0
D9	IO16RSB0
D10	IO18RSB0
D11	IO28RSB0
D12	IO34RSB0
D13	IO37RSB0
D14	IO41RSB0
D15	IO43RSB0
D16	GBB1/IO57RSB0
D17	GBA0/IO58RSB0
D18	GBA1/IO59RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO173PDB3
E5	GAA2/IO174PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO13RSB0
E9	IO14RSB0
E10	IO21RSB0
E11	IO27RSB0
E12	IO32RSB0

484-Pin FBGA	
Pin Number	A3P600L Function
E13	IO38RSB0
E14	IO42RSB0
E15	GBC1/IO55RSB0
E16	GBB0/IO56RSB0
E17	IO52RSB0
E18	GBA2/IO60PDB1
E19	IO60NDB1
E20	GND
E21	NC
E22	NC
F1	NC
F2	NC
F3	NC
F4	IO173NDB3
F5	IO174NDB3
F6	VMV3
F7	IO07RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO20RSB0
F11	IO24RSB0
F12	IO33RSB0
F13	IO39RSB0
F14	IO44RSB0
F15	GBC0/IO54RSB0
F16	IO51RSB0
F17	VMV0
F18	IO61NPB1
F19	IO63PDB1
F20	NC
F21	NC
F22	NC
G1	IO170NDB3
G2	IO170PDB3
G3	NC
G4	IO171NDB3

484-Pin FBGA	
Pin Number	A3P600L Function
G5	IO171PDB3
G6	GAC2/IO172PDB3
G7	IO06RSB0
G8	GNDQ
G9	IO10RSB0
G10	IO19RSB0
G11	IO26RSB0
G12	IO30RSB0
G13	IO40RSB0
G14	IO45RSB0
G15	GNDQ
G16	IO50RSB0
G17	GBB2/IO61PPB1
G18	IO53RSB0
G19	IO63NDB1
G20	NC
G21	NC
G22	NC
H1	NC
H2	NC
H3	V_{CC}
H4	IO166PDB3
H5	IO167NPB3
H6	IO172NDB3
H7	IO169NDB3
H8	VMV0
H9	V_{CCI}B0
H10	V_{CCI}B0
H11	IO25RSB0
H12	IO31RSB0
H13	V_{CCI}B0
H14	V_{CCI}B0
H15	VMV1
H16	GBC2/IO62PDB1
H17	IO67PPB1
H18	IO64PPB1

484-Pin FBGA	
Pin Number	A3P600L Function
H19	IO66PDB1
H20	V_{CC}
H21	NC
H22	NC
J1	NC
J2	NC
J3	NC
J4	IO166NDB3
J5	IO168NPB3
J6	IO167PPB3
J7	IO169PDB3
J8	V_{CCI}B3
J9	GND
J10	V_{CC}
J11	V_{CC}
J12	V_{CC}
J13	V_{CC}
J14	GND
J15	V_{CCI}B1
J16	IO62NDB1
J17	IO64NPB1
J18	IO65PPB1
J19	IO66NDB1
J20	NC
J21	IO68PDB1
J22	IO68NDB1
K1	IO157PDB3
K2	IO157NDB3
K3	NC
K4	IO165NDB3
K5	IO165PDB3
K6	IO168PPB3
K7	GFC1/IO164PPB3
K8	V_{CCI}B3
K9	V_{CC}
K10	GND

484-Pin FBGA	
Pin Number	A3P600L Function
K11	GND
K12	GND
K13	GND
K14	V_{CC}
K15	VvB1
K16	GCC1/IO69PPB1
K17	IO65NPB1
K18	IO75PDB1
K19	IO75NDB1
K20	NC
K21	IO76NDB1
K22	IO76PDB1
L1	NC
L2	IO155PDB3
L3	NC
L4	GFB0/IO163NPB3
L5	GFA0/IO162NDB3
L6	GFB1/IO163PPB3
L7	V_{COMPLF}
L8	GFC0/IO164NPB3
L9	V_{CC}
L10	GND
L11	GND
L12	GND
L13	GND
L14	V_{CC}
L15	GCC0/IO69NPB1
L16	GCB1/IO70PPB1
L17	GCA0/IO71NPB1
L18	IO67NPB1
L19	GCB0/IO70NPB1
L20	IO77PDB1
L21	IO77NDB1
L22	IO78NPB1
M1	NC
M2	IO155NDB3

484-Pin FBGA	
Pin Number	A3P600L Function
M3	IO158NPB3
M4	GFA2/IO161PPB3
M5	GFA1/IO162PDB3
M6	V_{CCPLF}
M7	IO160NDB3
M8	GFB2/IO160PDB3
M9	V_{CC}
M10	GND
M11	GND
M12	GND
M13	GND
M14	V_{CC}
M15	GCB2/IO73PPB1
M16	GCA1/IO71PPB1
M17	GCC2/IO74PPB1
M18	IO80PPB1
M19	GCA2/IO72PDB1
M20	IO79PPB1
M21	IO78PPB1
M22	NC
N1	IO154NDB3
N2	IO154PDB3
N3	NC
N4	GFC2/IO159PDB3
N5	IO161NPB3
N6	IO156PPB3
N7	IO129RSB2
N8	V_{CCI}B3
N9	V_{CC}
N10	GND
N11	GND
N12	GND
N13	GND
N14	V_{CC}
N15	V_{CCI}B1
N16	IO73NPB1

484-Pin FBGA	
Pin Number	A3P600L Function
N17	IO80NPB1
N18	IO74NPB1
N19	IO72NDB1
N20	NC
N21	IO79NPB1
N22	NC
P1	NC
P2	IO153PDB3
P3	IO153NDB3
P4	IO159NDB3
P5	IO156NPB3
P6	IO151PPB3
P7	IO158PPB3
P8	V_{CCI}B3
P9	GND
P10	V_{CC}
P11	V_{CC}
P12	V_{CC}
P13	V_{CC}
P14	GND
P15	V_{CCI}B1
P16	GDB0/IO87NPB1
P17	IO85NDB1
P18	IO85PDB1
P19	IO84PDB1
P20	NC
P21	IO81PDB1
P22	NC
R1	NC
R2	NC
R3	V_{CC}
R4	IO150PDB3
R5	IO151NPB3
R6	IO147NPB3
R7	GEC0/IO146NPB3
R8	VMV3

484-Pin FBGA	
Pin Number	A3P600L Function
R9	V_{CCI}B2
R10	V_{CCI}B2
R11	IO117RSB2
R12	IO110RSB2
R13	V_{CCI}B2
R14	V_{CCI}B2
R15	VMV2
R16	IO94RSB2
R17	GDB1/IO87PPB1
R18	GDC1/IO86PDB1
R19	IO84NDB1
R20	V_{CC}
R21	IO81NDB1
R22	IO82PDB1
T1	IO152PDB3
T2	IO152NDB3
T3	NC
T4	IO150NDB3
T5	IO147PPB3
T6	GEC1/IO146PPB3
T7	IO140RSB2
T8	GNDQ
T9	GEA2/IO143RSB2
T10	IO126RSB2
T11	IO120RSB2
T12	IO108RSB2
T13	IO103RSB2
T14	IO99RSB2
T15	GNDQ
T16	IO92RSB2
T17	V_{JTAG}
T18	GDC0/IO86NDB1
T19	GDA1/IO88PDB1
T20	NC
T21	IO83PDB1
T22	IO82NDB1

484-Pin FBGA	
Pin Number	A3P600L Function
U1	IO149PDB3
U2	IO149NDB3
U3	NC
U4	GEB1/IO145PDB3
U5	GEB0/IO145NDB3
U6	VMV2
U7	IO138RSB2
U8	IO136RSB2
U9	IO131RSB2
U10	IO124RSB2
U11	IO119RSB2
U12	IO107RSB2
U13	IO104RSB2
U14	IO97RSB2
U15	VMV1
U16	TCK
U17	V_{PUMP}
U18	TRST
U19	GDA0/IO88NDB1
U20	NC
U21	IO83NDB1
U22	NC
V1	NC
V2	NC
V3	GND
V4	GEA1/IO144PDB3
V5	GEA0/IO144NDB3
V6	IO139RSB2
V7	GEC2/IO141RSB2
V8	IO132RSB2
V9	IO127RSB2
V10	IO121RSB2
V11	IO114RSB2
V12	IO109RSB2
V13	IO105RSB2
V14	IO98RSB2

484-Pin FBGA	
Pin Number	**A3P600L Function**
V15	IO96RSB2
V16	GDB2/IO90RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	NC
W1	NC
W2	IO148PDB3
W3	NC
W4	GND
W5	IO137RSB2
W6	FF/GEB2/IO142RSB2
W7	IO134RSB2
W8	IO125RSB2
W9	IO123RSB2
W10	IO118RSB2
W11	IO115RSB2
W12	IO111RSB2
W13	IO106RSB2
W14	IO102RSB2
W15	GDC2/IO91RSB2
W16	IO93RSB2
W17	GDA2/IO89RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	V_{CCI}B3
Y2	IO148NDB3
Y3	NC
Y4	NC
Y5	GND
Y6	NC

484-Pin FBGA	
Pin Number	**A3P600L Function**
Y7	NC
Y8	V_{CC}
Y9	V_{CC}
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	V_{CC}
Y15	V_{CC}
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	V_{CCI}B1

484-Pin FBGA	
Pin Number	A3P1000L Function
A1	GND
A2	GND
A3	V_{CCI}B0
A4	IO07RSB0
A5	IO09RSB0
A6	IO13RSB0
A7	IO18RSB0
A8	IO20RSB0
A9	IO26RSB0
A10	IO32RSB0
A11	IO40RSB0
A12	IO41RSB0
A13	IO53RSB0
A14	IO59RSB0
A15	IO64RSB0
A16	IO65RSB0
A17	IO67RSB0
A18	IO69RSB0
A19	NC
A20	V_{CCI}B0
A21	GND
A22	GND
AA1	GND
AA2	V_{CCI}B3
AA3	NC
AA4	IO181RSB2
AA5	IO178RSB2
AA6	IO175RSB2
AA7	IO169RSB2
AA8	IO166RSB2
AA9	IO160RSB2
AA10	IO152RSB2
AA11	IO146RSB2
AA12	IO139RSB2
AA13	IO133RSB2
AA14	NC

484-Pin FBGA	
Pin Number	A3P1000L Function
AA15	NC
AA16	IO122RSB2
AA17	IO119RSB2
AA18	IO117RSB2
AA19	NC
AA20	NC
AA21	V_{CCI}B1
AA22	GND
AB1	GND
AB2	GND
AB3	V_{CCI}B2
AB4	IO180RSB2
AB5	IO176RSB2
AB6	IO173RSB2
AB7	IO167RSB2
AB8	IO162RSB2
AB9	IO156RSB2
AB10	IO150RSB2
AB11	IO145RSB2
AB12	IO144RSB2
AB13	IO132RSB2
AB14	IO127RSB2
AB15	IO126RSB2
AB16	IO123RSB2
AB17	IO121RSB2
AB18	IO118RSB2
AB19	NC
AB20	V_{CCI}B2
AB21	GND
AB22	GND
B1	GND
B2	V_{CCI}B3
B3	NC
B4	IO06RSB0
B5	IO08RSB0
B6	IO12RSB0

484-Pin FBGA	
Pin Number	A3P1000L Function
B7	IO15RSB0
B8	IO19RSB0
B9	IO24RSB0
B10	IO31RSB0
B11	IO39RSB0
B12	IO48RSB0
B13	IO54RSB0
B14	IO58RSB0
B15	IO63RSB0
B16	IO66RSB0
B17	IO68RSB0
B18	IO70RSB0
B19	NC
B20	NC
B21	V_{CCI}B1
B22	GND
C1	V_{CCI}B3
C2	IO220PDB3
C3	NC
C4	NC
C5	GND
C6	IO10RSB0
C7	IO14RSB0
C8	V_{CC}
C9	V_{CC}
C10	IO30RSB0
C11	IO37RSB0
C12	IO43RSB0
C13	NC
C14	V_{CC}
C15	V_{CC}
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

484-Pin FBGA	
Pin Number	A3P1000L Function
C21	NC
C22	V_{CCI}B1
D1	IO219PDB3
D2	IO220NDB3
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO16RSB0
D9	IO22RSB0
D10	IO28RSB0
D11	IO35RSB0
D12	IO45RSB0
D13	IO50RSB0
D14	IO55RSB0
D15	IO61RSB0
D16	GBB1/IO75RSB0
D17	GBA0/IO76RSB0
D18	GBA1/IO77RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	IO219NDB3
E2	NC
E3	GND
E4	GAB2/IO224PDB3
E5	GAA2/IO225PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO17RSB0
E9	IO21RSB0
E10	IO27RSB0
E11	IO34RSB0
E12	IO44RSB0

484-Pin FBGA	
Pin Number	A3P1000L Function
E13	IO51RSB0
E14	IO57RSB0
E15	GBC1/IO73RSB0
E16	GBB0/IO74RSB0
E17	IO71RSB0
E18	GBA2/IO78PDB1
E19	IO81PDB1
E20	GND
E21	NC
E22	IO84PDB1
F1	NC
F2	IO215PDB3
F3	IO215NDB3
F4	IO224NDB3
F5	IO225NDB3
F6	VMV3
F7	IO11RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO25RSB0
F11	IO36RSB0
F12	IO42RSB0
F13	IO49RSB0
F14	IO56RSB0
F15	GBC0/IO72RSB0
F16	IO62RSB0
F17	VMV0
F18	IO78NDB1
F19	IO81NDB1
F20	IO82PPB1
F21	NC
F22	IO84NDB1
G1	IO214NDB3
G2	IO214PDB3
G3	NC
G4	IO222NDB3

484-Pin FBGA	
Pin Number	A3P1000L Function
G5	IO222PDB3
G6	GAC2/IO223PDB3
G7	IO223NDB3
G8	GNDQ
G9	IO23RSB0
G10	IO29RSB0
G11	IO33RSB0
G12	IO46RSB0
G13	IO52RSB0
G14	IO60RSB0
G15	GNDQ
G16	IO80NDB1
G17	GBB2/IO79PDB1
G18	IO79NDB1
G19	IO82NPB1
G20	IO85PDB1
G21	IO85NDB1
G22	NC
H1	NC
H2	NC
H3	V_{CC}
H4	IO217PDB3
H5	IO218PDB3
H6	IO221NDB3
H7	IO221PDB3
H8	VMV0
H9	V_{CCI}B0
H10	V_{CCI}B0
H11	IO38RSB0
H12	IO47RSB0
H13	V_{CCI}B0
H14	V_{CCI}B0
H15	VMV1
H16	GBC2/IO80PDB1
H17	IO83PPB1
H18	IO86PPB1

484-Pin FBGA	
Pin Number	A3P1000L Function
H19	IO87PDB1
H20	V_{CC}
H21	NC
H22	NC
J1	IO212NDB3
J2	IO212PDB3
J3	NC
J4	IO217NDB3
J5	IO218NDB3
J6	IO216PDB3
J7	IO216NDB3
J8	V_{CCI}B3
J9	GND
J10	V_{CC}
J11	V_{CC}
J12	V_{CC}
J13	V_{CC}
J14	GND
J15	V_{CCI}B1
J16	IO83NPB1
J17	IO86NPB1
J18	IO90PPB1
J19	IO87NDB1
J20	NC
J21	IO89PDB1
J22	IO89NDB1
K1	IO211PDB3
K2	IO211NDB3
K3	NC
K4	IO210PPB3
K5	IO213NDB3
K6	IO213PDB3
K7	GFC1/IO209PPB3
K8	V_{CCI}B3
K9	V_{CC}
K10	GND

484-Pin FBGA	
Pin Number	A3P1000L Function
K11	GND
K12	GND
K13	GND
K14	V_{CC}
K15	V_{CCI}B1
K16	GCC1/IO91PPB1
K17	IO90NPB1
K18	IO88PDB1
K19	IO88NDB1
K20	IO94NPB1
K21	IO98NDB1
K22	IO98PDB1
L1	NC
L2	IO200PDB3
L3	IO210NPB3
L4	GFB0/IO208NPB3
L5	GFA0/IO207NDB3
L6	GFB1/IO208PPB3
L7	V_{COMPLF}
L8	GFC0/IO209NPB3
L9	V_{CC}
L10	GND
L11	GND
L12	GND
L13	GND
L14	V_{CC}
L15	GCC0/IO91NPB1
L16	GCB1/IO92PPB1
L17	GCA0/IO93NPB1
L18	IO96NPB1
L19	GCB0/IO92NPB1
L20	IO97PDB1
L21	IO97NDB1
L22	IO99NPB1
M1	NC
M2	IO200NDB3

484-Pin FBGA	
Pin Number	A3P1000L Function
M3	IO206NDB3
M4	GFA2/IO206PDB3
M5	GFA1/IO207PDB3
M6	V_{CCPLF}
M7	IO205NDB3
M8	GFB2/IO205PDB3
M9	V_{CC}
M10	GND
M11	GND
M12	GND
M13	GND
M14	V_{CC}
M15	GCB2/IO95PPB1
M16	GCA1/IO93PPB1
M17	GCC2/IO96PPB1
M18	IO100PPB1
M19	GCA2/IO94PPB1
M20	IO101PPB1
M21	IO99PPB1
M22	NC
N1	IO201NDB3
N2	IO201PDB3
N3	NC
N4	GFC2/IO204PDB3
N5	IO204NDB3
N6	IO203NDB3
N7	IO203PDB3
N8	V_{CCI}B3
N9	V_{CC}
N10	GND
N11	GND
N12	GND
N13	GND
N14	V_{CC}
N15	V_{CCI}B1
N16	IO95NPB1

484-Pin FBGA	
Pin Number	A3P1000L Function
N17	IO100NPB1
N18	IO102NDB1
N19	IO102PDB1
N20	NC
N21	IO101NPB1
N22	IO103PDB1
P1	NC
P2	IO199PDB3
P3	IO199NDB3
P4	IO202NDB3
P5	IO202PDB3
P6	IO196PPB3
P7	IO193PPB3
P8	V_{CCI}B3
P9	GND
P10	V_{CC}
P11	V_{CC}
P12	V_{CC}
P13	V_{CC}
P14	GND
P15	V_{CCI}B1
P16	GDB0/IO112NPB1
P17	IO106NDB1
P18	IO106PDB1
P19	IO107PDB1
P20	NC
P21	IO104PDB1
P22	IO103NDB1
R1	NC
R2	IO197PPB3
R3	V_{CC}
R4	IO197NPB3
R5	IO196NPB3
R6	IO193NPB3
R7	GEC0/IO190NPB3
R8	VMV3

484-Pin FBGA	
Pin Number	A3P1000L Function
R9	V_{CCI}B2
R10	V_{CCI}B2
R11	IO147RSB2
R12	IO136RSB2
R13	V_{CCI}B2
R14	V_{CCI}B2
R15	VMV2
R16	IO110NDB1
R17	GDB1/IO112PPB1
R18	GDC1/IO111PDB1
R19	IO107NDB1
R20	V_{CC}
R21	IO104NDB1
R22	IO105PDB1
T1	IO198PDB3
T2	IO198NDB3
T3	NC
T4	IO194PPB3
T5	IO192PPB3
T6	GEC1/IO190PPB3
T7	IO192NPB3
T8	GNDQ
T9	GEA2/IO187RSB2
T10	IO161RSB2
T11	IO155RSB2
T12	IO141RSB2
T13	IO129RSB2
T14	IO124RSB2
T15	GNDQ
T16	IO110PDB1
T17	V_{JTAG}
T18	GDC0/IO111NDB1
T19	GDA1/IO113PDB1
T20	NC
T21	IO108PDB1
T22	IO105NDB1

484-Pin FBGA	
Pin Number	A3P1000L Function
U1	IO195PDB3
U2	IO195NDB3
U3	IO194NPB3
U4	GEB1/IO189PDB3
U5	GEB0/IO189NDB3
U6	VMV2
U7	IO179RSB2
U8	IO171RSB2
U9	IO165RSB2
U10	IO159RSB2
U11	IO151RSB2
U12	IO137RSB2
U13	IO134RSB2
U14	IO128RSB2
U15	VMV1
U16	TCK
U17	V_{PUMP}
U18	TRST
U19	GDA0/IO113NDB1
U20	NC
U21	IO108NDB1
U22	IO109PDB1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO188PDB3
V5	GEA0/IO188NDB3
V6	IO184RSB2
V7	GEC2/IO185RSB2
V8	IO168RSB2
V9	IO163RSB2
V10	IO157RSB2
V11	IO149RSB2
V12	IO143RSB2
V13	IO138RSB2
V14	IO131RSB2

484-Pin FBGA	
Pin Number	**A3P1000L Function**
V15	IO125RSB2
V16	GDB2/IO115RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO109NDB1
W1	NC
W2	IO191PDB3
W3	NC
W4	GND
W5	IO183RSB2
W6	FF/GEB2/IO186RSB2
W7	IO172RSB2
W8	IO170RSB2
W9	IO164RSB2
W10	IO158RSB2
W11	IO153RSB2
W12	IO142RSB2
W13	IO135RSB2
W14	IO130RSB2
W15	GDC2/IO116RSB2
W16	IO120RSB2
W17	GDA2/IO114RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	V_{CCI}B3
Y2	IO191NDB3
Y3	NC
Y4	IO182RSB2
Y5	GND
Y6	IO177RSB2

484-Pin FBGA	
Pin Number	**A3P1000L Function**
Y7	IO174RSB2
Y8	V_{CC}
Y9	V_{CC}
Y10	IO154RSB2
Y11	IO148RSB2
Y12	IO140RSB2
Y13	NC
Y14	V_{CC}
Y15	V_{CC}
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	V_{CCI}B1

484-Pin FBGA	
Pin Number	A3PE3000L Function
A1	GND
A2	GND
A3	V_{CCI}B0
A4	IO10NDB0V1
A5	IO10PDB0V1
A6	IO16NDB0V1
A7	IO16PDB0V1
A8	IO18PDB0V2
A9	IO24PDB0V2
A10	IO28NDB0V3
A11	IO28PDB0V3
A12	IO46PDB1V0
A13	IO54PDB1V1
A14	IO56NDB1V1
A15	IO56PDB1V1
A16	IO64NDB1V2
A17	IO64PDB1V2
A18	IO72NDB1V3
A19	IO74NDB1V4
A20	V_{CCI}B1
A21	GND
A22	GND
AA1	GND
AA2	V_{CCI}B6
AA3	IO228PDB5V4
AA4	IO224PDB5V3
AA5	IO218NDB5V3
AA6	IO218PDB5V3
AA7	IO212NDB5V2
AA8	IO212PDB5V2
AA9	IO198PDB5V0
AA10	IO198NDB5V0
AA11	IO188PPB4V4
AA12	IO180NDB4V3
AA13	IO180PDB4V3
AA14	IO170NDB4V2

484-Pin FBGA	
Pin Number	A3PE3000L Function
AA15	IO170PDB4V2
AA16	IO166NDB4V1
AA17	IO166PDB4V1
AA18	IO160NDB4V0
AA19	IO160PDB4V0
AA20	IO158NPB4V0
AA21	V_{CCI}B3
AA22	GND
AB1	GND
AB2	GND
AB3	V_{CCI}B5
AB4	IO216NDB5V2
AB5	IO216PDB5V2
AB6	IO210NDB5V2
AB7	IO210PDB5V2
AB8	IO208NDB5V1
AB9	IO208PDB5V1
AB10	IO197NDB5V0
AB11	IO197PDB5V0
AB12	IO174NDB4V2
AB13	IO174PDB4V2
AB14	IO172NDB4V2
AB15	IO172PDB4V2
AB16	IO168NDB4V1
AB17	IO168PDB4V1
AB18	IO162NDB4V1
AB19	IO162PDB4V1
AB20	V_{CCI}B4
AB21	GND
AB22	GND
B1	GND
B2	V_{CCI}B7
B3	IO06PPB0V0
B4	IO08NDB0V0
B5	IO08PDB0V0
B6	IO14NDB0V1

484-Pin FBGA	
Pin Number	A3PE3000L Function
B7	IO14PDB0V1
B8	IO18NDB0V2
B9	IO24NDB0V2
B10	IO34PDB0V4
B11	IO40PDB0V4
B12	IO46NDB1V0
B13	IO54NDB1V1
B14	IO62NDB1V2
B15	IO62PDB1V2
B16	IO68NDB1V3
B17	IO68PDB1V3
B18	IO72PDB1V3
B19	IO74PDB1V4
B20	IO76NPB1V4
B21	V_{CCI}B2
B22	GND
C1	V_{CCI}B7
C2	IO303PDB7V3
C3	IO305PDB7V3
C4	IO06NPB0V0
C5	GND
C6	IO12NDB0V1
C7	IO12PDB0V1
C8	V_{CC}
C9	V_{CC}
C10	IO34NDB0V4
C11	IO40NDB0V4
C12	IO48NDB1V0
C13	IO48PDB1V0
C14	V_{CC}
C15	V_{CC}
C16	IO70NDB1V3
C17	IO70PDB1V3
C18	GND
C19	IO76PPB1V4
C20	IO88NDB2V0

484-Pin FBGA	
Pin Number	A3PE3000L Function
C21	IO94PPB2V1
C22	V_{CCI}B2
D1	IO293PDB7V2
D2	IO303NDB7V3
D3	IO305NDB7V3
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO20PDB0V2
D9	IO22PDB0V2
D10	IO30PDB0V3
D11	IO38NDB0V4
D12	IO52NDB1V1
D13	IO52PDB1V1
D14	IO66NDB1V3
D15	IO66PDB1V3
D16	GBB1/IO80PDB1V4
D17	GBA0/IO81NDB1V4
D18	GBA1/IO81PDB1V4
D19	GND
D20	IO88PDB2V0
D21	IO90PDB2V1
D22	IO94NPB2V1
E1	IO293NDB7V2
E2	IO299PPB7V3
E3	GND
E4	GAB2/IO308PDB7V4
E5	GAA2/IO309PDB7V4
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO20NDB0V2
E9	IO22NDB0V2
E10	IO30NDB0V3
E11	IO38PDB0V4
E12	IO44NDB1V0

484-Pin FBGA	
Pin Number	A3PE3000L Function
E13	IO58NDB1V2
E14	IO58PDB1V2
E15	GBC1/IO79PDB1V4
E16	GBB0/IO80NDB1V4
E17	GNDQ
E18	GBA2/IO82PDB2V0
E19	IO86NDB2V0
E20	GND
E21	IO90NDB2V1
E22	IO98PDB2V2
F1	IO299NPB7V3
F2	IO301NDB7V3
F3	IO301PDB7V3
F4	IO308NDB7V4
F5	IO309NDB7V4
F6	VMV7
F7	V_{CCPLA}
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO32NDB0V3
F11	IO32PDB0V3
F12	IO44PDB1V0
F13	IO50NDB1V1
F14	IO60PDB1V2
F15	GBC0/IO79NDB1V4
F16	V_{CCPLB}
F17	VMV2
F18	IO82NDB2V0
F19	IO86PDB2V0
F20	IO96PDB2V1
F21	IO96NDB2V1
F22	IO98NDB2V2
G1	IO289NDB7V1
G2	IO289PDB7V1
G3	IO291PPB7V2
G4	IO295PDB7V2

484-Pin FBGA	
Pin Number	A3PE3000L Function
G5	IO297PDB7V2
G6	GAC2/IO307PDB7V4
G7	V_{COMPLA}
G8	GNDQ
G9	IO26NDB0V3
G10	IO26PDB0V3
G11	IO36PDB0V4
G12	IO42PDB1V0
G13	IO50PDB1V1
G14	IO60NDB1V2
G15	GNDQ
G16	V_{COMPLB}
G17	GBB2/IO83PDB2V0
G18	IO92PDB2V1
G19	IO92NDB2V1
G20	IO102PDB2V2
G21	IO102NDB2V2
G22	IO105NDB2V2
H1	IO286PSB7V1
H2	IO291NPB7V2
H3	V_{CC}
H4	IO295NDB7V2
H5	IO297NDB7V2
H6	IO307NDB7V4
H7	IO287PDB7V1
H8	VMV0
H9	V_{CCI}B0
H10	V_{CCI}B0
H11	IO36NDB0V4
H12	IO42NDB1V0
H13	V_{CCI}B1
H14	V_{CCI}B1
H15	VMV1
H16	GBC2/IO84PDB2V0
H17	IO83NDB2V0
H18	IO100NDB2V2

484-Pin FBGA	
Pin Number	A3PE3000L Function
H19	IO100PDB2V2
H20	V_{CC}
H21	VMV2
H22	IO105PDB2V2
J1	IO285NDB7V1
J2	IO285PDB7V1
J3	VMV7
J4	IO279PDB7V0
J5	IO283PDB7V1
J6	IO281PDB7V0
J7	IO287NDB7V1
J8	V_{CCI}B7
J9	GND
J10	V_{CC}
J11	V_{CC}
J12	V_{CC}
J13	V_{CC}
J14	GND
J15	V_{CCI}B2
J16	IO84NDB2V0
J17	IO104NDB2V2
J18	IO104PDB2V2
J19	IO106PPB2V3
J20	GNDQ
J21	IO109PDB2V3
J22	IO107PDB2V3
K1	IO277NDB7V0
K2	IO277PDB7V0
K3	GNDQ
K4	IO279NDB7V0
K5	IO283NDB7V1
K6	IO281NDB7V0
K7	GFC1/IO275PPB7V0
K8	V_{CCI}B7
K9	V_{CC}
K10	GND

484-Pin FBGA	
Pin Number	A3PE3000L Function
K11	GND
K12	GND
K13	GND
K14	V_{CC}
K15	V_{CCI}B2
K16	GCC1/IO112PPB2V3
K17	IO108NDB2V3
K18	IO108PDB2V3
K19	IO110NPB2V3
K20	IO106NPB2V3
K21	IO109NDB2V3
K22	IO107NDB2V3
L1	IO257PSB6V2
L2	IO276PDB7V0
L3	IO276NDB7V0
L4	GFB0/IO274NPB7V0
L5	GFA0/IO273NDB6V4
L6	GFB1/IO274PPB7V0
L7	V_{COMPLF}
L8	GFC0/IO275NPB7V0
L9	V_{CC}
L10	GND
L11	GND
L12	GND
L13	GND
L14	V_{CC}
L15	GCC0/IO112NPB2V3
L16	GCB1/IO113PPB2V3
L17	GCA0/IO114NPB3V0
L18	V_{COMPLC}
L19	GCB0/IO113NPB2V3
L20	IO110PPB2V3
L21	IO111NDB2V3
L22	IO111PDB2V3
M1	GNDQ
M2	IO255NPB6V2

484-Pin FBGA	
Pin Number	A3PE3000L Function
M3	IO272NDB6V4
M4	GFA2/IO272PDB6V4
M5	GFA1/IO273PDB6V4
M6	V_{CCPLF}
M7	IO271NDB6V4
M8	GFB2/IO271PDB6V4
M9	V_{CC}
M10	GND
M11	GND
M12	GND
M13	GND
M14	V_{CC}
M15	GCB2/IO116PPB3V0
M16	GCA1/IO114PPB3V0
M17	GCC2/IO117PPB3V0
M18	V_{CCPLC}
M19	GCA2/IO115PDB3V0
M20	IO115NDB3V0
M21	IO126PDB3V1
M22	IO124PSB3V1
N1	IO255PPB6V2
N2	IO253NDB6V2
N3	VMV6
N4	GFC2/IO270PPB6V4
N5	IO261PPB6V3
N6	IO263PDB6V3
N7	IO263NDB6V3
N8	V_{CCI}B6
N9	V_{CC}
N10	GND
N11	GND
N12	GND
N13	GND
N14	V_{CC}
N15	V_{CCI}B3
N16	IO116NPB3V0

484-Pin FBGA	
Pin Number	A3PE3000L Function
N17	IO132NPB3V2
N18	IO117NPB3V0
N19	IO132PPB3V2
N20	GNDQ
N21	IO126NDB3V1
N22	IO128PDB3V1
P1	IO247PDB6V1
P2	IO253PDB6V2
P3	IO270NPB6V4
P4	IO261NPB6V3
P5	IO249PPB6V1
P6	IO259PDB6V3
P7	IO259NDB6V3
P8	V_{CCI}B6
P9	GND
P10	V_{CC}
P11	V_{CC}
P12	V_{CC}
P13	V_{CC}
P14	GND
P15	V_{CCI}B3
P16	GDB0/IO152NPB3V4
P17	IO136NDB3V2
P18	IO136PDB3V2
P19	IO138PDB3V3
P20	VMV3
P21	IO130PDB3V2
P22	IO128NDB3V1
R1	IO247NDB6V1
R2	IO245PDB6V1
R3	V_{CC}
R4	IO249NPB6V1
R5	IO251NDB6V2
R6	IO251PDB6V2
R7	GEC0/IO236NPB6V0
R8	VMV5

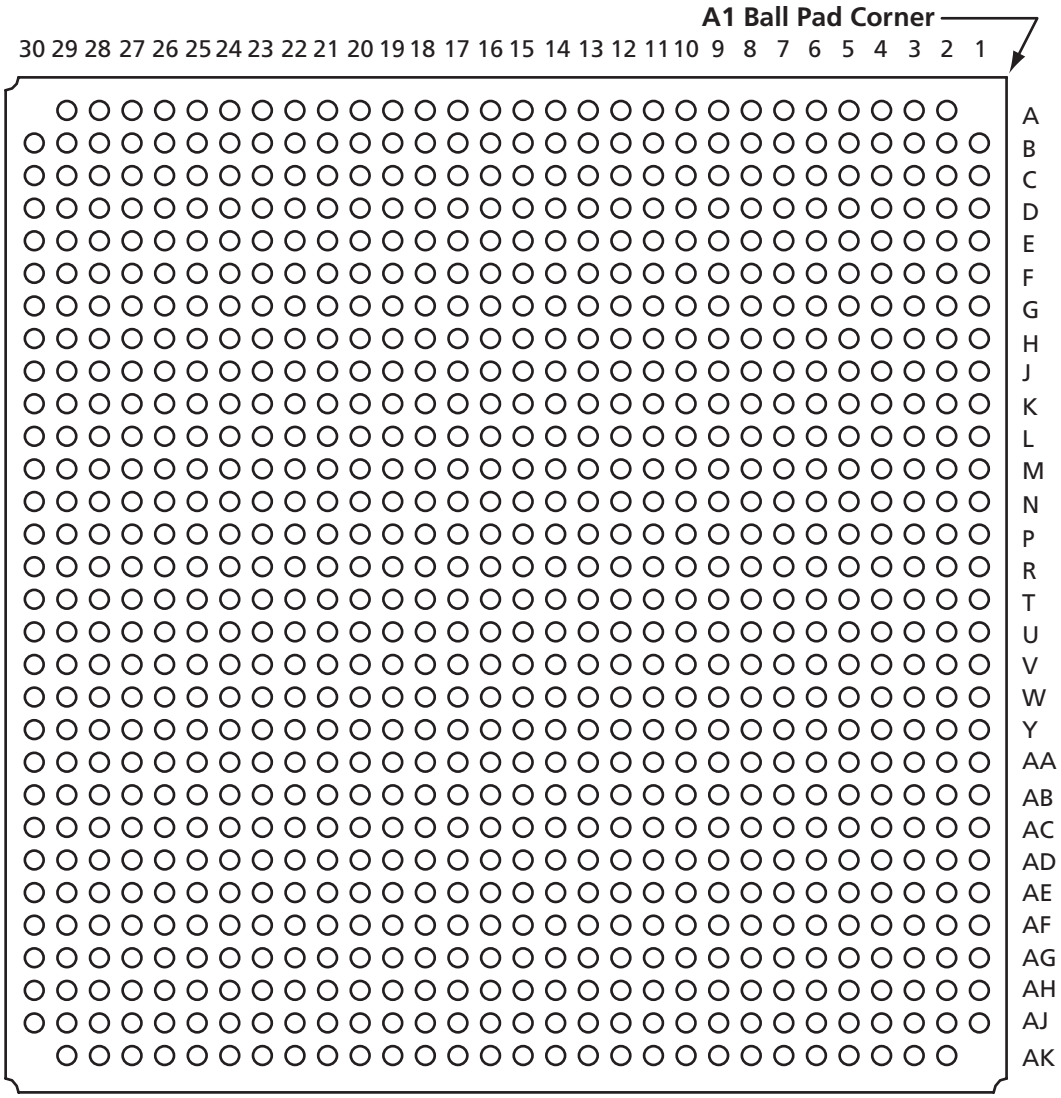
484-Pin FBGA	
Pin Number	A3PE3000L Function
R9	V_{CCI}B5
R10	V_{CCI}B5
R11	IO196NDB5V0
R12	IO196PDB5V0
R13	V_{CCI}B4
R14	V_{CCI}B4
R15	VMV3
R16	V_{CCPLD}
R17	GDB1/IO152PPB3V4
R18	GDC1/IO151PDB3V4
R19	IO138NDB3V3
R20	V_{CC}
R21	IO130NDB3V2
R22	IO134PDB3V2
T1	IO243PPB6V1
T2	IO245NDB6V1
T3	IO243NPB6V1
T4	IO241PDB6V0
T5	IO241NDB6V0
T6	GEC1/IO236PPB6V0
T7	V_{COMPLE}
T8	GNDQ
T9	GEA2/IO233PPB5V4
T10	IO206NDB5V1
T11	IO202NDB5V1
T12	IO194NDB5V0
T13	IO186NDB4V4
T14	IO186PDB4V4
T15	GNDQ
T16	V_{COMPLD}
T17	V_{JTAG}
T18	GDC0/IO151NDB3V4
T19	GDA1/IO153PDB3V4
T20	IO144PDB3V3
T21	IO140PDB3V3
T22	IO134NDB3V2

484-Pin FBGA	
Pin Number	A3PE3000L Function
U1	IO240PPB6V0
U2	IO238PDB6V0
U3	IO238NDB6V0
U4	GEB1/IO235PDB6V0
U5	GEB0/IO235NDB6V0
U6	VMV6
U7	V_{CCPLE}
U8	IO233NPB5V4
U9	IO222PPB5V3
U10	IO206PDB5V1
U11	IO202PDB5V1
U12	IO194PDB5V0
U13	IO176NDB4V2
U14	IO176PDB4V2
U15	VMV4
U16	TCK
U17	V_{PUMP}
U18	TRST
U19	GDA0/IO153NDB3V4
U20	IO144NDB3V3
U21	IO140NDB3V3
U22	IO142PDB3V3
V1	IO239PDB6V0
V2	IO240NPB6V0
V3	GND
V4	GEA1/IO234PDB6V0
V5	GEA0/IO234NDB6V0
V6	GNDQ
V7	GEC2/IO231PDB5V4
V8	IO222NPB5V3
V9	IO204NDB5V1
V10	IO204PDB5V1
V11	IO195NDB5V0
V12	IO195PDB5V0
V13	IO178NDB4V3
V14	IO178PDB4V3

484-Pin FBGA	
Pin Number	**A3PE3000L Function**
V15	IO155NDB4V0
V16	GDB2/IO155PDB4V0
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	IO146PDB3V4
V22	IO142NDB3V3
W1	IO239NDB6V0
W2	IO237PDB6V0
W3	IO230PSB5V4
W4	GND
W5	IO232NDB5V4
W6	FF/GEB2/IO232PDB5V4
W7	IO231NDB5V4
W8	IO214NDB5V2
W9	IO214PDB5V2
W10	IO200NDB5V0
W11	IO192NDB4V4
W12	IO184NDB4V3
W13	IO184PDB4V3
W14	IO156NDB4V0
W15	GDC2/IO156PDB4V0
W16	IO154NDB4V0
W17	GDA2/IO154PDB4V0
W18	TMS
W19	GND
W20	IO150NDB3V4
W21	IO146NDB3V4
W22	IO148PPB3V4
Y1	V_{CCI}B6
Y2	IO237NDB6V0
Y3	IO228NDB5V4
Y4	IO224NDB5V3
Y5	GND

484-Pin FBGA	
Pin Number	**A3PE3000L Function**
Y6	IO220NDB5V3
Y7	IO220PDB5V3
Y8	V_{CC}
Y9	V_{CC}
Y10	IO200PDB5V0
Y11	IO192PDB4V4
Y12	IO188NPB4V4
Y13	IO187PSB4V4
Y14	V_{CC}
Y15	V_{CC}
Y16	IO164NDB4V1
Y17	IO164PDB4V1
Y18	GND
Y19	IO158PPB4V0
Y20	IO150PDB3V4
Y21	IO148NPB3V4
Y22	V_{CCI}B3

896-Pin FBGA



Note: This is the bottom view.

Figure 4 •

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

896-Pin FBGA	
Pin Number	A3PE3000L Function
A2	GND
A3	GND
A4	IO14NPB0V1
A5	GND
A6	IO07NPB0V0
A7	GND
A8	IO09NDB0V1
A9	IO17NDB0V2
A10	IO17PDB0V2
A11	IO21NDB0V2
A12	IO21PDB0V2
A13	IO33NDB0V4
A14	IO33PDB0V4
A15	IO35NDB0V4
A16	IO35PDB0V4
A17	IO41NDB1V0
A18	IO43NDB1V0
A19	IO43PDB1V0
A20	IO45NDB1V0
A21	IO45PDB1V0
A22	IO57NDB1V2
A23	IO57PDB1V2
A24	GND
A25	IO69PPB1V3
A26	GND
A27	GBC1/IO79PPB1V4
A28	GND
A29	GND
AA1	IO256PDB6V2
AA2	IO248PDB6V1
AA3	IO248NDB6V1
AA4	IO246NDB6V1
AA5	GEA1/IO234PDB6V0
AA6	GEA0/IO234NDB6V0
AA7	IO243PPB6V1
AA8	IO245NDB6V1

896-Pin FBGA	
Pin Number	A3PE3000L Function
AA9	GEB1/IO235PPB6V0
AA10	V_{CC}
AA11	IO226PPB5V4
AA12	V_{CCI}B5
AA13	V_{CCI}B5
AA14	V_{CCI}B5
AA15	V_{CCI}B5
AA16	V_{CCI}B4
AA17	V_{CCI}B4
AA18	V_{CCI}B4
AA19	V_{CCI}B4
AA20	IO174PDB4V2
AA21	V_{CC}
AA22	IO142NPB3V3
AA23	IO144NDB3V3
AA24	IO144PDB3V3
AA25	IO146NDB3V4
AA26	IO146PDB3V4
AA27	IO147PDB3V4
AA28	IO139NDB3V3
AA29	IO139PDB3V3
AA30	IO133NDB3V2
AB1	IO256NDB6V2
AB2	IO244PDB6V1
AB3	IO244NDB6V1
AB4	IO241PDB6V0
AB5	IO241NDB6V0
AB6	IO243NPB6V1
AB7	V_{CCI}B6
AB8	V_{CCPLE}
AB9	V_{CC}
AB10	IO222PDB5V3
AB11	IO218PPB5V3
AB12	IO206NDB5V1
AB13	IO206PDB5V1
AB14	IO198NDB5V0

896-Pin FBGA	
Pin Number	A3PE3000L Function
AB15	IO198PDB5V0
AB16	IO192NDB4V4
AB17	IO192PDB4V4
AB18	IO178NDB4V3
AB19	IO178PDB4V3
AB20	IO174NDB4V2
AB21	IO162NPB4V1
AB22	V_{CC}
AB23	V_{CCPLD}
AB24	V_{CCI}B3
AB25	IO150PDB3V4
AB26	IO148PDB3V4
AB27	IO147NDB3V4
AB28	IO145PDB3V3
AB29	IO143PDB3V3
AB30	IO137PDB3V2
AC1	IO254PDB6V2
AC2	IO254NDB6V2
AC3	IO240PDB6V0
AC4	GEC1/IO236PDB6V0
AC5	IO237PDB6V0
AC6	IO237NDB6V0
AC7	V_{COMPLE}
AC8	GND
AC9	IO226NPB5V4
AC10	IO222NDB5V3
AC11	IO216NPB5V2
AC12	IO210NPB5V2
AC13	IO204NDB5V1
AC14	IO204PDB5V1
AC15	IO194NDB5V0
AC16	IO188NDB4V4
AC17	IO188PDB4V4
AC18	IO182PPB4V3
AC19	IO170NPB4V2
AC20	IO164NDB4V1

896-Pin FBGA	
Pin Number	A3PE3000L Function
AC21	IO164PDB4V1
AC22	IO162PPB4V1
AC23	GND
AC24	V_{COMPLD}
AC25	IO150NDB3V4
AC26	IO148NDB3V4
AC27	GDA1/IO153PDB3V4
AC28	IO145NDB3V3
AC29	IO143NDB3V3
AC30	IO137NDB3V2
AD1	GND
AD2	IO242NPB6V1
AD3	IO240NDB6V0
AD4	GEC0/IO236NDB6V0
AD5	V_{CCI}B6
AD6	GNDQ
AD6	GNDQ
AD7	V_{CC}
AD8	VMV5
AD9	V_{CCI}B5
AD10	IO224PPB5V3
AD11	IO218NPB5V3
AD12	IO216PPB5V2
AD13	IO210PPB5V2
AD14	IO202PPB5V1
AD15	IO194PDB5V0
AD16	IO190PDB4V4
AD17	IO182NPB4V3
AD18	IO176NDB4V2
AD19	IO176PDB4V2
AD20	IO170PPB4V2
AD21	IO166PDB4V1
AD22	V_{CCI}B4
AD23	TCK
AD24	V_{CC}
AD25	TRST

896-Pin FBGA	
Pin Number	A3PE3000L Function
AD26	V_{CCI}B3
AD27	GDA0/IO153NDB3V4
AD28	GDC0/IO151NDB3V4
AD29	GDC1/IO151PDB3V4
AD30	GND
AE1	IO242PPB6V1
AE2	V_{CC}
AE3	IO239PDB6V0
AE4	IO239NDB6V0
AE5	VMV6
AE5	VMV6
AE6	GND
AE7	GNDQ
AE8	IO230NDB5V4
AE9	IO224NPB5V3
AE10	IO214NPB5V2
AE11	IO212NDB5V2
AE12	IO212PDB5V2
AE13	IO202NPB5V1
AE14	IO200NDB5V0
AE15	IO196PDB5V0
AE16	IO190NDB4V4
AE17	IO184PDB4V3
AE18	IO184NDB4V3
AE19	IO172PDB4V2
AE20	IO172NDB4V2
AE21	IO166NDB4V1
AE22	IO160PDB4V0
AE23	GNDQ
AE24	VMV4
AE25	GND
AE26	GDB0/IO152NDB3V4
AE27	GDB1/IO152PDB3V4
AE28	VMV3
AE28	VMV3
AE29	V_{CC}

896-Pin FBGA	
Pin Number	A3PE3000L Function
AE30	IO149PDB3V4
AF1	GND
AF2	IO238PPB6V0
AF3	V_{CCI}B6
AF4	IO220NPB5V3
AF5	V_{CC}
AF6	IO228NDB5V4
AF7	V_{CCI}B5
AF8	IO230PDB5V4
AF9	IO229NDB5V4
AF10	IO229PDB5V4
AF11	IO214PPB5V2
AF12	IO208NDB5V1
AF13	IO208PDB5V1
AF14	IO200PDB5V0
AF15	IO196NDB5V0
AF16	IO186NDB4V4
AF17	IO186PDB4V4
AF18	IO180NDB4V3
AF19	IO180PDB4V3
AF20	IO168NDB4V1
AF21	IO168PDB4V1
AF22	IO160NDB4V0
AF23	IO158NPB4V0
AF24	V_{CCI}B4
AF25	IO154NPB4V0
AF26	V_{CC}
AF27	TDO
AF28	V_{CCI}B3
AF29	GNDQ
AF29	GNDQ
AF30	GND
AG1	IO238NPB6V0
AG2	V_{CC}
AG3	IO232NPB5V4
AG4	GND

896-Pin FBGA	
Pin Number	A3PE3000L Function
AG5	IO220PPB5V3
AG6	IO228PDB5V4
AG7	IO231NDB5V4
AG8	GEC2/IO231PDB5V4
AG9	IO225NPB5V3
AG10	IO223NPB5V3
AG11	IO221PDB5V3
AG12	IO221NDB5V3
AG13	IO205NPB5V1
AG14	IO199NDB5V0
AG15	IO199PDB5V0
AG16	IO187NDB4V4
AG17	IO187PDB4V4
AG18	IO181NDB4V3
AG19	IO171PPB4V2
AG20	IO165NPB4V1
AG21	IO161NPB4V0
AG22	IO159NDB4V0
AG23	IO159PDB4V0
AG24	IO158PPB4V0
AG25	GDB2/IO155PDB4V0
AG26	GDA2/IO154PPB4V0
AG27	GND
AG28	V_{JTAG}
AG29	V_{CC}
AG30	IO149NDB3V4
AH1	GND
AH2	IO233NPB5V4
AH3	V_{CC}
AH4	FF/GEB2/IO232PPB5V4
AH5	V_{CCI}B5
AH6	IO219NDB5V3
AH7	IO219PDB5V3
AH8	IO227NDB5V4
AH9	IO227PDB5V4

896-Pin FBGA	
Pin Number	A3PE3000L Function
AH10	IO225PPB5V3
AH11	IO223PPB5V3
AH12	IO211NDB5V2
AH13	IO211PDB5V2
AH14	IO205PPB5V1
AH15	IO195NDB5V0
AH16	IO185NDB4V3
AH17	IO185PDB4V3
AH18	IO181PDB4V3
AH19	IO177NDB4V2
AH20	IO171NPB4V2
AH21	IO165PPB4V1
AH22	IO161PPB4V0
AH23	IO157NDB4V0
AH24	IO157PDB4V0
AH25	IO155NDB4V0
AH26	V_{CCI}B4
AH27	TDI
AH28	V_{CC}
AH29	V_{PUMP}
AH30	GND
AJ1	GND
AJ2	GND
AJ3	GEA2/IO233PPB5V4
AJ4	V_{CC}
AJ5	IO217NPB5V2
AJ6	V_{CC}
AJ7	IO215NPB5V2
AJ8	IO213NDB5V2
AJ9	IO213PDB5V2
AJ10	IO209NDB5V1
AJ11	IO209PDB5V1
AJ12	IO203NDB5V1
AJ13	IO203PDB5V1
AJ14	IO197NDB5V0
AJ15	IO195PDB5V0

896-Pin FBGA	
Pin Number	A3PE3000L Function
AJ16	IO183NDB4V3
AJ17	IO183PDB4V3
AJ18	IO179NPB4V3
AJ19	IO177PDB4V2
AJ20	IO173NDB4V2
AJ21	IO173PDB4V2
AJ22	IO163NDB4V1
AJ23	IO163PDB4V1
AJ24	IO167NPB4V1
AJ25	V_{CC}
AJ26	IO156NPB4V0
AJ27	V_{CC}
AJ28	TMS
AJ29	GND
AJ30	GND
AK2	GND
AK3	GND
AK4	IO217PPB5V2
AK5	GND
AK6	IO215PPB5V2
AK7	GND
AK8	IO207NDB5V1
AK9	IO207PDB5V1
AK10	IO201NDB5V0
AK11	IO201PDB5V0
AK12	IO193NDB4V4
AK13	IO193PDB4V4
AK14	IO197PDB5V0
AK15	IO191NDB4V4
AK16	IO191PDB4V4
AK17	IO189NDB4V4
AK18	IO189PDB4V4
AK19	IO179PPB4V3
AK20	IO175NDB4V2
AK21	IO175PDB4V2
AK22	IO169NDB4V1

896-Pin FBGA	
Pin Number	A3PE3000L Function
AK23	IO169PDB4V1
AK24	GND
AK25	IO167PPB4V1
AK26	GND
AK27	GDC2/IO156PPB4V0
AK28	GND
AK29	GND
B1	GND
B2	GND
B3	GAA2/IO309PPB7V4
B4	V_{CC}
B5	IO14PPB0V1
B6	V_{CC}
B7	IO07PPB0V0
B8	IO09PDB0V1
B9	IO15PPB0V1
B10	IO19NDB0V2
B11	IO19PDB0V2
B12	IO29NDB0V3
B13	IO29PDB0V3
B14	IO31PPB0V3
B15	IO37NDB0V4
B16	IO37PDB0V4
B17	IO41PDB1V0
B18	IO51NDB1V1
B19	IO59PDB1V2
B20	IO53PDB1V1
B21	IO53NDB1V1
B22	IO61NDB1V2
B23	IO61PDB1V2
B24	IO69NPB1V3
B25	V_{CC}
B26	GBC0/IO79NPB1V4
B27	V_{CC}
B28	IO64NPB1V2
B29	GND

896-Pin FBGA	
Pin Number	A3PE3000L Function
B30	GND
C1	GND
C2	IO309NPB7V4
C3	V_{CC}
C4	GAA0/IO00NPB0V0
C5	V_{CCI}B0
C6	IO03PDB0V0
C7	IO03NDB0V0
C8	GAB1/IO01PDB0V0
C9	IO05PDB0V0
C10	IO15NPB0V1
C11	IO25NDB0V3
C12	IO25PDB0V3
C13	IO31NPB0V3
C14	IO27NDB0V3
C15	IO39NDB0V4
C16	IO39PDB0V4
C17	IO55PPB1V1
C18	IO51PDB1V1
C19	IO59NDB1V2
C20	IO63NDB1V2
C21	IO63PDB1V2
C22	IO67NDB1V3
C23	IO67PDB1V3
C24	IO75NDB1V4
C25	IO75PDB1V4
C26	V_{CCI}B1
C27	IO64PPB1V2
C28	V_{CC}
C29	GBA1/IO81PPB1V4
C30	GND
D1	IO303PPB7V3
D2	V_{CC}
D3	IO305NPB7V3
D4	GND
D5	GAA1/IO00PPB0V0

896-Pin FBGA	
Pin Number	A3PE3000L Function
D6	GAC1/IO02PDB0V0
D7	IO06NPB0V0
D8	GAB0/IO01NDB0V0
D9	IO05NDB0V0
D10	IO11NDB0V1
D11	IO11PDB0V1
D12	IO23NDB0V2
D13	IO23PDB0V2
D14	IO27PDB0V3
D15	IO40PDB0V4
D16	IO47NDB1V0
D17	IO47PDB1V0
D18	IO55NPB1V1
D19	IO65NDB1V3
D20	IO65PDB1V3
D21	IO71NDB1V3
D22	IO71PDB1V3
D23	IO73NDB1V4
D24	IO73PDB1V4
D25	IO74NDB1V4
D26	GBB0/IO80NPB1V4
D27	GND
D28	GBA0/IO81NPB1V4
D29	V_{CC}
D30	GBA2/IO82PPB2V0
E1	GND
E2	IO303NPB7V3
E3	V_{CCI}B7
E4	IO305PPB7V3
E5	V_{CC}
E6	GAC0/IO02NDB0V0
E7	V_{CCI}B0
E8	IO06PPB0V0
E9	IO24NDB0V2
E10	IO24PDB0V2
E11	IO13NDB0V1

896-Pin FBGA	
Pin Number	A3PE3000L Function
E12	IO13PDB0V1
E13	IO34NDB0V4
E14	IO34PDB0V4
E15	IO40NDB0V4
E16	IO49NDB1V1
E17	IO49PDB1V1
E18	IO50PDB1V1
E19	IO58PDB1V2
E20	IO60NDB1V2
E21	IO77PDB1V4
E22	IO68NDB1V3
E23	IO68PDB1V3
E24	V_{CCI}B1
E25	IO74PDB1V4
E26	V_{CC}
E27	GBB1/IO80PPB1V4
E28	V_{CCI}B2
E29	IO82NPB2V0
E30	GND
F1	IO296PPB7V2
F2	V_{CC}
F3	IO306PDB7V4
F4	IO297PDB7V2
F5	VMV7
F5	VMV7
F6	GND
F7	GNDQ
F8	IO12NDB0V1
F9	IO12PDB0V1
F10	IO10PDB0V1
F11	IO16PDB0V1
F12	IO22NDB0V2
F13	IO30NDB0V3
F14	IO30PDB0V3
F15	IO36PDB0V4
F16	IO48NDB1V0

896-Pin FBGA	
Pin Number	A3PE3000L Function
F17	IO48PDB1V0
F18	IO50NDB1V1
F19	IO58NDB1V2
F20	IO60PDB1V2
F21	IO77NDB1V4
F22	IO72NDB1V3
F23	IO72PDB1V3
F24	GNDQ
F25	GND
F26	VMV2
F26	VMV2
F27	IO86PDB2V0
F28	IO92PDB2V1
F29	V_{CC}
F30	IO100NPB2V2
G1	GND
G2	IO296NPB7V2
G3	IO306NDB7V4
G4	IO297NDB7V2
G5	V_{CCI}B7
G6	GNDQ
G6	GNDQ
G7	V_{CC}
G8	VMV0
G9	V_{CCI}B0
G10	IO10NDB0V1
G11	IO16NDB0V1
G12	IO22PDB0V2
G13	IO26PPB0V3
G14	IO38NPB0V4
G15	IO36NDB0V4
G16	IO46NDB1V0
G17	IO46PDB1V0
G18	IO56NDB1V1
G19	IO56PDB1V1
G20	IO66NDB1V3

896-Pin FBGA	
Pin Number	A3PE3000L Function
G21	IO66PDB1V3
G22	V_{CCI}B1
G23	VMV1
G24	V_{CC}
G25	GNDQ
G25	GNDQ
G26	V_{CCI}B2
G27	IO86NDB2V0
G28	IO92NDB2V1
G29	IO100PPB2V2
G30	GND
H1	IO294PDB7V2
H2	IO294NDB7V2
H3	IO300NDB7V3
H4	IO300PDB7V3
H5	IO295PDB7V2
H6	IO299PDB7V3
H7	V_{COMPLA}
H8	GND
H9	IO08NDB0V0
H10	IO08PDB0V0
H11	IO18PDB0V2
H12	IO26NPB0V3
H13	IO28NDB0V3
H14	IO28PDB0V3
H15	IO38PPB0V4
H16	IO42NDB1V0
H17	IO52NDB1V1
H18	IO52PDB1V1
H19	IO62NDB1V2
H20	IO62PDB1V2
H21	IO70NDB1V3
H22	IO70PDB1V3
H23	GND
H24	V_{COMPLB}
H25	GBC2/IO84PDB2V0

896-Pin FBGA	
Pin Number	A3PE3000L Function
H26	IO84NDB2V0
H27	IO96PDB2V1
H28	IO96NDB2V1
H29	IO89PDB2V0
H30	IO89NDB2V0
J1	IO290NDB7V2
J2	IO290PDB7V2
J3	IO302NDB7V3
J4	IO302PDB7V3
J5	IO295NDB7V2
J6	IO299NDB7V3
J7	V_{CCI}B7
J8	V_{CCPLA}
J9	V_{CC}
J10	IO04NPB0V0
J11	IO18NDB0V2
J12	IO20NDB0V2
J13	IO20PDB0V2
J14	IO32NDB0V3
J15	IO32PDB0V3
J16	IO42PDB1V0
J17	IO44NDB1V0
J18	IO44PDB1V0
J19	IO54NDB1V1
J20	IO54PDB1V1
J21	IO76NPB1V4
J22	V_{CC}
J23	V_{CCPLB}
J24	V_{CCI}B2
J25	IO90PDB2V1
J26	IO90NDB2V1
J27	GBB2/IO83PDB2V0
J28	IO83NDB2V0
J29	IO91PDB2V1
J30	IO91NDB2V1
K1	IO288NDB7V1

896-Pin FBGA	
Pin Number	A3PE3000L Function
K2	IO288PDB7V1
K3	IO304NDB7V3
K4	IO304PDB7V3
K5	GAB2/IO308PDB7V4
K6	IO308NDB7V4
K7	IO301PDB7V3
K8	IO301NDB7V3
K9	GAC2/IO307PPB7V4
K10	V_{CC}
K11	IO04PPB0V0
K12	V_{CCI}B0
K13	V_{CCI}B0
K14	V_{CCI}B0
K15	V_{CCI}B0
K16	V_{CCI}B1
K17	V_{CCI}B1
K18	V_{CCI}B1
K19	V_{CCI}B1
K20	IO76PPB1V4
K21	V_{CC}
K22	IO78PPB1V4
K23	IO88NDB2V0
K24	IO88PDB2V0
K25	IO94PDB2V1
K26	IO94NDB2V1
K27	IO85PDB2V0
K28	IO85NDB2V0
K29	IO93PDB2V1
K30	IO93NDB2V1
L1	IO286NDB7V1
L2	IO286PDB7V1
L3	IO298NDB7V3
L4	IO298PDB7V3
L5	IO283PDB7V1
L6	IO291NDB7V2
L7	IO291PDB7V2

896-Pin FBGA	
Pin Number	A3PE3000L Function
L8	IO293PDB7V2
L9	IO293NDB7V2
L10	IO307NPB7V4
L11	V_{CC}
L12	V_{CC}
L13	V_{CC}
L14	V_{CC}
L15	V_{CC}
L16	V_{CC}
L17	V_{CC}
L18	V_{CC}
L19	V_{CC}
L20	V_{CC}
L21	IO78NPB1V4
L22	IO104NPB2V2
L23	IO98NDB2V2
L24	IO98PDB2V2
L25	IO87PDB2V0
L26	IO87NDB2V0
L27	IO97PDB2V1
L28	IO101PDB2V2
L29	IO103PDB2V2
L30	IO119NDB3V0
M1	IO282NDB7V1
M2	IO282PDB7V1
M3	IO292NDB7V2
M4	IO292PDB7V2
M5	IO283NDB7V1
M6	IO285PDB7V1
M7	IO287PDB7V1
M8	IO289PDB7V1
M9	IO289NDB7V1
M10	V_{CCI}B7
M11	V_{CC}
M12	GND
M13	GND

896-Pin FBGA	
Pin Number	A3PE3000L Function
M14	GND
M15	GND
M16	GND
M17	GND
M18	GND
M19	GND
M20	V_{CC}
M21	$V_{CCI}B2$
M22	NC
M23	IO104PPB2V2
M24	IO102PDB2V2
M25	IO102NDB2V2
M26	IO95PDB2V1
M27	IO97NDB2V1
M28	IO101NDB2V2
M29	IO103NDB2V2
M30	IO119PDB3V0
N1	IO276PDB7V0
N2	IO278PDB7V0
N3	IO280PDB7V0
N4	IO284PDB7V1
N5	IO279PDB7V0
N6	IO285NDB7V1
N7	IO287NDB7V1
N8	IO281NDB7V0
N9	IO281PDB7V0
N10	$V_{CCI}B7$
N11	V_{CC}
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N17	GND
N18	GND
N19	GND

896-Pin FBGA	
Pin Number	A3PE3000L Function
N20	V_{CC}
N21	$V_{CCI}B2$
N22	IO106NDB2V3
N23	IO106PDB2V3
N24	IO108PDB2V3
N25	IO108NDB2V3
N26	IO95NDB2V1
N27	IO99NDB2V2
N28	IO99PDB2V2
N29	IO107PDB2V3
N30	IO107NDB2V3
P1	IO276NDB7V0
P2	IO278NDB7V0
P3	IO280NDB7V0
P4	IO284NDB7V1
P5	IO279NDB7V0
P6	GFC1/IO275PDB7V0
P7	GFC0/IO275NDB7V0
P8	IO277PDB7V0
P9	IO277NDB7V0
P10	$V_{CCI}B7$
P11	V_{CC}
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	GND
P18	GND
P19	GND
P20	V_{CC}
P21	$V_{CCI}B2$
P22	GCC1/IO112PDB2V3
P23	IO110PDB2V3
P24	IO110NDB2V3
P25	IO109PPB2V3

896-Pin FBGA	
Pin Number	A3PE3000L Function
P26	IO111NPB2V3
P27	IO105PDB2V2
P28	IO105NDB2V2
P29	GCC2/IO117PDB3V0
P30	IO117NDB3V0
R1	GFC2/IO270PDB6V4
R2	GFB1/IO274PPB7V0
R3	V_{COMPLF}
R4	GFA0/IO273NDB6V4
R5	GFB0/IO274NPB7V0
R6	IO271NDB6V4
R7	GFB2/IO271PDB6V4
R8	IO269PDB6V4
R9	IO269NDB6V4
R10	$V_{CCI}B7$
R11	V_{CC}
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R17	GND
R18	GND
R19	GND
R20	V_{CC}
R21	$V_{CCI}B2$
R22	GCC0/IO112NDB2V3
R23	GCB2/IO116PDB3V0
R24	IO118PDB3V0
R25	IO111PPB2V3
R26	IO122PPB3V1
R27	GCA0/IO114NPB3V0
R28	V_{COMPLC}
R29	GCB1/IO113PPB2V3
R30	IO115NPB3V0
T1	IO270NDB6V4

896-Pin FBGA	
Pin Number	A3PE3000L Function
T2	V_{CCPLF}
T3	GFA2/IO272PPB6V4
T4	GFA1/IO273PDB6V4
T5	IO272NPB6V4
T6	IO267NDB6V4
T7	IO267PDB6V4
T8	IO265PDB6V3
T9	IO263PDB6V3
T10	V_{CCI}B6
T11	V_{CC}
T12	GND
T13	GND
T14	GND
T15	GND
T16	GND
T17	GND
T18	GND
T19	GND
T20	V_{CC}
T21	V_{CCI}B3
T22	IO109NPB2V3
T23	IO116NDB3V0
T24	IO118NDB3V0
T25	IO122NPB3V1
T26	GCA1/IO114PPB3V0
T27	GCB0/IO113NPB2V3
T28	GCA2/IO115PPB3V0
T29	V_{CCPLC}
T30	IO121PDB3V0
U1	IO268PDB6V4
U2	IO264NDB6V3
U3	IO264PDB6V3
U4	IO258PDB6V3
U5	IO258NDB6V3
U6	IO257PPB6V2
U7	IO261PPB6V3

896-Pin FBGA	
Pin Number	A3PE3000L Function
U8	IO265NDB6V3
U9	IO263NDB6V3
U10	V_{CCI}B6
U11	V_{CC}
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U18	GND
U19	GND
U20	V_{CC}
U21	V_{CCI}B3
U22	IO120PDB3V0
U23	IO128PDB3V1
U24	IO124PDB3V1
U25	IO124NDB3V1
U26	IO126PDB3V1
U27	IO129PDB3V1
U28	IO127PDB3V1
U29	IO125PDB3V1
U30	IO121NDB3V0
V1	IO268NDB6V4
V2	IO262PDB6V3
V3	IO260PDB6V3
V4	IO252PDB6V2
V5	IO257NPB6V2
V6	IO261NPB6V3
V7	IO255PDB6V2
V8	IO259PDB6V3
V9	IO259NDB6V3
V10	V_{CCI}B6
V11	V_{CC}
V12	GND
V13	GND

896-Pin FBGA	
Pin Number	A3PE3000L Function
V14	GND
V15	GND
V16	GND
V17	GND
V18	GND
V19	GND
V20	V_{CC}
V21	V_{CCI}B3
V22	IO120NDB3V0
V23	IO128NDB3V1
V24	IO132PDB3V2
V25	IO130PPB3V2
V26	IO126NDB3V1
V27	IO129NDB3V1
V28	IO127NDB3V1
V29	IO125NDB3V1
V30	IO123PDB3V1
W1	IO266NDB6V4
W2	IO262NDB6V3
W3	IO260NDB6V3
W4	IO252NDB6V2
W5	IO251NDB6V2
W6	IO251PDB6V2
W7	IO255NDB6V2
W8	IO249PPB6V1
W9	IO253PDB6V2
W10	V_{CCI}B6
W11	V_{CC}
W12	GND
W13	GND
W14	GND
W15	GND
W16	GND
W17	GND
W18	GND
W19	GND

896-Pin FBGA	
Pin Number	A3PE3000L Function
W20	V_{CC}
W21	V_{CCI}B3
W22	IO134PDB3V2
W23	IO138PDB3V3
W24	IO132NDB3V2
W25	IO136NPB3V2
W26	IO130NPB3V2
W27	IO141PDB3V3
W28	IO135PDB3V2
W29	IO131PDB3V2
W30	IO123NDB3V1
Y1	IO266PDB6V4
Y2	IO250PDB6V2
Y3	IO250NDB6V2
Y4	IO246PDB6V1
Y5	IO247NDB6V1
Y6	IO247PDB6V1
Y7	IO249NPB6V1
Y8	IO245PDB6V1
Y9	IO253NDB6V2
Y10	GEB0/IO235NPB6V0
Y11	V_{CC}
Y12	V_{CC}
Y13	V_{CC}
Y14	V_{CC}
Y15	V_{CC}
Y16	V_{CC}
Y17	V_{CC}
Y18	V_{CC}
Y19	V_{CC}
Y20	V_{CC}
Y21	IO142PPB3V3
Y22	IO134NDB3V2
Y23	IO138NDB3V3
Y24	IO140NDB3V3
Y25	IO140PDB3V3

896-Pin FBGA	
Pin Number	A3PE3000L Function
Y26	IO136PPB3V2
Y27	IO141NDB3V3
Y28	IO135NDB3V2
Y29	IO131NDB3V2
Y30	IO133PDB3V2

Part Number and Revision Date

Part Number 51700100-003-1
Revised April 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (v1.1)	Page
v1.0 (January 2008)	The "324-Pin FBGA" package diagram was replaced.	3-29

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advance," "Preliminary," and "Production." The definitions of these categories are as follows:

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Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

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51700100-005-9/2.09