

2SK3494

N-channel enhancement mode MOSFET

■ Features

- Low on-resistance, low Q_g
- High avalanche resistance

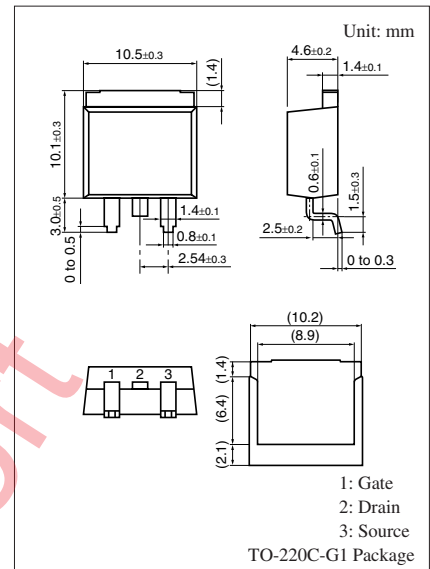
■ Applications

- For PDP
- For high-speed switching

■ Absolute Maximum Ratings $T_C = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain-source surrender voltage	V_{DSS}	250	V
Gate-source surrender voltage	V_{GSS}	± 30	V
Drain current	I_D	20	A
Peak drain current	I_{DP}	80	A
Avalanche energy capability*	EAS	657	mJ
Power dissipation	P_D	50	W
		$T_a = 25^\circ\text{C}$	1.4
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to $+150$	$^\circ\text{C}$

Note) *: $L = 2.79$ mH, $I_L = 20$ A, $V_{DD} = 50$ V, 1 pulse, $T_a = 25^\circ\text{C}$



Marking Symbol: K3494

■ Electrical Characteristics $T_C = 25^\circ\text{C} \pm 3^\circ\text{C}$

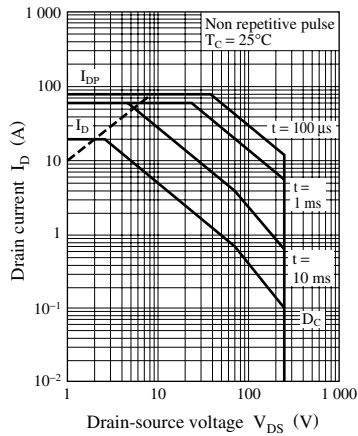
Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
Drain-source surrender voltage	V_{DSS}	$I_D = 1$ mA, $V_{GS} = 0$	250			V	
Gate threshold voltage	V_{th}	$V_{DS} = 10$ V, $I_D = 1$ mA	2.0		4.0	V	
Drain-source cutoff current	I_{DSS}	$V_{DS} = 200$ V, $V_{GS} = 0$			10	μA	
Gate-source cutoff current	I_{GSS}	$V_{GS} = \pm 30$ V, $V_{DS} = 0$			± 1	μA	
Drain-source ON resistance	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 10$ A		82	105	m Ω	
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 10$ V, $I_D = 10$ A	7	14		S	
Short-circuit forward transfer capacitance (Common-source)	C_{iss}	$V_{DS} = 25$ V, $V_{GS} = 0$, $f = 1$ MHz		2450		pF	
Short-circuit output capacitance (Common-source)	C_{oss}				356		pF
Reverse transfer capacitance (Common-source)	C_{rss}				40		pF
Turn-on delay time	$t_{d(on)}$	$V_{DD} \approx 100$ V, $I_D = 10$ A $R_L = 10$ Ω , $V_{GS} = 10$ V		36		ns	
Rise time	T_r			20		ns	
Turn-off delay time	$t_{d(off)}$			184		ns	
Fall time	t_f			29		ns	

■ Electrical Characteristics (continued) $T_C = 25^\circ\text{C} \pm 3^\circ\text{C}$

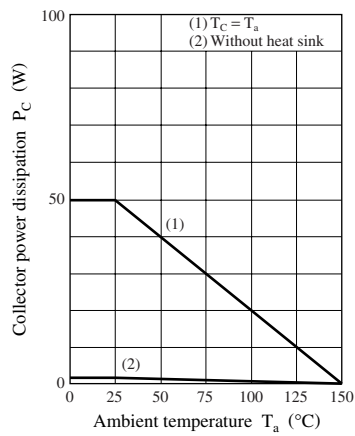
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Diode forward voltage	V_{DSF}	$I_{DR} = 20\text{ A}, V_{GS} = 0$			-1.5	V
Reverse recovery time	t_{rr}	$L = 230\ \mu\text{H}, V_{DD} = 100\text{ V}$		142		ns
Reverse recovery charge	Q_{rr}	$I_{DR} = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		668		nC
Gate charge load	Q_g	$V_{DD} = 100\text{ V}, I_D = 10\text{ A}$		41		nC
Gate-source charge	Q_{gs}	$V_{GS} = 10\text{ V}$		8.4		nC
Gate-drain charge	Q_{gd}			14		nC
Thermal resistance (ch-c)	$R_{th(ch-c)}$				2.5	$^\circ\text{C}/\text{W}$
Thermal resistance (ch-a)	$R_{th(ch-a)}$				89.2	$^\circ\text{C}/\text{W}$

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

Safe operation area



$P_C - T_a$



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