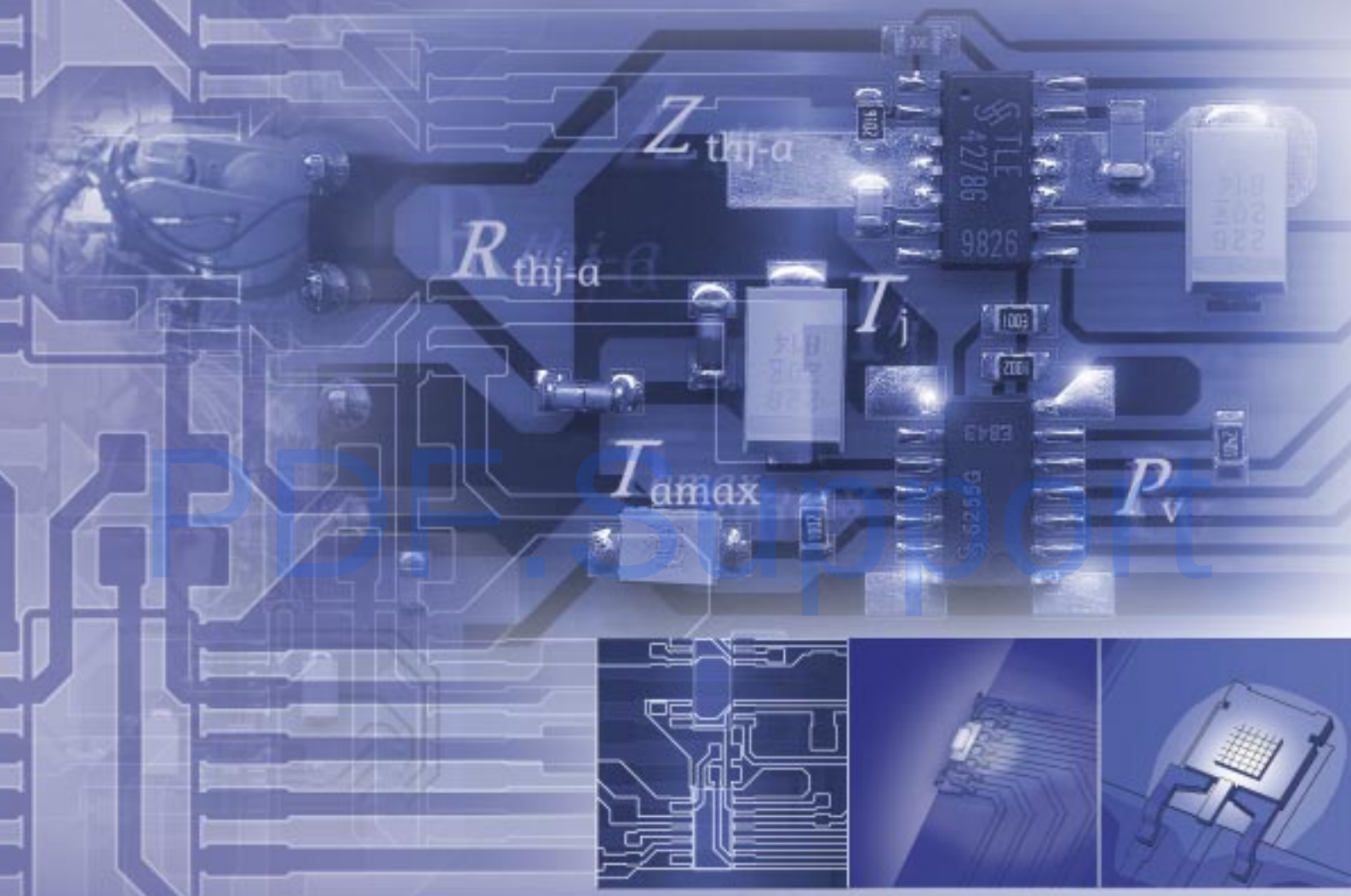
Thermal Resistance Theory and Practice



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SMD Packages

Infineon technologies

Never stop thinking

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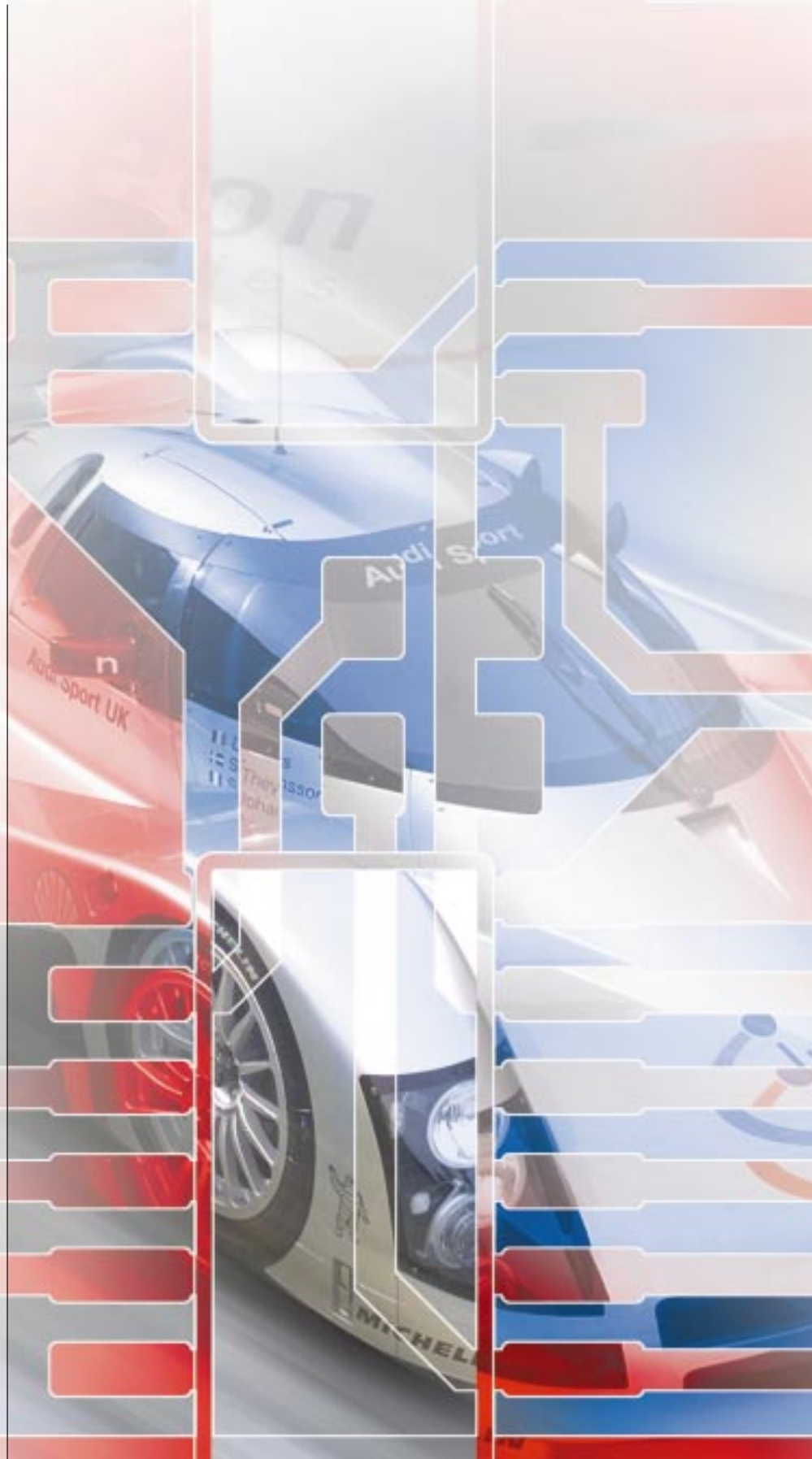

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Introduction

Power-SMD applications or what's the size of the heat sink ?

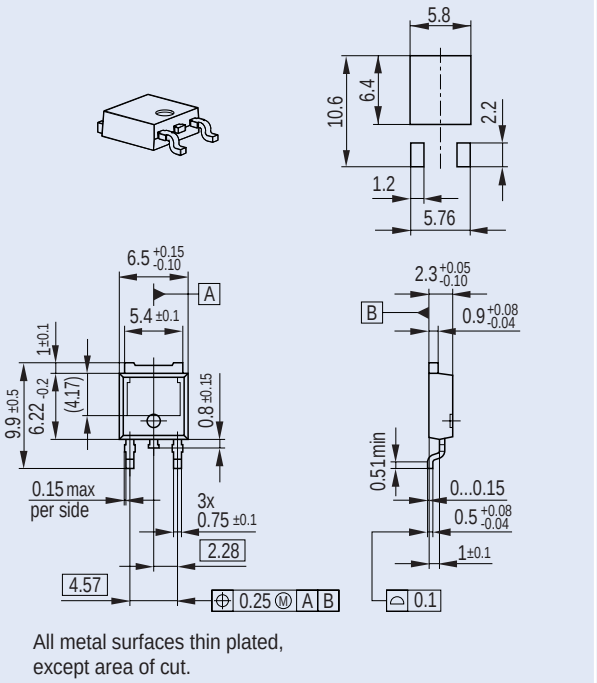
More and more frequently, modern SMD-component users (Surface Mounted Devices) ask the question, "What's the size of the heat sink ?"
The reason: The trend from through-hole packages to low-cost SMD-applications is marked by the improvement of chip technologies.
„Silicon instead of heat sink" is therefore possible in many cases. The printed circuit board (PCB) itself becomes the heat sink. As many applications today use PCBs assembled with SMD-technology, the emphasis is on Power-ICs in SMD packages mounted on single-sided PCBs laminated on one side.
Pricing pressure demands simple processes and lowest-cost solutions. This report describes a solution.

SMD-Package Properties for Power Applications

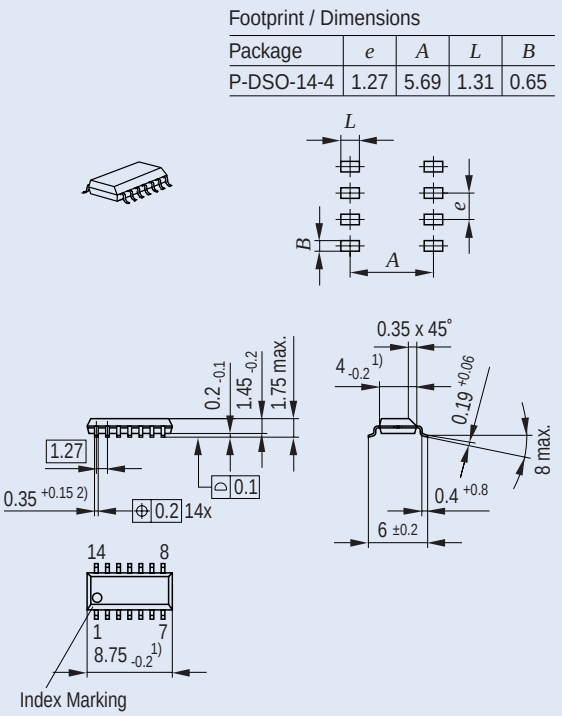
There are two basic groups of packages:

Heat Sink packages are the first group.The heat sink (chip carrier - lead frame) is soldered directly to the PCB. The thermal resistance of this packages between chip and heat sink is called $R_{thj\text{-}c}$ (junction-case) and has low values.

Thermal Enhanced Leadframes constitute the second group of packages. Metal bridges are connected between the chip carrier (lead frame) and the pins. From the outside, this package looks identical to standard components because the plastic molding compound conceals these details. **Figure 1** shows both types of packages with the examples P-TO252-3-1 (D-Pack) and P-DSO-14-4 (3 center pins each per side of the cooling path). The internal structure is described in more detail in this report and can be seen in **Figure 11**.



P-TO252-3-1



P-DSO-14-4

Dimensions in mm

Figure 1 **Heat Sink - vs. Thermal Enhanced Package Types**

Using a printed circuit board as a heat sink ? How do I calculate that ? How big does my heat sink need to be ? Which size do we need ?

In earlier fabrications, a solid heat sink was either screwed or clamped to the power package. It was easy to calculate the thermal resistance from the geometry of the heat sink.
In SMD-technology, this calculation is much more difficult because the heat path must be evaluated: chip (junction) - lead frame - case or pin - footprint - PCB materials (basic material, thickness of the laminate) - PCB volume - surroundings.
As the layout of the PCB is a main contributor to the result, a new technique must be applied. The Appendix proivdes thermal data for all packages listed in **Table 1**.

Let us start with some theoretical considerations:

Static Properties

To facilitate discussion of the static properties of a Power IC (PIC), the internal structure of a PIC and its method of mounting on a PCB or heat sink is illustrated in **Figure 2**. The PIC consists of a chip mounted on a chip carrier or lead frame, and held by solder or bonding adhesive. The lead frame consists of a high-conductivity material such as copper, and can have a

Package	Heat Sink / Pin
P-DSO-8-1	–
P-DSO-14-4	Pin 3-5; 10-12
P-DSO-16-1	–
P-DSO-20-1	–
P-DSO-20-6	Pin 4-7; 14-17
P-DSO-24-3	Pin 5-8; 17-20
P-DSO-28-6	Pin 6-9; 20-23
P-DSO-20-10	Tab
P-DSO-36-10	Tab
SCT-595-5-1	Pin 2; 5
SOT-223-4-2	Tab or Pin 4
P-TO252-3-1 (D-Pack)	Tab
P-TO263-5-1	Tab

Table 1 **The Most Important SMD-Packages**

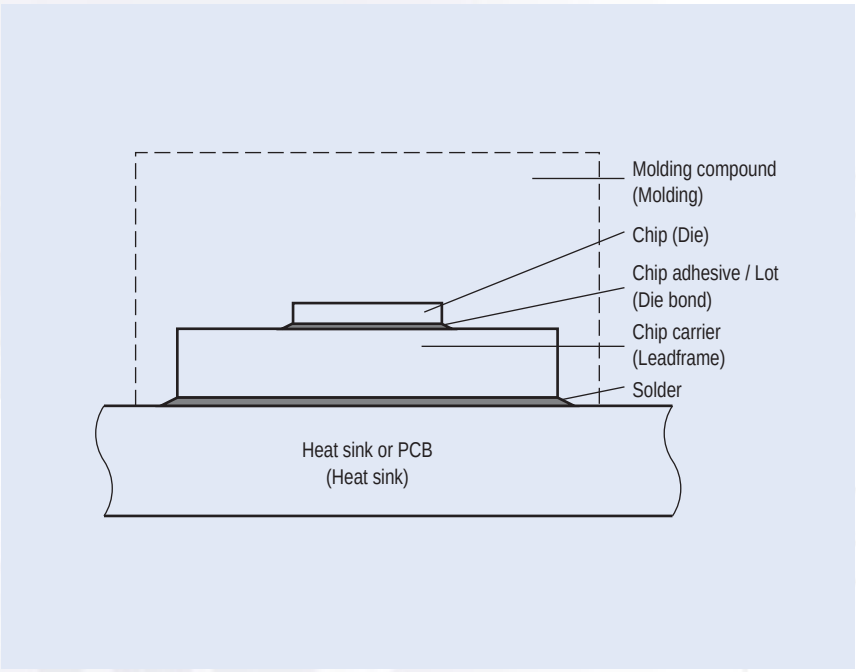


Figure 2 **Internal Structure of a PIC and Method of Mounting on a Heat Sink**

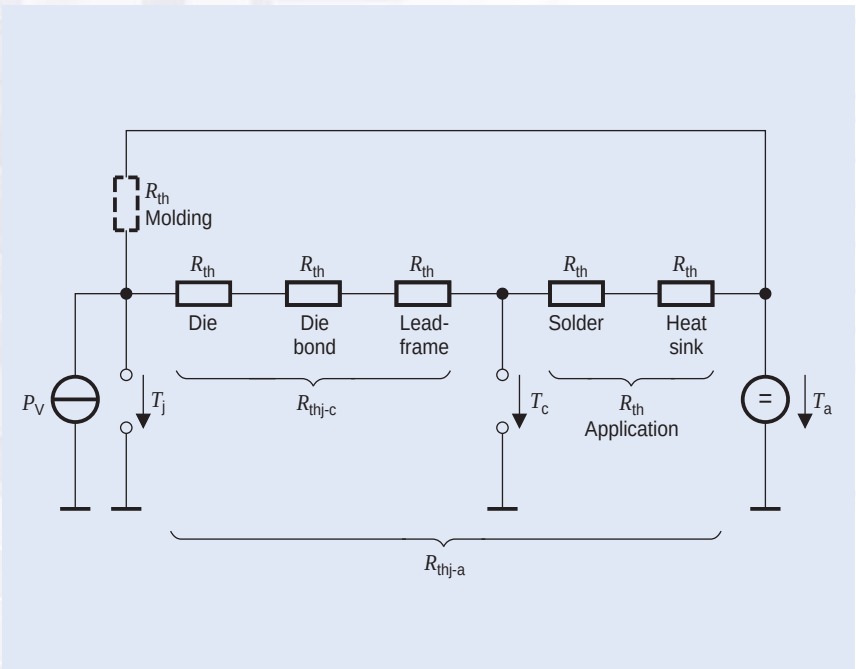


Figure 3 **Static Equivalent Circuit for the Structure shown in Figure 2**

thickness of several millimeters. The associated static equivalent circuit is shown in **Figure 3**. The following analogies with electrical quantities have been used:

- The power dissipation P_V occurring close to the chip surface is symbolized by a current source.
- The thermal resistances are represented by ohmic resistors. The "resistance" network is essentially a serial connection to the ambient temperature. As a first approximation, the parallel-connected thermal resistance of the molding (broken lines) can be neglected in power packages.
- The ambient temperature is represented by a voltage source.

In accordance with the analogy, the thermal current $P_V = Q/t$ can now be calculated from the "thermic Ohm's law" $V = I \bullet R$ as $T_j - T_a = P_V \bullet R_{thj-a}$.

For the purpose of discussing the application as a whole, the function $P_V = f(T_a)$ is of practical interest. One obtains:
$P_V = - T_a / R_{thj-a} + T_j / R_{thj-a}$.
This is a descending straight line of gradient $-1 / R_{thj-a}$ with its zero at T_j.

In **Figure 4**, this function is shown for the P-DSO-14-4 Package (Thermal Enhanced Power Package) mounted on the standard application board. From this function, the user can derive the permissible power dissipation directly for any ambient temperature. At T_a = 85 °C, for example, the permissible dissipation is approxi-mately 0.7 W. The exact value can be calculated from the equation $P_V = (T_j - T_{amax}) / R_{thj\text{-}a}$ = 65 K / 92 K/W = 0.7 W.
It should be noted that in the data sheets of the PICs the power dissipation is given as a function of the package (case) temperature T_C, because the application-specific thermal resistances are not known to the manufacturer. This function, like the previous one, is a descending straight line. The slope now has the value $1 / R_{thj\text{-}c}$. The zero remains at T_j. As an example, this function is presented in **Figure 5** for the P-TO252-3-1 Package.
The new P-TO252-3-1 package has a thermal resistance of max. 4 K/W and is unique in the small size of its base area when compared with packages of equivalent performance (PCB board area). At approximately 30 °C, the permissible power dissipation is 30 W. Higher power dissipation is prevented by intervention of the chip-internal current limiters. For this reason, the value for power dissipation at lower temperatures remains constant.

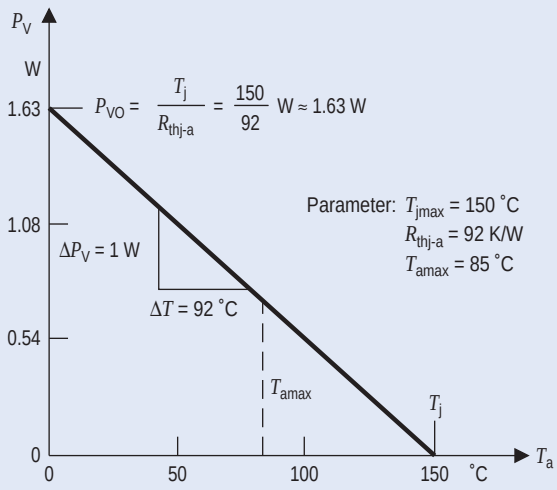


Figure 4 **Permissible Power Dissipation of the P-DSO-14-4 Package Mounted on a PCB with 300 mm² Cooling Area, as a Function of Ambient Temperature**

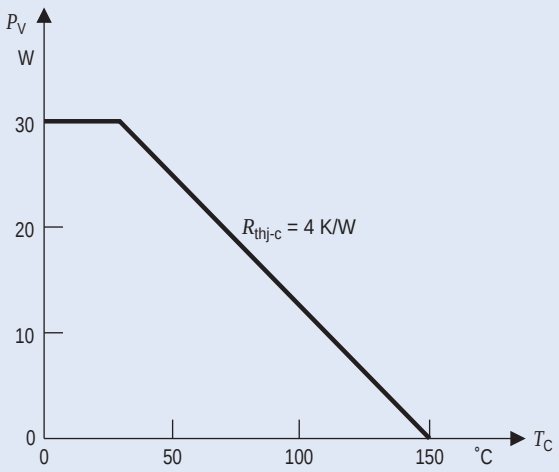


Figure 5 **Permissible Power Dissipation of the P-TO252-3-1 as a Function of the Package (Case) Temperature**

Dynamic Properties

As mentioned earlier, the thermal behavior of PICs changes when dynamic phenomena are considered (pulse power operation). This behavior can be described in terms of thermal capacity C_{th}, which is directly proportional to the relevant volume V (in cm³), to the density ρ (in g/cm³) of the material and to a proportionality factor of the specific heat c in Ws/g • K.
The applicable equation is:
$C_{th} = c \bullet \rho \bullet V = m \bullet c$
This means: The thermal capacity of a body of mass $m = \rho \bullet V$ corresponds to the quantity of heat needed to heat the body by 1 °C.
To calculate the temperature change ΔT it is necessary to use the quantity-of-charge equation for a capacitance C.
The equation is:
$V \bullet C = I \bullet t = Q$
By analogy, the quantity-of-heat equation is:
$\Delta T \bullet C_{th} = P \bullet t = Q$
This means: Just as the current $I = Q/t$ represents a transport of charge per unit of time, the power dissipation P represents the transport of thermal energy per unit of time. Consequently:

$$\Delta T = \frac{P \bullet t}{C_{th}}$$

The equivalent circuit of the P-TO263-7-3 power package, with the thermal capacities added, is shown in **Figure 6**. The thermal capacities calculated from the material and the volume are shown in parallel with the thermal resistances.
When calculating the components of a network it is necessary to know the thickness d, the cross-sectional area A and the thermal conductivity L in W/m • K, in order to obtain the appropriate thermal resistance R_{th}. The formula is:

$$R_{th} = \frac{d}{L \bullet A} \left[\frac{K}{W}\right]$$

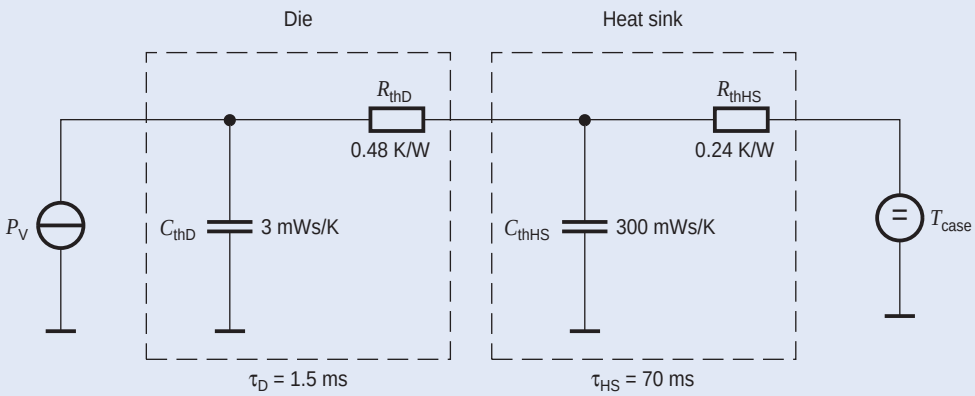


Figure 6 **Thermal Equivalent Circuit of the P-TO263-7-3 Package (Simplified)**

Thermal Resistance - Theory and Practice

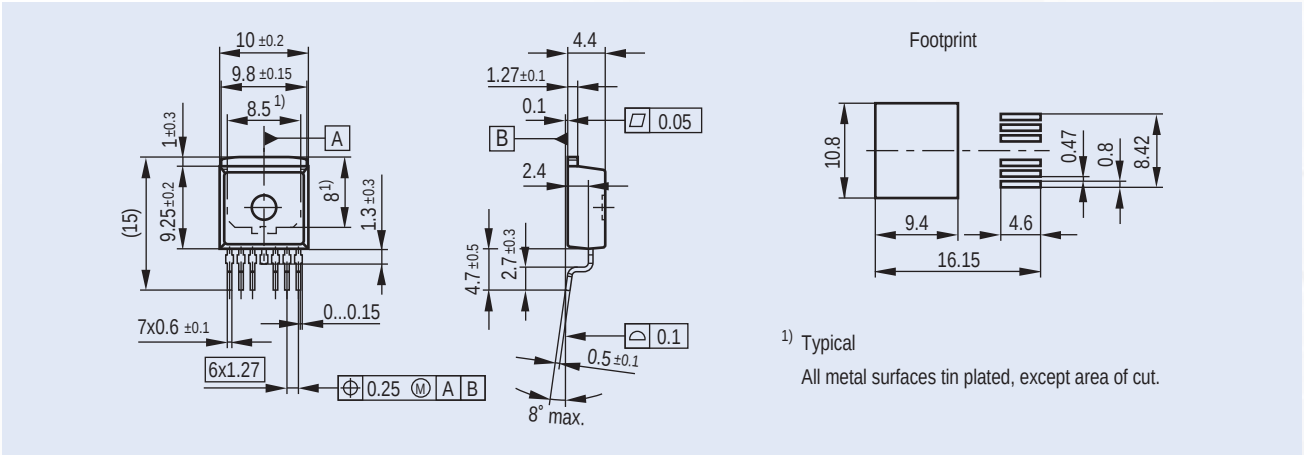


Figure 7 Outline Drawing of the P-TO263-7-3 Power Package

To calculate the thermal capacity C_{th}, it is necessary to know the volume $V = d \cdot A$, the specific weight ρ in g/cm3 and the specific thermal capacity c in Ws/g • K.

The thermal capacity C_{th} is calculated from:
$C_{th} = m \cdot c$ (Ws/T).
The package dimensions are shown in **Figure 7**.

Table 2 lists all the important parametric data of the P-TO263-7-3 package.

Parameters for the Chip	Symbol	Value	Dimension
Area	A_D	5	mm²
Thickness	d_D	360	µm
Thermal conductivity of silicon	L_{Si}	150	W/m • K
Thermal resistance of chip	R_{thD}	0.48	K/W
Specific weight of silicon	ρ_{Si}	2.33	g/cm³
Mass of chip	m_D	4.2	mg
Spec, thermal capacity of Si	c_{Si}	approx. 0.7	Ws/g • K
Thermal capacity of chip	C_{thD}	approx. 3	mWs/K
Thermal time constant of chip	τ_D	approx. 1.5	ms
Parameters for the Heat Slug	**Symbol**	**Value**	**Dimension**
Area (effective area of 64 mm²)	A_{HS}	14	mm²
Thickness	d_{HS}	1.27	mm
Thermal conductivity of cooper	L_{Cu}	384	W/m • K
Thermal resistance of heat slug	R_{thHS}	0.24	K/W
Specific weight of cooper	ρ_{Cu}	8.93	g/cm³
Mass of heat slug	m_{HS}	0.8	g
Spec, thermal capacity of Cu	c_{Cu}	0.385	Ws/g • K
Thermal capacity of heat slug	C_{thHS}	310	mWs/K
Thermal time constant of heat slug	τ_{HS}	70	ms

Table 2 Parametric Data of the P-TO263-7-3

The die bond and molding components have been omitted from this discussion because they do not significantly influence the calculation of $R_{thj\text{-}c}$.
For reference, these data are listed here:

- R_{thDB} = 0.01 to 0.1 K/W;
- C_{thDB} = 0.1 to 0.5 mWs/K;
- τ_{DB} = 1 to 50 ms;
- R_{thM} = 100 K/W;
- C_{thM} = 0.64 Ws/K and
- τ_{M} = 64 s.

(Die Bond = index: DB; molding = index: M)

The time constance of the die bond is smaller than that of the chip by two orders of magnitude and can, thus, be neglected.
The thermal resistance R_{thM} of the molding is even three orders of magnitude bigger than that of the chip and that of the heat slug, and, being in parallel, can be neglected also.
Pulse operation and the associated chip temperature responses also deserve examination.
In accordance with the analogy to electrical systems, the chip temperature response can be viewed like a voltage increase across an RC section which is being fed by a current pulse generator.
The following relationship applies:
$V_{(t)} = R \bullet I \bullet (1 - e^{t/R \cdot C})$
and for the increase in temperature:
$T_{(t)} = R_{th} \bullet P \bullet (1 - e^{t/R_{th} \cdot C_{th}})$

This heating-up and cooling-down process is presented qualitatively in **Figure 8** (valid for t_p >> 2 ms only).
The chip temperature goes up and down between T_{min} and T_{max}. The variation depends on the magnitude of the power pulse and its duty cycle.

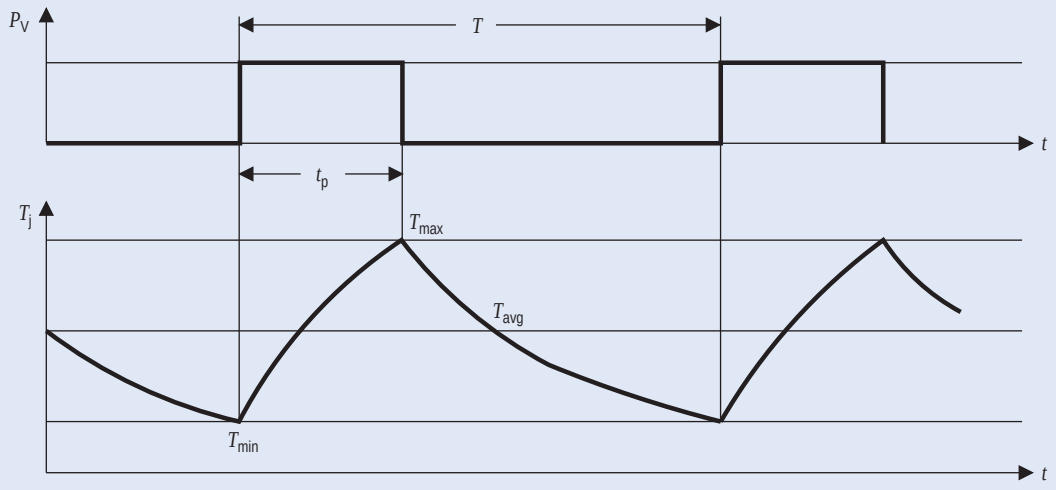


Figure 8 **Chip Temperature T_j vs. Time, for Periodic Pulse Operation**

This junction temperature transients can be represented in the form of a function if the dynamic thermal impedance $Z_{th} = (T_{max} - T_{min}) / P_V$ is shown versus pulse width t_p for different duty cycles (duty cycle = DC = t_p/T) (**Figure 9**).
A special case of this representation is the dynamic thermal impedance in single-pulse operation (DC = 0). **Figure 10** shows the thermal impedance in single-pulse operation for the medium-power package P-DSO-14-4 for three different cooling areas on the PCB.
This function clearly shows the regions of dominance of the various time constants of the chip, the lead frame, and the PCB.
The chip time constant t_D lies in the millisecond range, whereas the lead frame dominates in the range of several 100 ms and the PCB in the 100-second range.

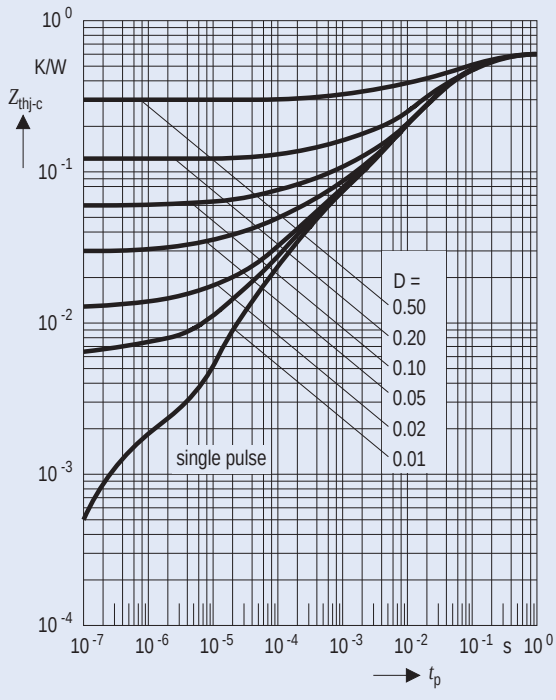


Figure 9 **Dynamic Thermal Impedance Z_{thj-c} of a P-TO263-7-3 Package**

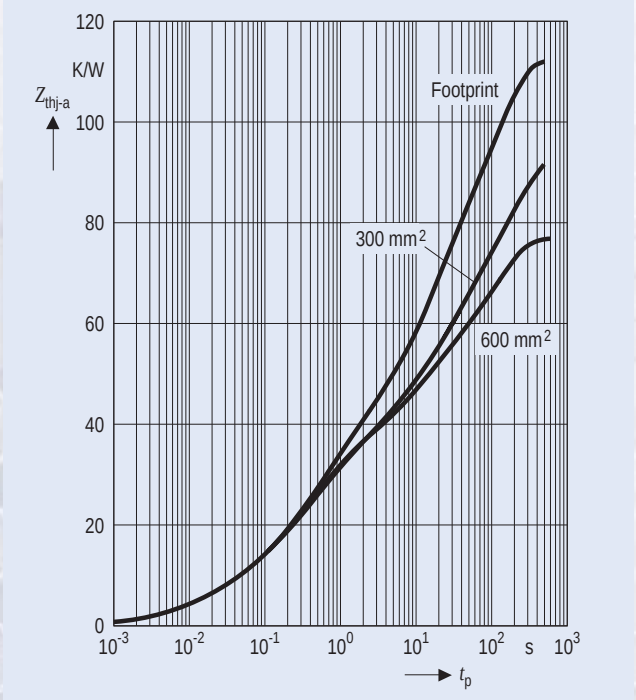
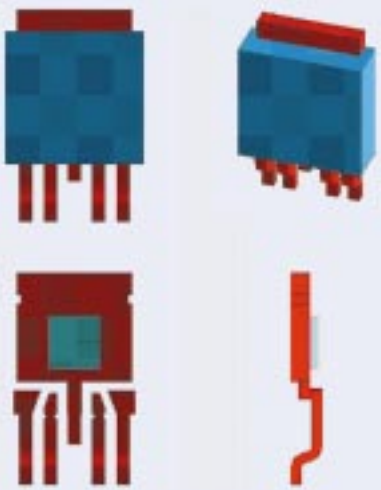


Figure 10 **Thermal Impedance of the P-DSO-14-4 Package for Single-Pulse Operation**

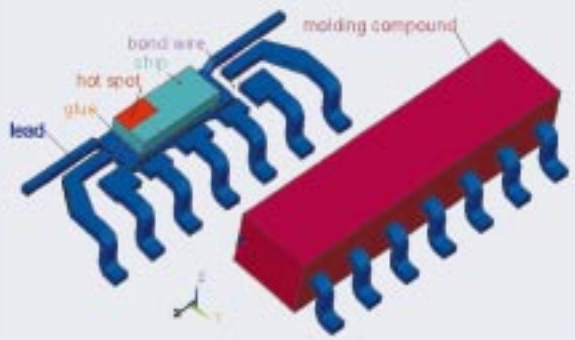
Finite Element Method (FEM)

The steps of the Finite Element Method (FEM) are explained below and one example is provided per group.

The geometric data of the package is entered into the FEM model to calculate the thermal resistance. This avoids time-consuming measurements. **Figure 11** shows an implemented model.



P-TO252-3-1

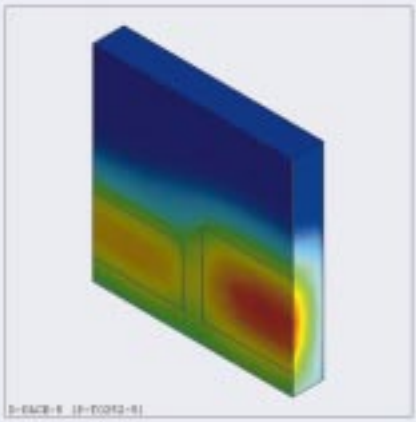


P-DSO-14-4

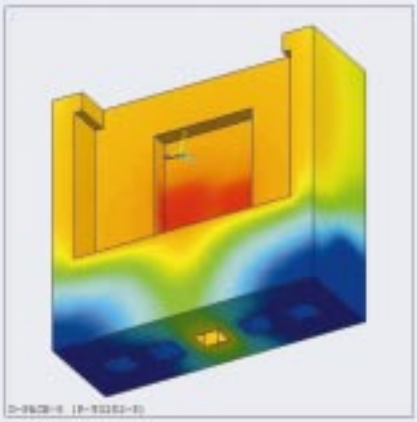
Figure 11 **FEM Model of Heat Sink and Thermal Enhanced Package**

Thermal Resistance - Theory and Practice

The temperatures of the individual components (chip, die-pad, molding compound, and leadframe) can be viewed individually or in combination (**Figure 12**).

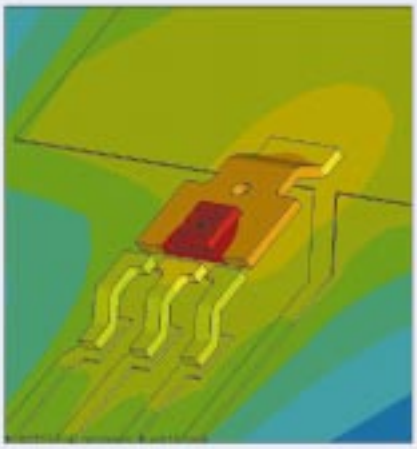


Chip with two active areas (dice only)

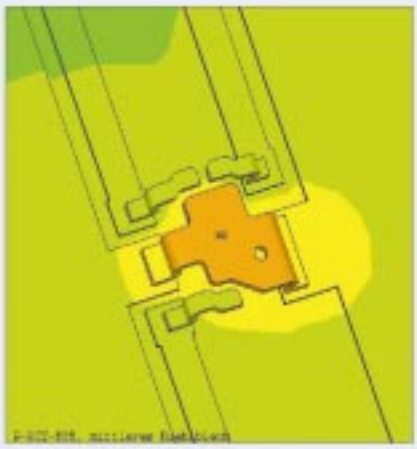


Mold compound without cooling tab,chip and lead frame

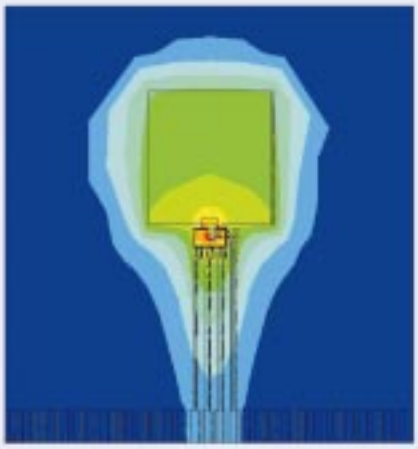
P-TO252-3-1 without mold compound with P_V = 3 W for determining the $R_{thj\text{-}c}$



Chip and lead frame of the SOT223-4-2 package on a PCB with heat sink



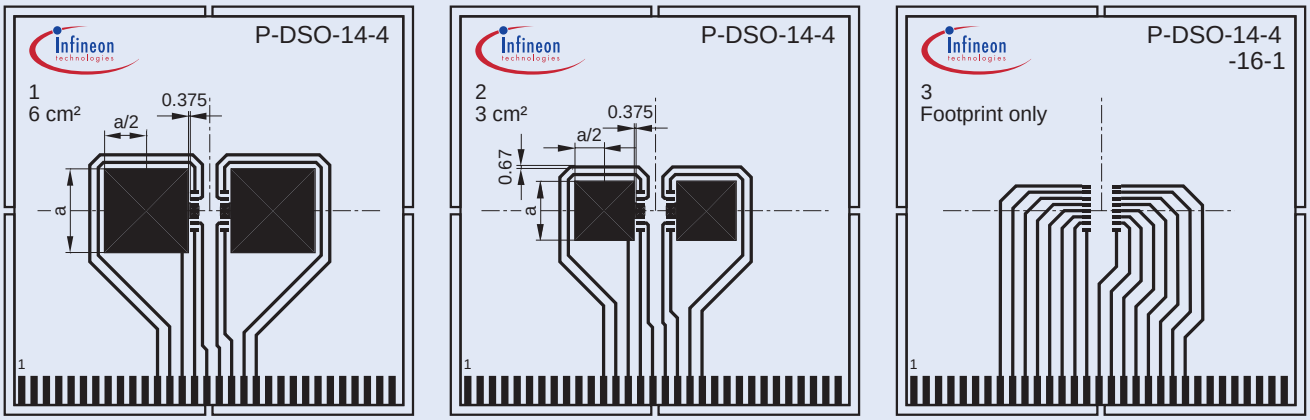
Lead frame of the SCT595-5-1 on a PCB with heat sink



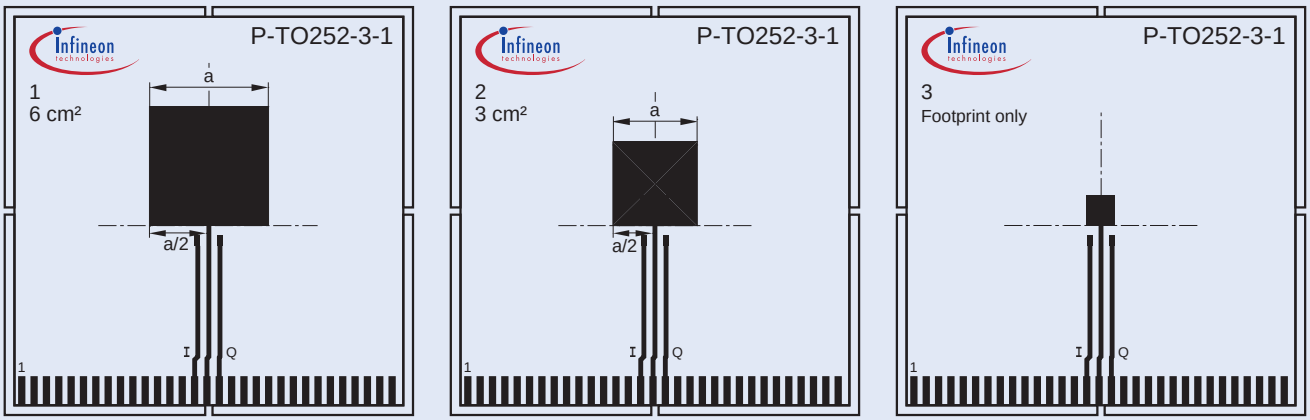
SOT223-4-2 on a PCB with 6 cm² heat sink; $R_{thj\text{-}a}$ ~ 70 K/W is calculated at P_V = 0.5 W

Figure 12 FEM Analysis Possibilities

Three different PCBs have been created for each package model. They differ in the size of the copper laminated area A (heat sink) which is linked to the heat dissipating parts of the case (die-pad in the P-TO252-3-1 or center pins in the P-DSO-14) (**Figure 13**).



Application-Board for R_{th} Measurement R_{th}-P-DSO-14-4 LP 1.0



Application-Board for R_{th} Measurement R_{th}-P-TO252-3-1 LP 1.1

Figure 13 PCB-Layout for FEM-Simulation P-DSO-14-4 and P-TO252-3-1

Determining the Static Heat Resistance

The FEM simulation calculates the thermal static resistance $R_{thj\text{-}a}$ (junction-ambient) and the $R_{thj\text{-}c}$ (junction-case) for packages with enhanced die-pad or $R_{thj\text{-}pin}$ (junction to a defined pin) for thermal enhanced P-DSO packages without die-pad. This value depends only slightly on the active chip area. It is sufficient to simulate just one medium-sized chip (>2 mm²).
If the static thermal resistance $R_{thj\text{-}a}$ is applied versus the PCB heat sink area, a very important function is obtained for the application of the component. By estimating the heat sink area in a real application, the user can easily determine the expected $R_{thj\text{-}a}$, especially as the simulated values are calculated in still air. Therefore, they represent the "worst case". In real applications the values for the heat resistance are much lower. At an air stream of 500 lin ft/min (linear feet per minute) the $R_{thj\text{-}a}$ of the P-DSO-14-4 for example is up to 15 % lower (**Figure 15**).

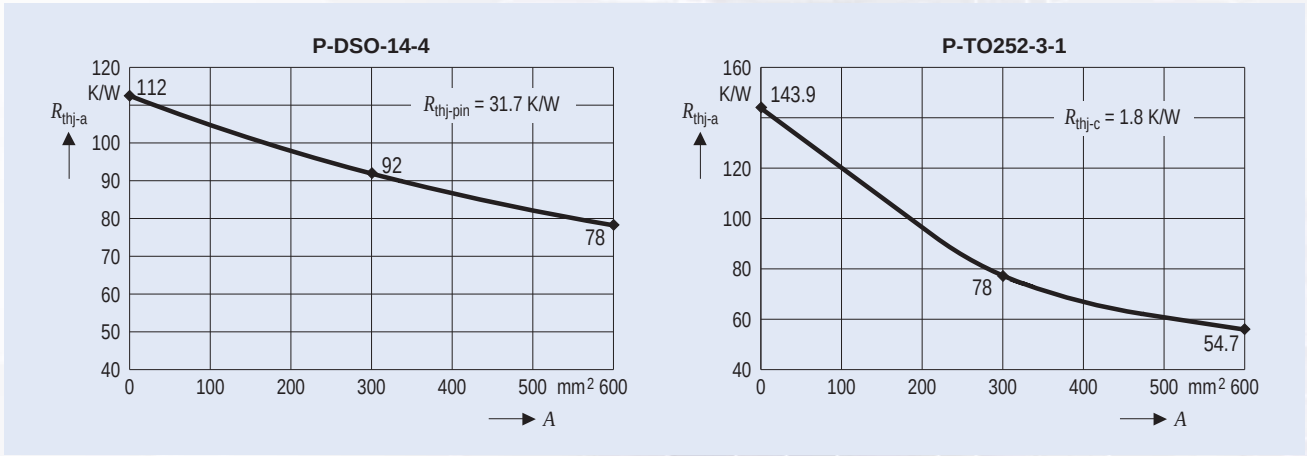


Figure 14 Thermal Resistance Junction to Ambient $R_{thj\text{-}a}$ vs. PCB Heat Sink Area A at zero airflow

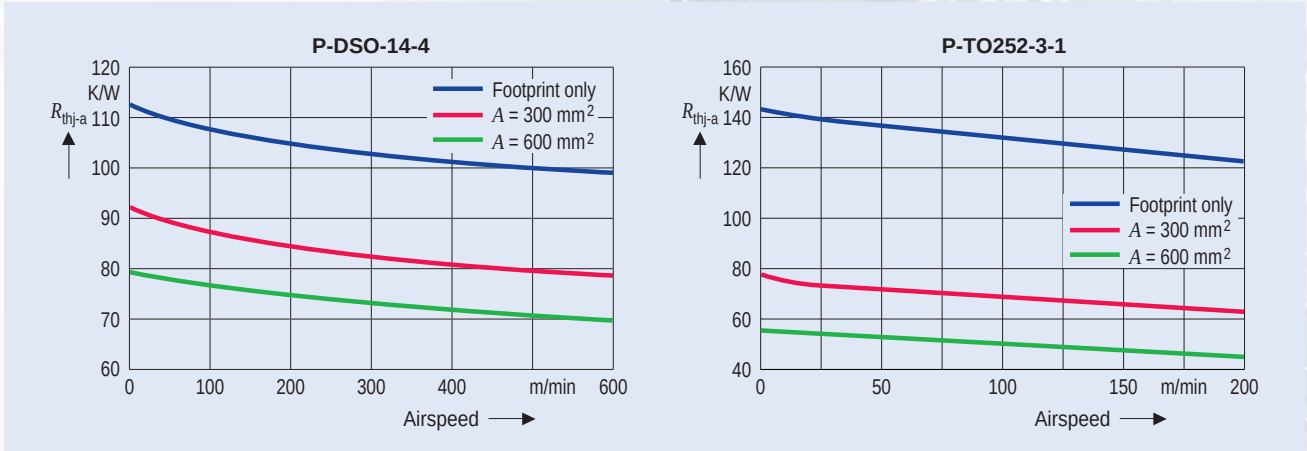


Figure 15 Thermal Resistance Junction to Ambient $R_{thj\text{-}a}$ vs. Airspeed for the P-DSO-14-4 and P-TO252-3-1 Packages

Measuring the $R_{thj\text{-}a}$ in a Real Application:

Using the measurement described below the real thermal resistance can be determined.
To determine the actual $R_{thj\text{-}a}$ the temperature difference between chip temperature T_j and ambient temperature T_a is required. The equation $R_{thj\text{-}a} = \frac{T_j - T_a}{P_V}$ applies.

The power loss P_V and the ambient temperature T_a can be determined easily in a temperature chamber or calculated.

To measure the chip temperature (T_j) requires a little trick:
A temperature sensor is required on the chip which can also be read during operation. In many products a substrate diode can be used at an output (Status, Reset, etc.) to measure the chip temperature.
To do this, the forward voltage V_F of the diode is measured at load independent current as a calibration curve. Due to the characteristic temperature behavior of the forward voltage - it has a negative temperature coefficient of approx. -2 mV/K - the relevant chip temperature can be determined.

The calibration curve is measured in the temperature chamber with airflow. The power loss should be kept as low as possible to ensure the chip temperature remains equal to the ambient temperature.
For the voltage regulator TLE 4269 GM (P-DSO-14-4 Package) a calibration curve (measured at the diode at the reset output, pin 7). RO is illustrated in **Figure 16**.
Figure 17 shows the corresponding measuring circuit.

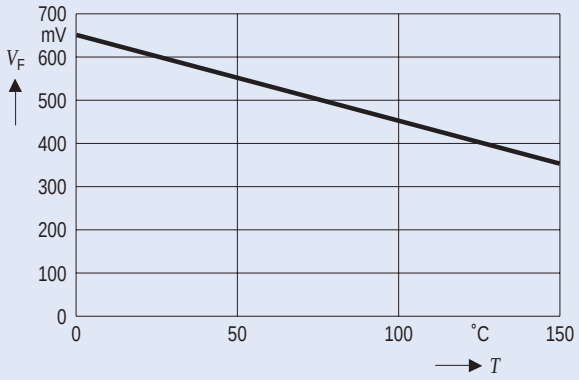


Figure 16 Calibration Curve TLE 4269 GM for I_{RO} = -500 µA (current drawn from Pin 7; RO)

Thermal Resistance - Theory and Practice

The $R_{thj\text{-}a}$ of any application can be determined by measuring the forward voltage of an output with substrate diode during operation (**Figure 17**).

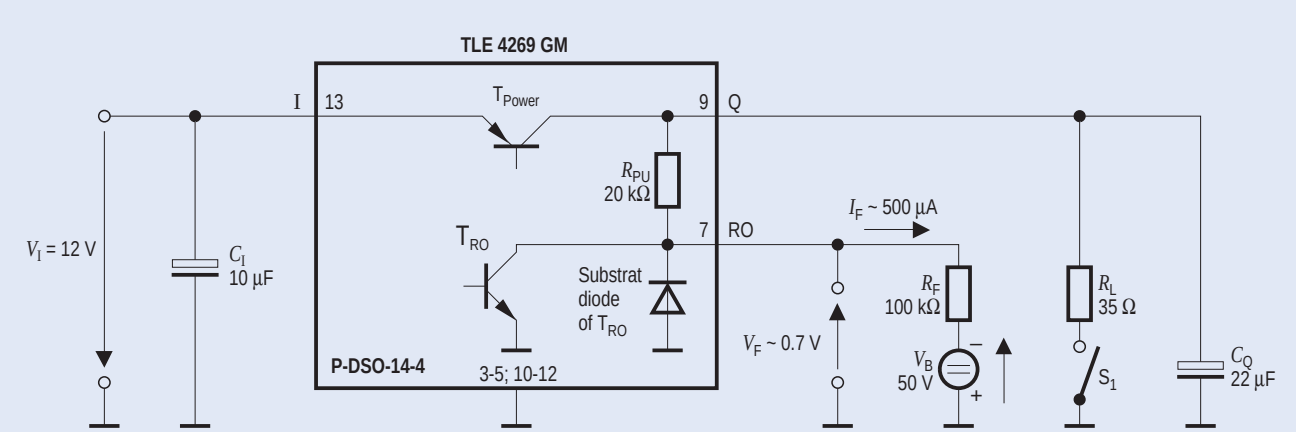
When the switch S1 is closed and the output voltage V_Q = 5 V, the output current is $\frac{5}{35}$ A.

The power loss $P_V = (V_I - V_Q) \bullet I_Q$ in the chip of the voltage regulator is now 1 W. Now, change the ambient temperature T_a and measure the respective forward voltage V_F of the diode. The appropriate T_j for every V_F value can be read from the calibration curve $V_F = f(T_j)$.

The exact heat resistance of the real application is calculated with this values in the formula

$$R_{thj\text{-}a} = \frac{T_j - T_a}{P_V}$$

Parameters such as air flow can be changed without affecting the measuring accuracy.



1. Measurement of function $V_F = f(T_a)$:
   S_1 open; we get I_Q = 0 mA
   and $P_V = V_I * I_I \sim 0$ mW
   $T_a \sim T_j$

2. Measurement of thermal resistance junction to ambient $R_{thj\text{-}a}$:
   S_1 closed; we get $I_Q = V_Q / R_Q$
   and $P_V = (V_I - V_Q) * I_Q \sim 1$ W
   T_j then can be found by measuring V_F at given T_a from function V_F vs. T_a
   then we get $R_{thj\text{-}a} = (T_a - T_j) / 1$ W

P_V = Power losses
T_a = Ambient temperature
T_j = Junction temperature

Figure 17 Measuring Circuit with TLE 4269GM

Determining the Dynamic Heat Resistance

The FEM analysis is used also for dynamic processes.
As described above, the dynamic thermal impedance is defined as the ratio of the temperature difference $\Delta T = T_j - T_a$ (chip temperature - start temperature) after the time t_p to the power loss.
If a transient FEM simulation is performed, it is easy to obtain the graph $Z_{thj\text{-}a} = f(t_p)$ (dynamic thermal impedance as a function of the pulse width t_p).
For the P-TO252-3-1 (D-Pack) and the P-DSO-14-4 the thermal impedances for the above-mentioned PCB configurations are specified (**Figure 18**).
The peak temperatures can be calculated easily from these curves:

– P-TO252-3-1 (D-Pack)
– 3 cm² heat sink
– Power loss P_V = 10 W
– Pulse width t_p = 200 ms
– Ambient temperature T_a = 85 °C.

From the middle curve (**Figure 18**), the $Z_{thj\text{-}a}$ of approximately 3.5 K/W at t_p = 200 ms gives a temperature rise $\Delta T = P_V \times Z_{thj\text{-}a}$ of 35 K and finally a peak temperature T_{jmax} of 85 °C+35 °C = 120 °C.

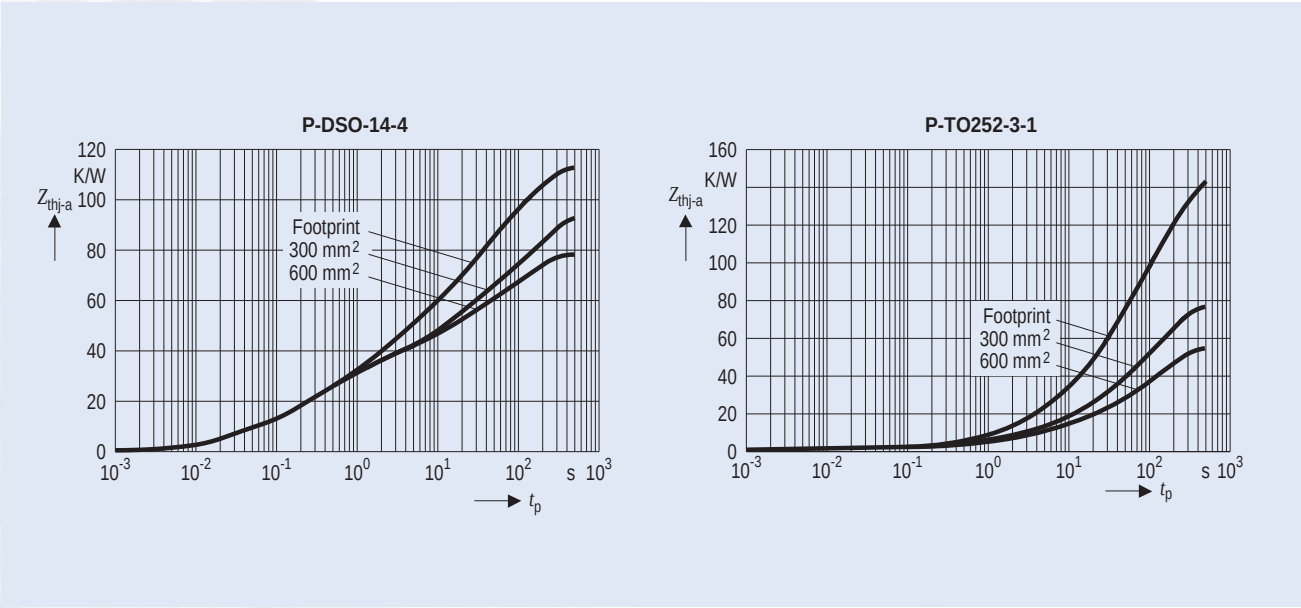


Figure 18 **Thermal Impedance Junction to Ambient $Z_{thj\text{-}a}$ vs. Single Pulse Time t_p**

Summary

For each case listed in **Table 1,** a „**Package and Thermal Information**" data sheet is provided in the appendix.Each data sheet shows the footprint and case dimensions. The various versions of the PCBs used for the simulation are shown. It shows the heat distribution diagrams and the result diagrams of the FEM simulation. The left side shows the diagram of the static thermal resistance $R_{thj\text{-}a}$ depending on the PCB heat sink area A. It includes the related thermal resistance $R_{thj\text{-}c}$ (junction-case) or $R_{thj\text{-}pin}$.

On the right side is the diagram for the dynamic heat resistance $Z_{thj\text{-}a}$, with three graphs for the various PCB heat sinks depending on the single pulse duration t_p. This information is a valuable aid for SMD Power applications. It is intentionally limited to PCBs laminated on one side because it represents the cost optimum. For double sided PCBs or multilayers a simple attempt with conductance cross sections can be made to determine the change in the PCB thermal resistance (compare thermal data sheet of P-DSO-20-10 with P-DSO-36-10 in the appendix).

The PCBs are usually installed in closed plastic cases. The most favorable heat path then usually forms at plug contacts to the cables because a supply wire with an adequate cross section is ideal as a heat conductor.

The future of chip placement requires mechatronic solutions where the PCB can be replaced by chip-connector-supply wire configurations.

Appendix

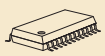

P-DSO-8-1 22


P-DSO-14-4 23

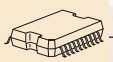

P-DSO-16-1 24


P-DSO-20-1 25


P-DSO-20-6 26


P-DSO-24-3 27

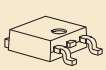

P-DSO-28-6 28

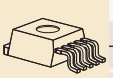

P-DSO-20-10 29


P-DSO-36-10 30


SCT595-5-1 31


SOT223-4-2 32

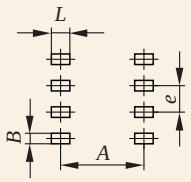

P-TO252-3-1 33


P-TO263-5-1 34

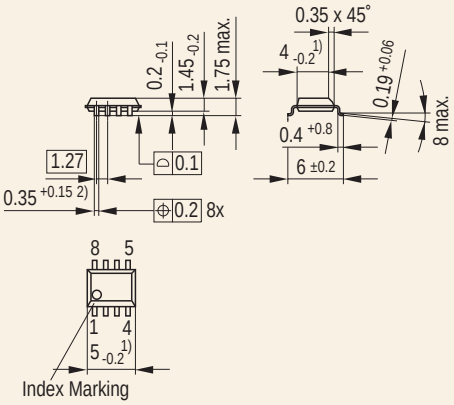
P-DSO-8-1

Footprint/Dimensions

Package	e	A	L	B
P-DSO-8-1	1.27	5.69	1.31	0.65



Reflow soldering

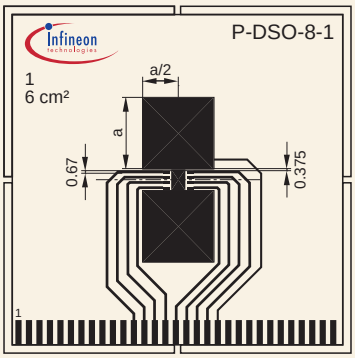


Index Marking

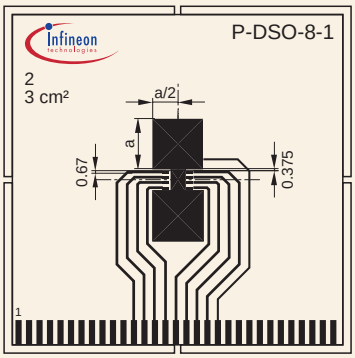
Dimensions in mm

PC-Board

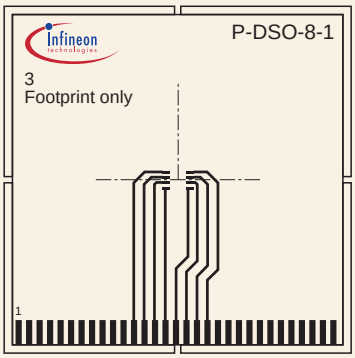
Application-Boards for R_{th} - Measurement



FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 600 mm²; a = 17.32 mm



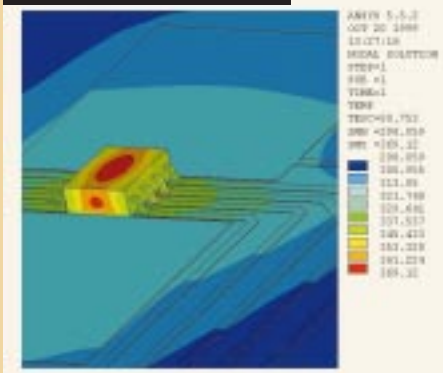
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 300 mm²; a = 12.247 mm



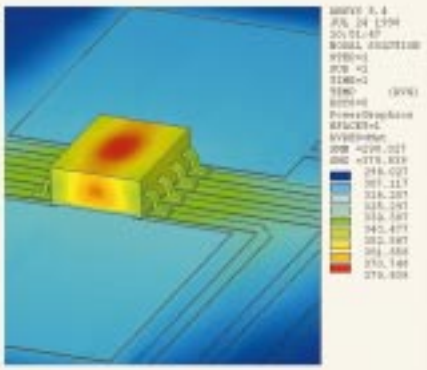
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
Footprint only

Finite Element Method

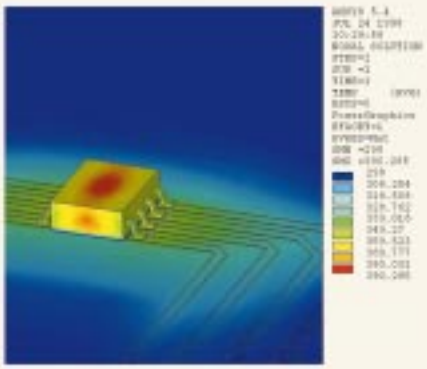
FEM Simulation (chip area ≥ 2 mm²; P_v = 0.5 W; zero airflow)



A = 600 mm²; T_a = 298 K; T_{max} = 369 K



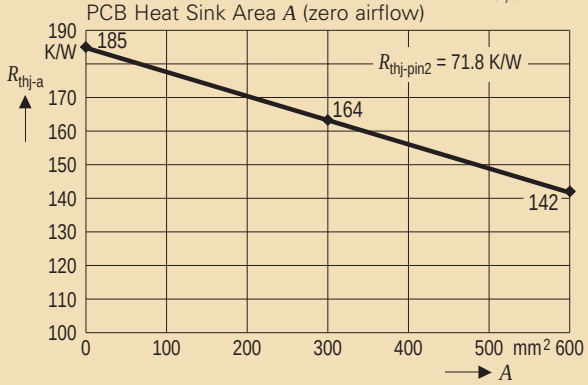
A = 300 mm²; T_a = 298 K; T_{max} = 380 K



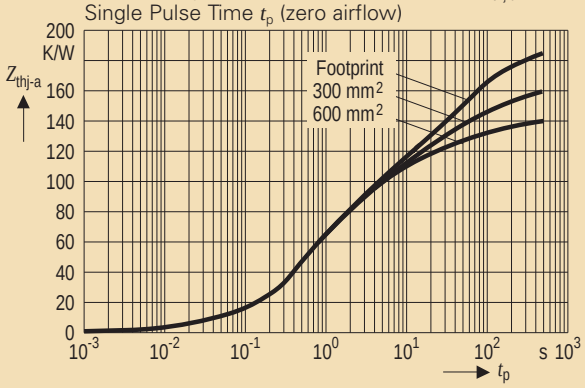
Footprint only; T_a = 298 K; T_{max} = 390 K

Diagrams

Thermal Resistance Junction to Ambient R_{thj-a} vs. PCB Heat Sink Area A (zero airflow)



Thermal Impedance Junction to Ambient Z_{thj-a} vs. Single Pulse Time t_p (zero airflow)

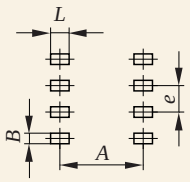


Package and Thermal Information

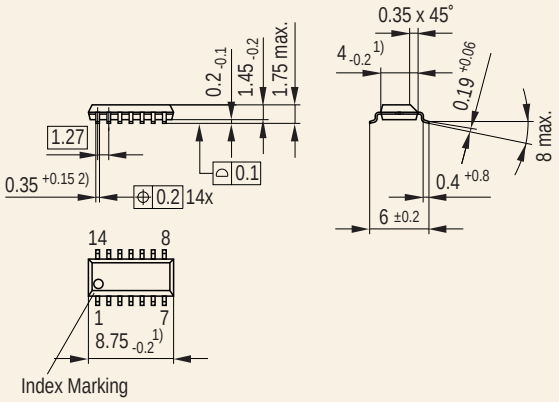
P-DSO-14-4

Footprint/Dimensions

Package	e	A	L	B
P-DSO-14-4	1.27	5.69	1.31	0.65



Reflow soldering

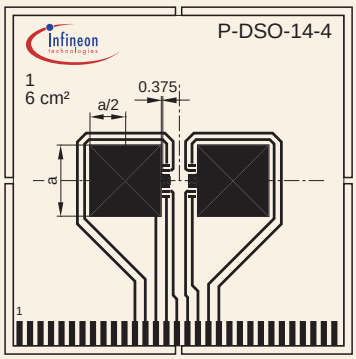


Index Marking

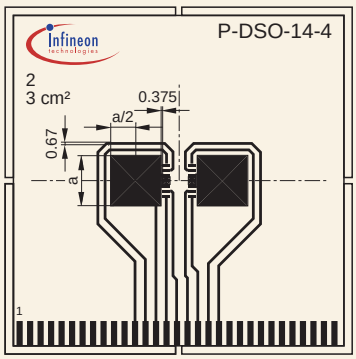
Dimensions in mm

PC-Board

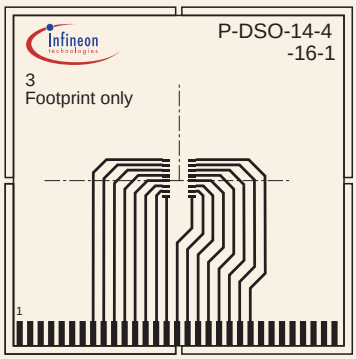
Application-Boards for R_{th} - Measurement



FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 600 mm²; a = 17.32 mm



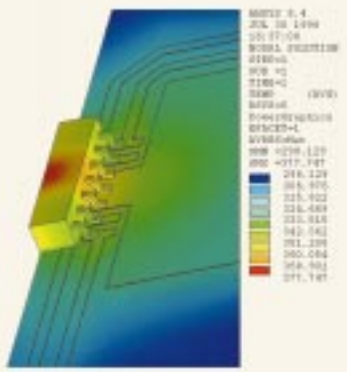
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 300 mm²; a = 12.247 mm



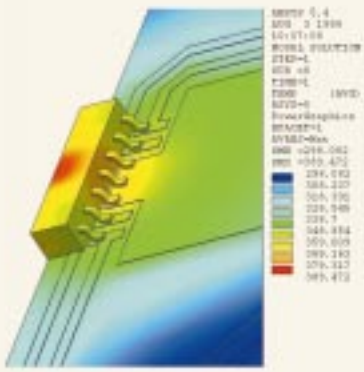
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
Footprint only

Finite Element Method

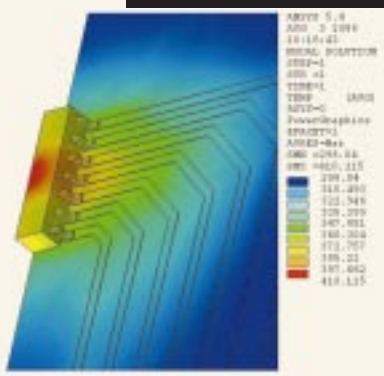
FEM Simulation (chip area ≥ 2 mm²; P_v = 1 W; zero airflow)



A = 600 mm²; T_a = 298.1 K; T_{max} = 377.7 K



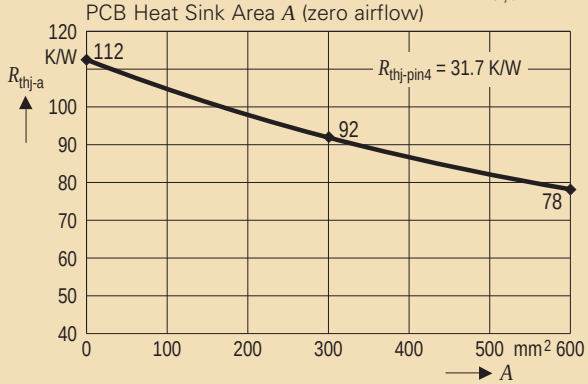
A = 300 mm²; T_a = 298 K; T_{max} = 389.8 K



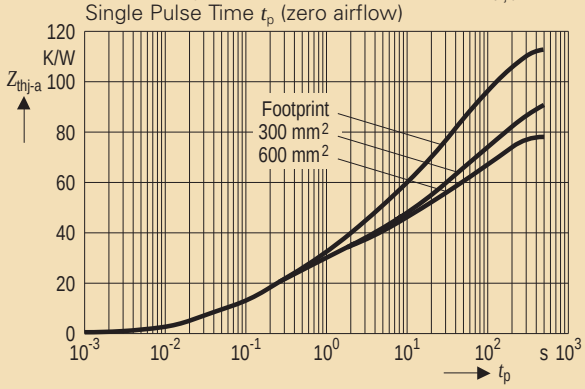
Footprint only; T_a = 298 K; T_{max} = 410.1 K

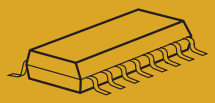
Diagrams

Thermal Resistance Junction to Ambient R_{thj-a} vs.
PCB Heat Sink Area A (zero airflow)



Thermal Impedance Junction to Ambient Z_{thj-a} vs.
Single Pulse Time t_p (zero airflow)

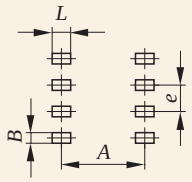




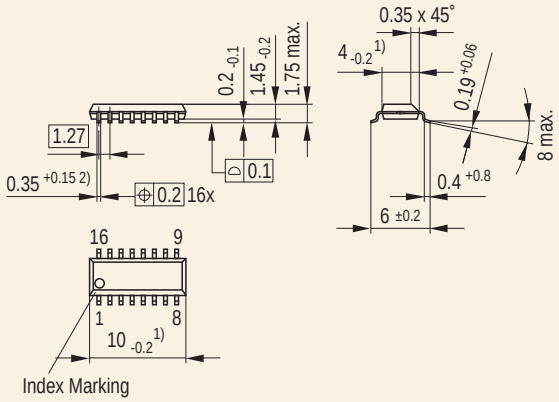
P-DSO-16-1

Footprint/Dimensions

Package	e	A	L	B
P-DSO-16-1	1.27	5.69	1.31	0.65



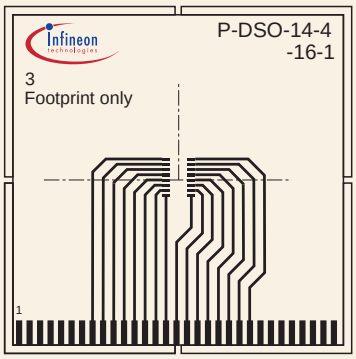
Reflow soldering



Dimensions in mm

PC-Board

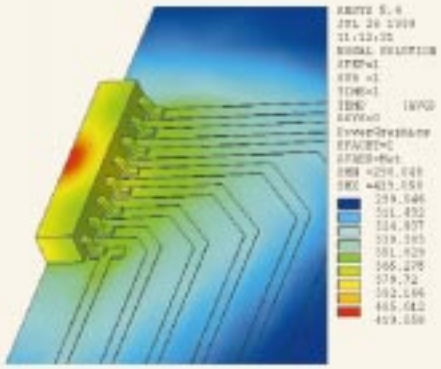
Application-Board for R_{th} - Measurement



FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
Footprint only

Finite Element Method

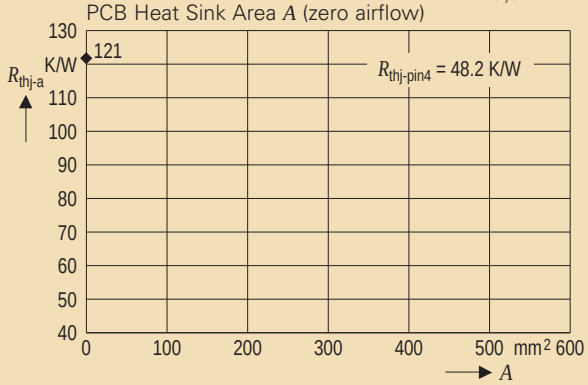
FEM Simulation (chip area ≥ 2 mm²; P_v = 1 W; zero airflow)



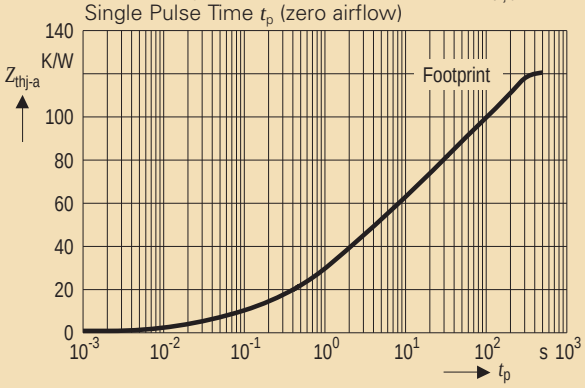
Footprint only; T_a = 298 K; T_{max} = 419.1 K

Diagrams

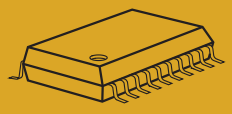
Thermal Resistance Junction to Ambient R_{thj-a} vs.
PCB Heat Sink Area A (zero airflow)



Thermal Impedance Junction to Ambient Z_{thj-a} vs.
Single Pulse Time t_p (zero airflow)



Package and Thermal Information



P-DSO-20-1

Footprint/Dimensions

Package	e	A	L	B
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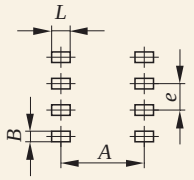
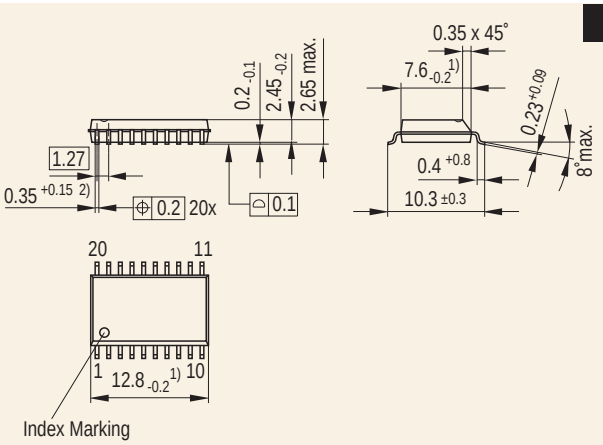
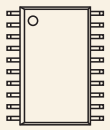


Reflow soldering

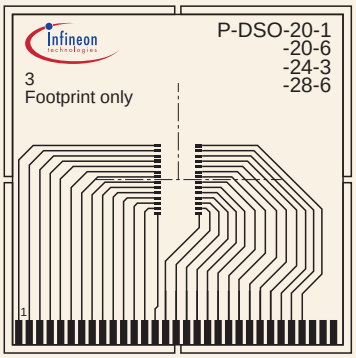




Dimensions in mm

PC-Board

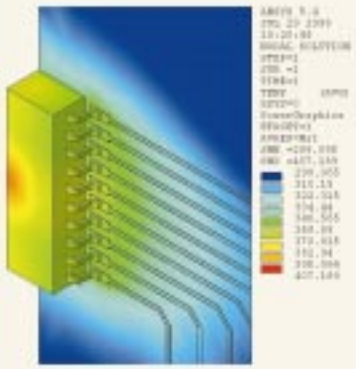
Application-Board for R_{th} - Measurement



FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
Footprint only

Finite Element Method

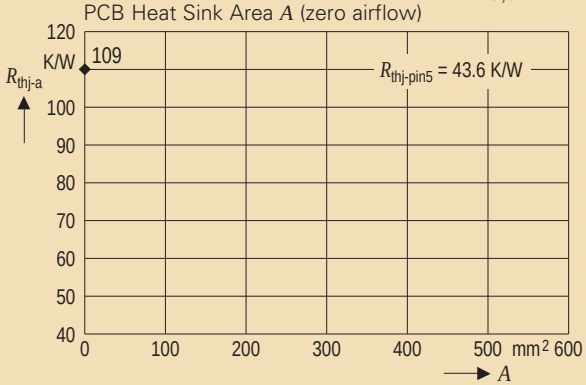
FEM Simulation (chip area ≥ 2 mm²; P_v = 1 W; zero airflow)



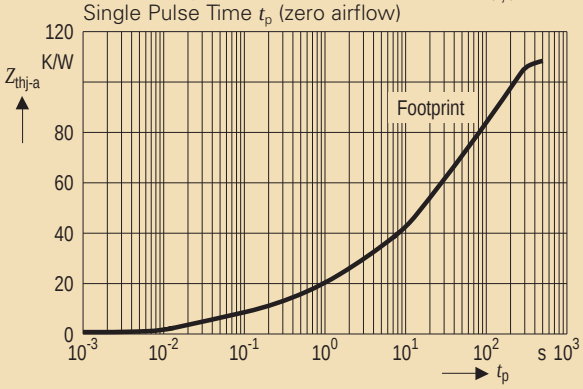
Footprint only; T_a = 298 K; T_{max} = 407 K

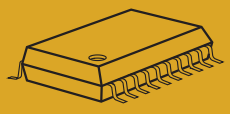
Diagrams

Thermal Resistance Junction to Ambient R_{thj-a} vs.
PCB Heat Sink Area A (zero airflow)



Thermal Impedance Junction to Ambient Z_{thj-a} vs.
Single Pulse Time t_p (zero airflow)

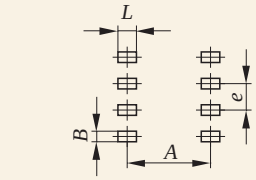




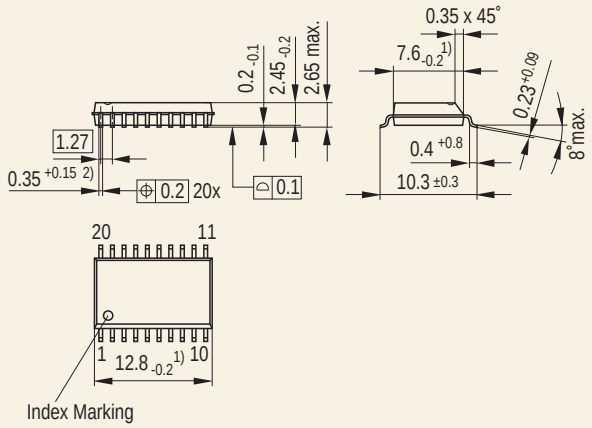
P-DSO-20-6

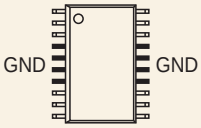
Footprint/Dimensions

Package	e	A	L	B
P-DSO-20-6	1.27	9.73	1.67	0.65



Reflow soldering

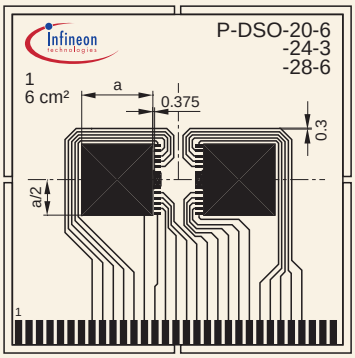




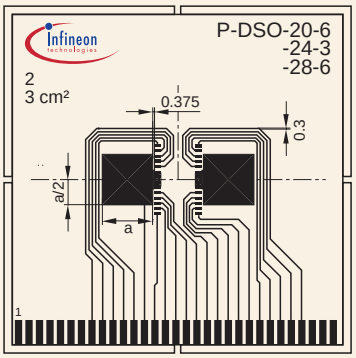
Dimensions in mm

PC-Board

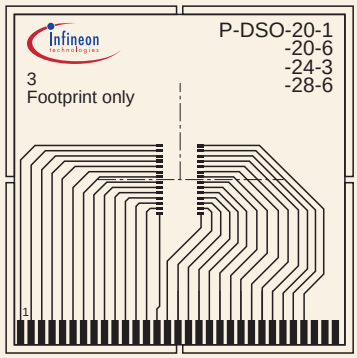
Application-Boards for R_{th} - Measurement



FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 600 mm²; a = 17.32 mm



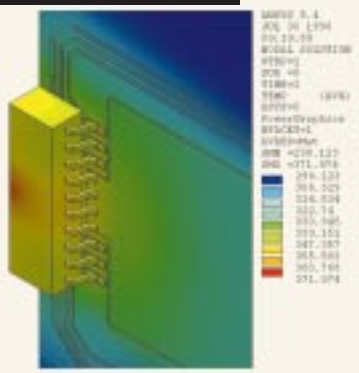
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 300 mm²; a = 12.247 mm



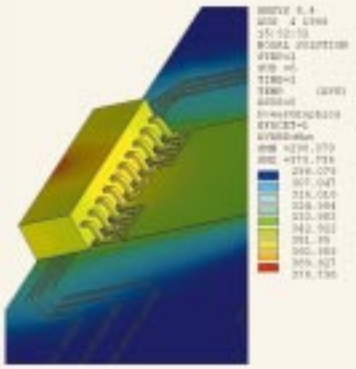
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
Footprint only

Finite Element Method

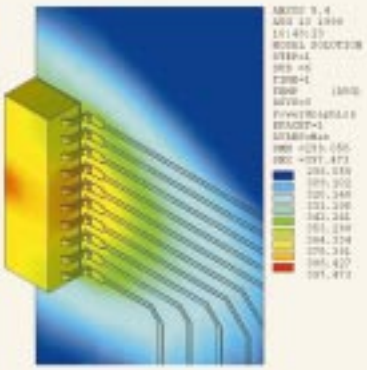
FEM Simulation (chip area ≥ 2 mm²; P_v = 1 W; zero airflow)



A = 600 mm²; T_a = 298 K; T_{max} = 372 K



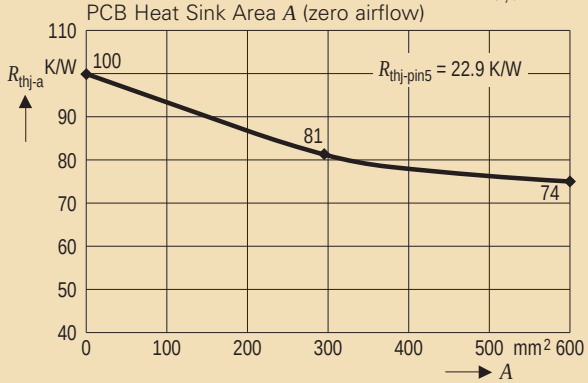
A = 300 mm²; T_a = 298 K; T_{max} = 379 K



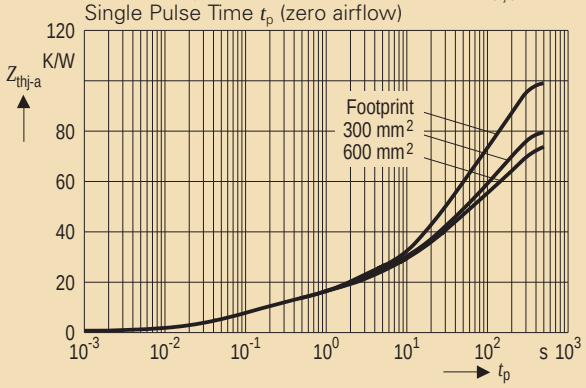
Footprint only; T_a = 298 K; T_{max} = 397 K

Diagrams

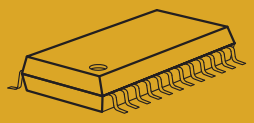
Thermal Resistance Junction to Ambient R_{thj-a} vs.
PCB Heat Sink Area A (zero airflow)



Thermal Impedance Junction to Ambient Z_{thj-a} vs.
Single Pulse Time t_p (zero airflow)



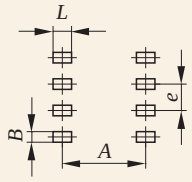
Package and Thermal Information



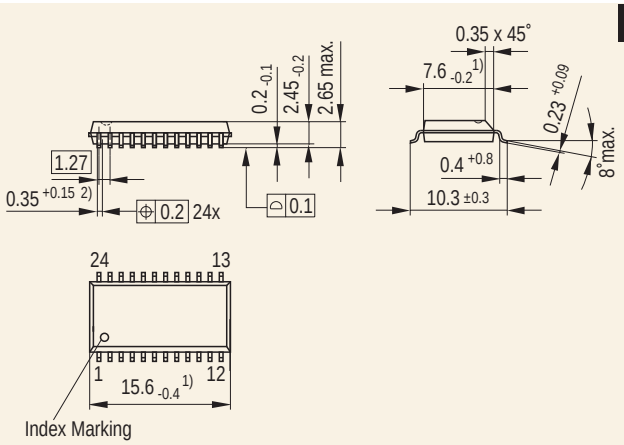
P-DSO-24-3

Footprint/Dimensions

Package	e	A	L	B
P-DSO-24-3	1.27	9.73	1.67	0.65



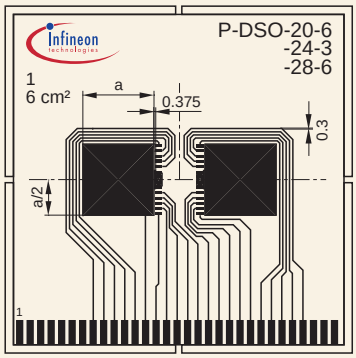
Reflow soldering



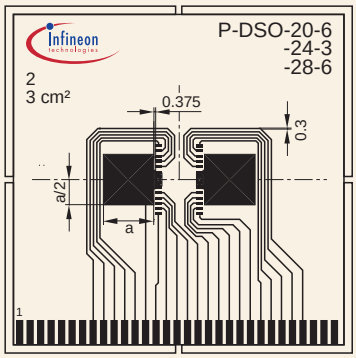
Dimensions in mm

PC-Board

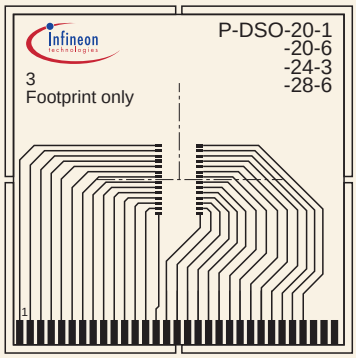
Application-Boards for R_{th} - Measurement



FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 600 mm²; a = 17.32 mm



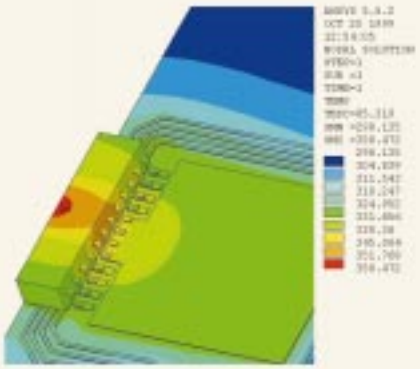
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 300 mm²; a = 12.247 mm



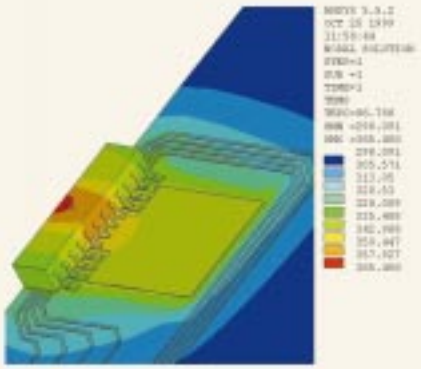
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
Footprint only

Finite Element Method

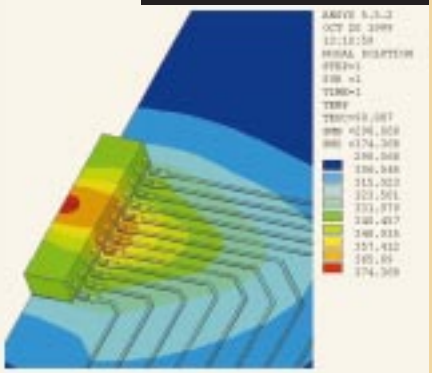
FEM Simulation (chip area ≥ 2 mm²; P_v = 1 W; zero airflow)



A = 600 mm²; T_a = 298 K; T_{max} = 358 K



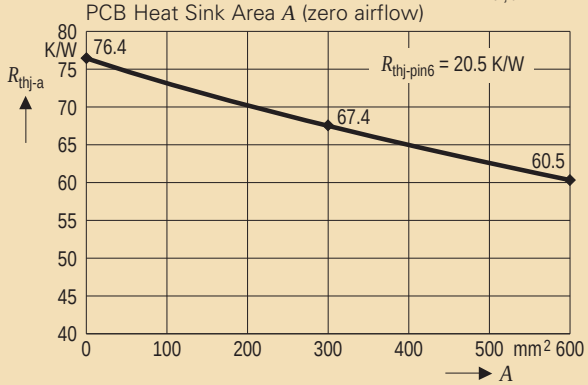
A = 300 mm²; T_a = 298 K; T_{max} = 365 K



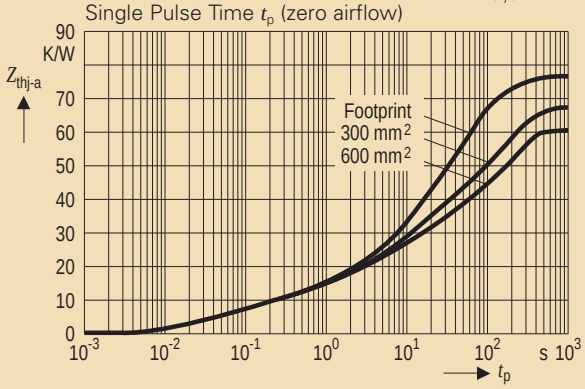
Footprint only; T_a = 298 K; T_{max} = 374 K

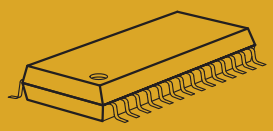
Diagrams

Thermal Resistance Junction to Ambient R_{thj-a} vs.
PCB Heat Sink Area A (zero airflow)



Thermal Impedance Junction to Ambient Z_{thj-a} vs.
Single Pulse Time t_p (zero airflow)

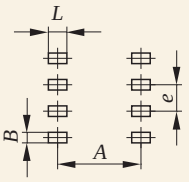




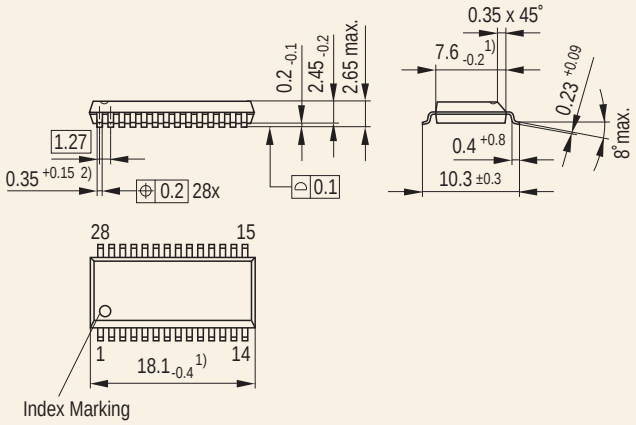
P-DSO-28-6

Footprint/Dimensions

Package	e	A	L	B
P-DSO-28-6	1.27	9.73	1.67	0.65



Reflow soldering

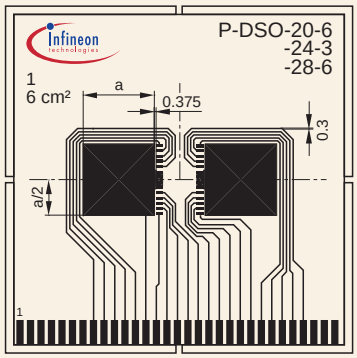


Index Marking

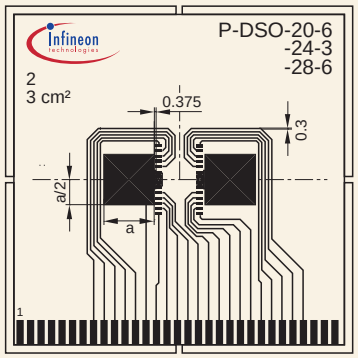
Dimensions in mm

PC-Board

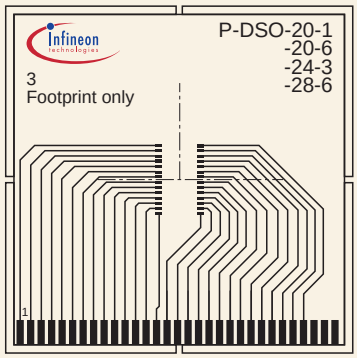
Application-Boards for R_{th} - Measurement



FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 600 mm²; a = 17.32 mm



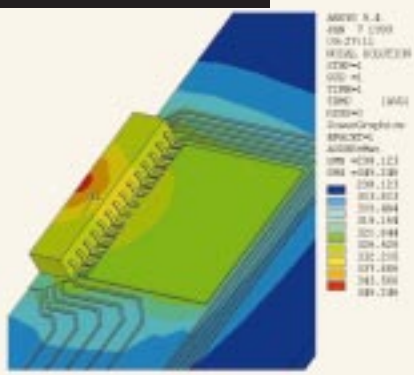
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 300 mm²; a = 12.247 mm



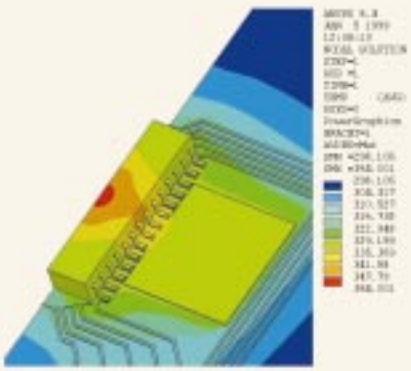
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
Footprint only

Finite Element Method

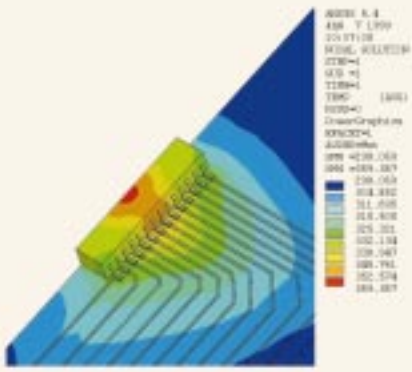
FEM Simulation (chip area ≥ 2 mm²; P_v = 1 W; zero airflow)



A = 600 mm²; T_a = 298 K; T_{max} = 349 K



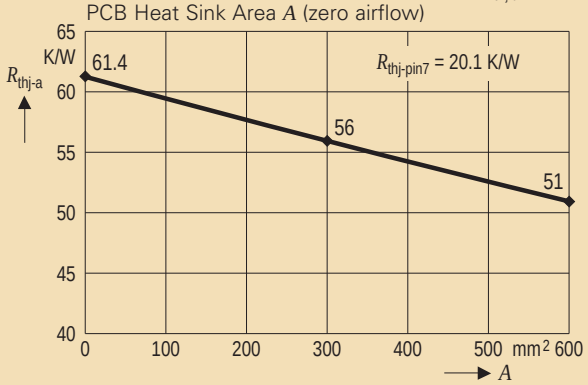
A = 300 mm²; T_a = 298 K; T_{max} = 354 K



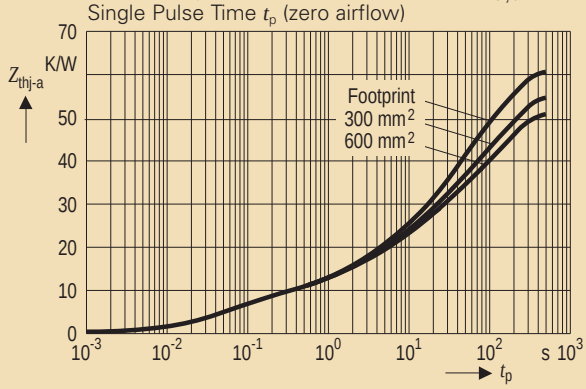
Footprint only; T_a = 298 K; T_{max} = 359 K

Diagrams

Thermal Resistance Junction to Ambient $R_{thj\text{-}a}$ vs.
PCB Heat Sink Area A (zero airflow)



Thermal Impedance Junction to Ambient $Z_{thj\text{-}a}$ vs.
Single Pulse Time t_p (zero airflow)

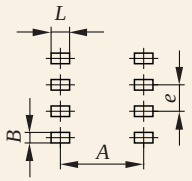


Package and Thermal Information

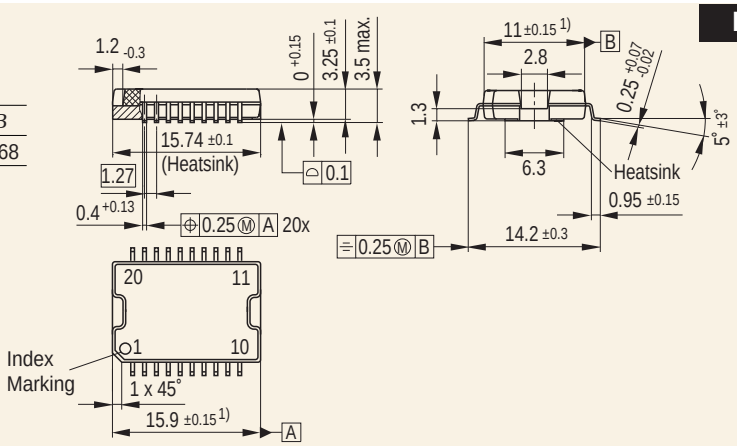
P-DSO-20-10

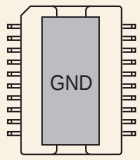
Footprint/Dimensions

Package	e	A	L	B
P-DSO-20-10	1.27	13.48	1.83	0.68



Reflow soldering

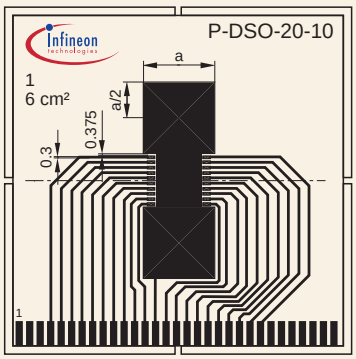




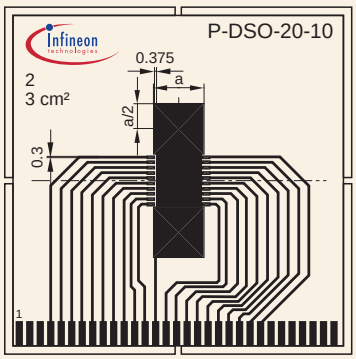
Dimensions in mm

PC-Board

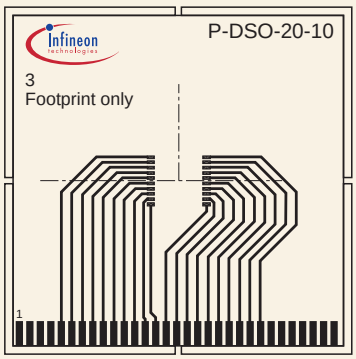
Application-Boards for R_{th} - Measurement



FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 600 mm²; a = 17.32 mm



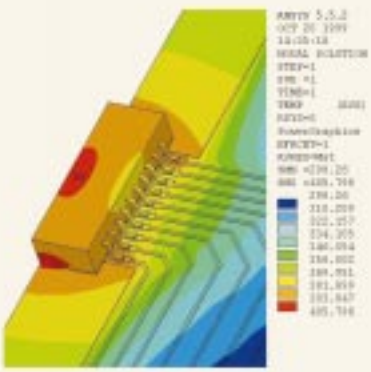
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 300 mm²; a = 12.247 mm



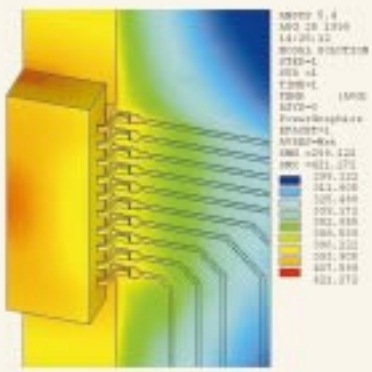
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
Footprint only

Finite Element Method

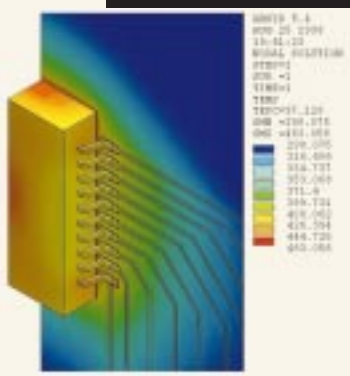
FEM Simulation (chip area ≥ 2 mm²; P_v = 3 W; zero airflow)



A = 600 mm²; T_a = 298 K; T_{max} = 406 K



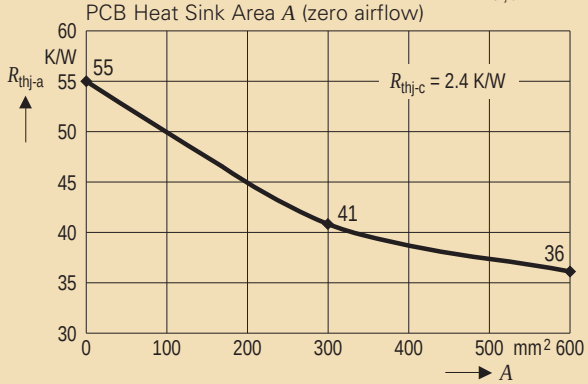
A = 300 mm²; T_a = 298 K; T_{max} = 421 K



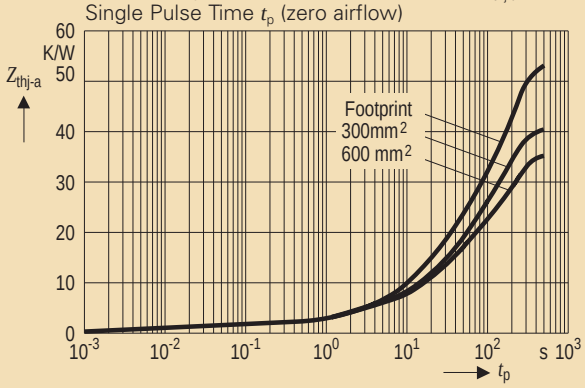
Footprint only; T_a = 298 K; T_{max} = 463 K

Diagrams

Thermal Resistance Junction to Ambient R_{thj-a} vs. PCB Heat Sink Area A (zero airflow)



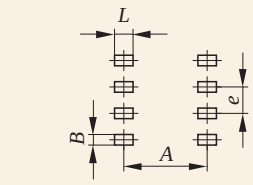
Thermal Impedance Junction to Ambient Z_{thj-a} vs. Single Pulse Time t_p (zero airflow)



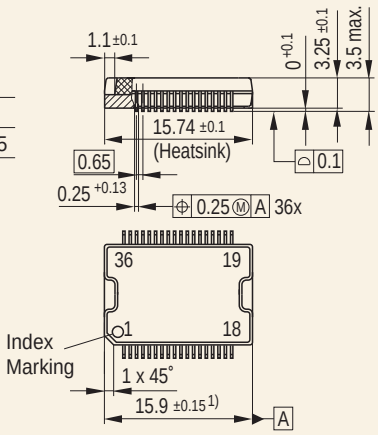
P-DSO-36-10

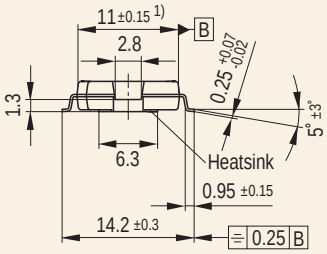
Footprint/Dimensions

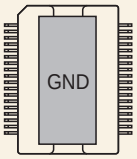
Package	e	A	L	B
P-DSO-36-10	0.65	13.48	1.83	0.45



Reflow soldering



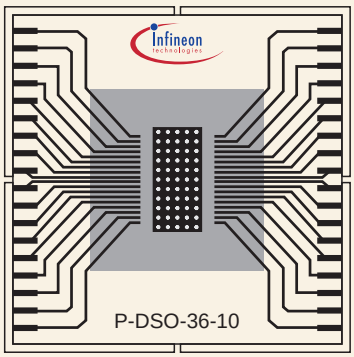




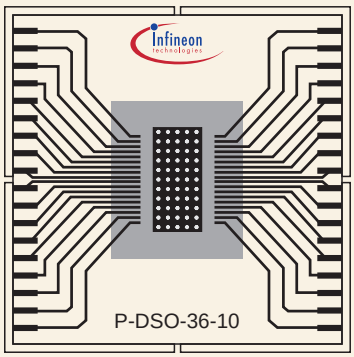
Dimensions in mm

PC-Board

Application-Boards for R_{th} - Measurement



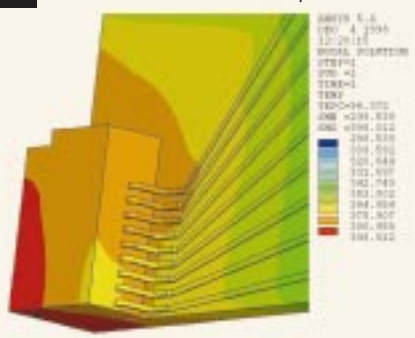
FR4; 47 x 50 x 1.5 mm; 70 µ Cu
A = 600 mm²; 24.5 x 24.5 mm



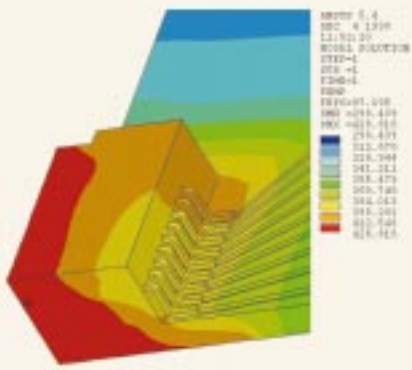
FR4; 47 x 50 x 1.5 mm; 70 µ Cu
A = 300 mm²; 16 x 19 mm

Finite Element Method

FEM Simulation (chip area ≥ 2 mm²; P_v = 3.5 W; zero airflow)



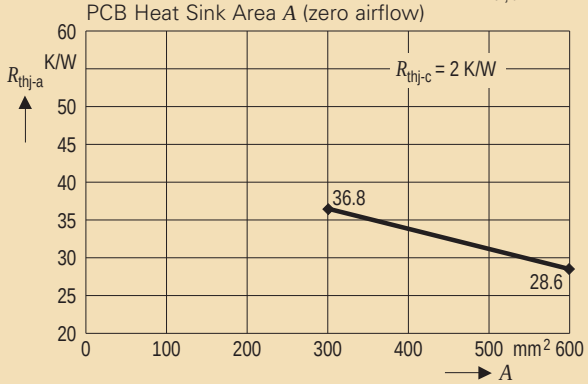
A = 600 mm²; T_a = 298 K; T_{max} = 398 K



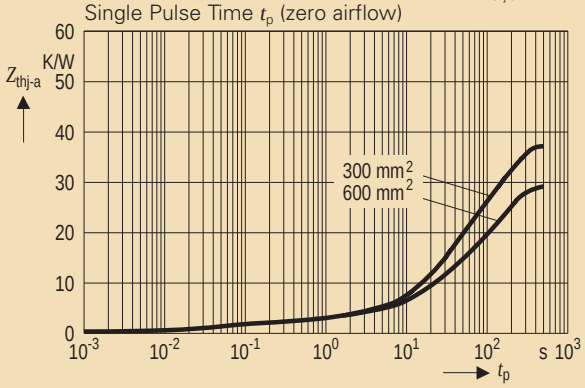
A = 300 mm²; T_a = 298 K; T_{max} = 427 K

Diagrams

Thermal Resistance Junction to Ambient R_{thj-a} vs. PCB Heat Sink Area A (zero airflow)



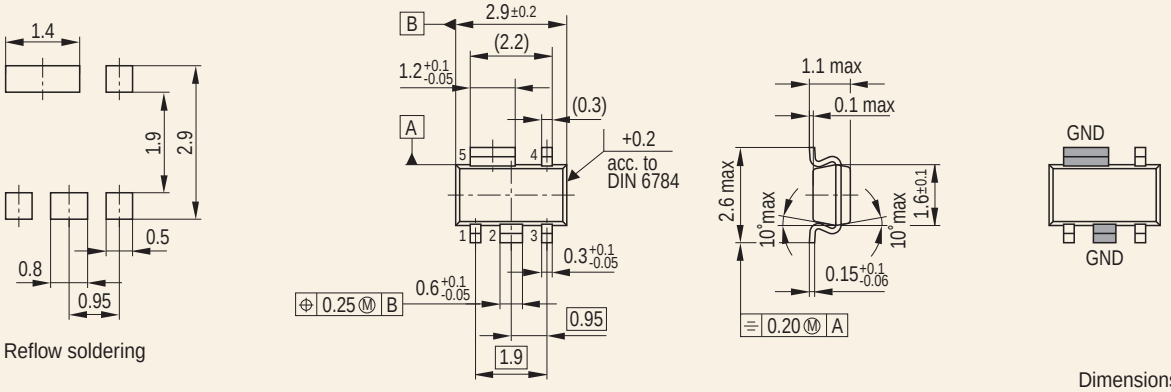
Thermal Impedance Junction to Ambient Z_{thj-a} vs. Single Pulse Time t_p (zero airflow)



Package and Thermal Information

SCT595-5-1

Footprint/Dimensions

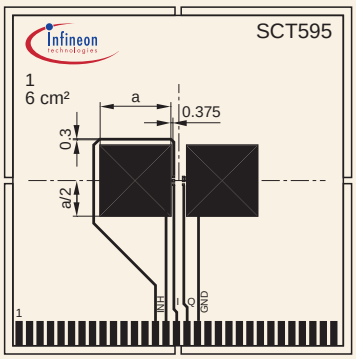


Reflow soldering

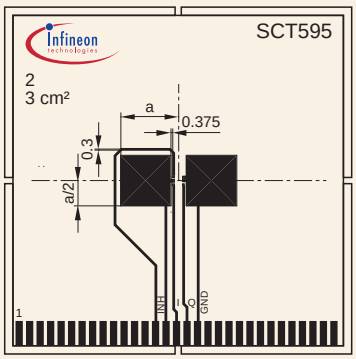
Dimensions in mm

PC-Board

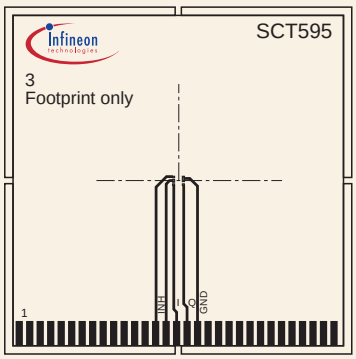
Application-Boards for R_{th} - Measurement



FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 600 mm²; a = 17.32 mm



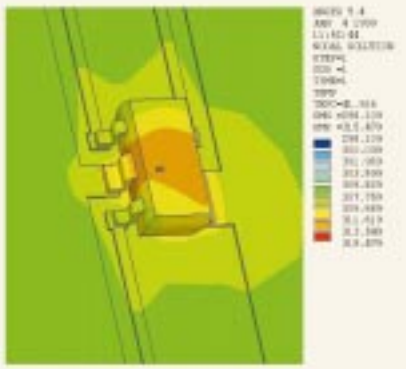
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 300 mm²; a = 12.247 mm



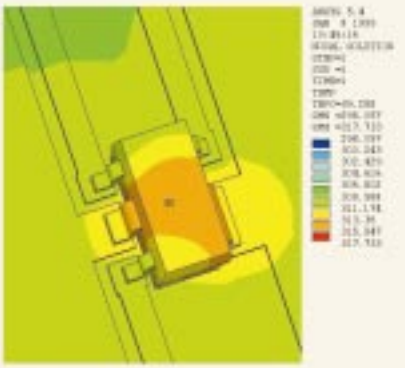
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
Footprint only

Finite Element Method

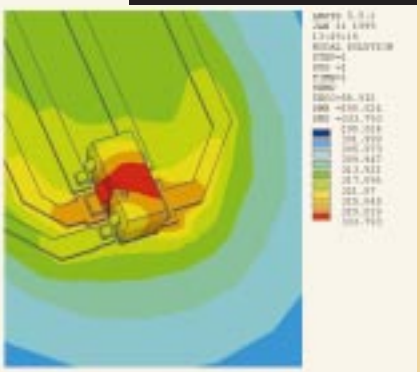
FEM Simulation (chip area ≥ 2 mm²; P_v = 0.2 W; zero airflow)



A = 600 mm²; T_a = 298 K; T_{max} = 315 K



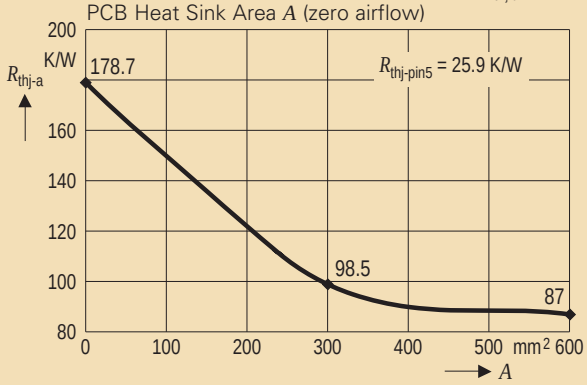
A = 300 mm²; T_a = 298 K; T_{max} = 318 K



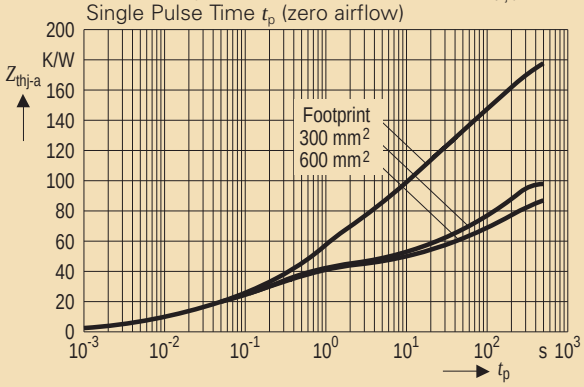
Footprint only; T_a = 298 K; T_{max} = 334 K

Diagrams

Thermal Resistance Junction to Ambient R_{thj-a} vs.
PCB Heat Sink Area A (zero airflow)

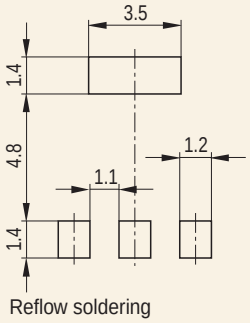


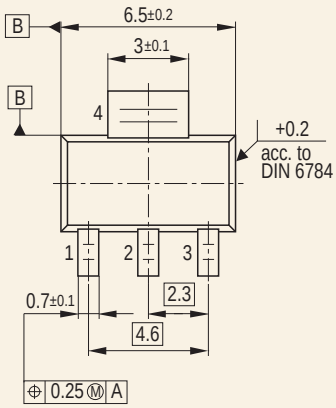
Thermal Impedance Junction to Ambient Z_{thj-a} vs.
Single Pulse Time t_p (zero airflow)

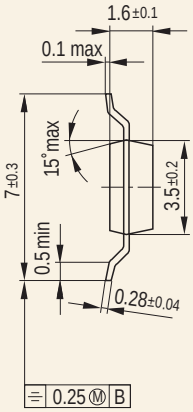


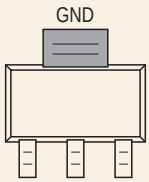
SOT223-4-2

Footprint/Dimensions





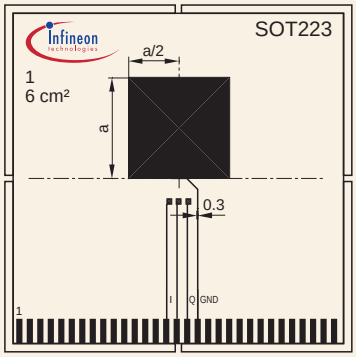




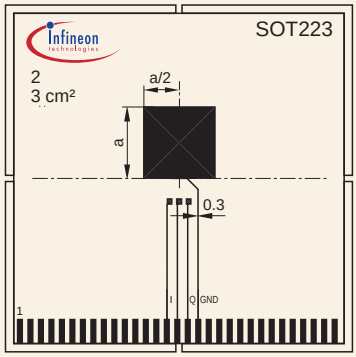
Dimensions in mm

PC-Board

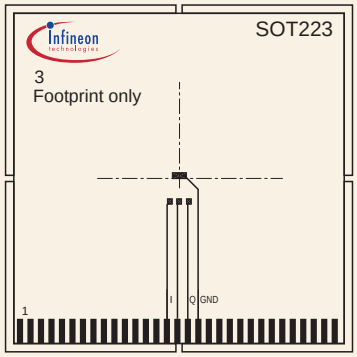
Application-Boards for R_{th} - Measurement



FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 600 mm²; a = 24.49 mm



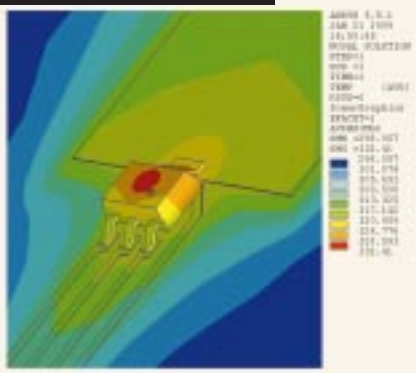
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 300 mm²; a = 17.32 mm



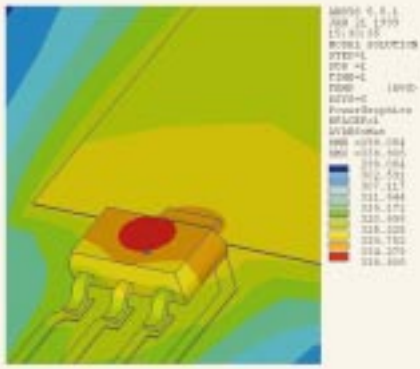
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
Footprint only

Finite Element Method

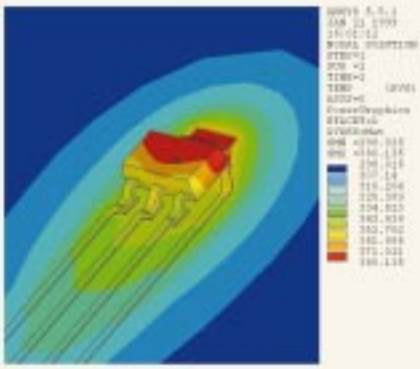
FEM Simulation (chip area ≥ 2 mm²; P_v = 0.5 W; zero airflow)



A = 600 mm²; T_a = 298 K; T_{max} = 332 K



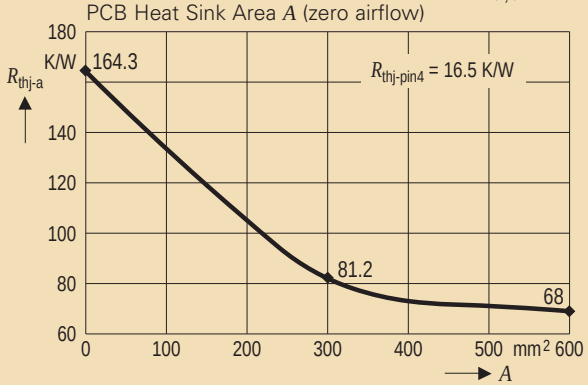
A = 300 mm²; T_a = 298 K; T_{max} = 339 K



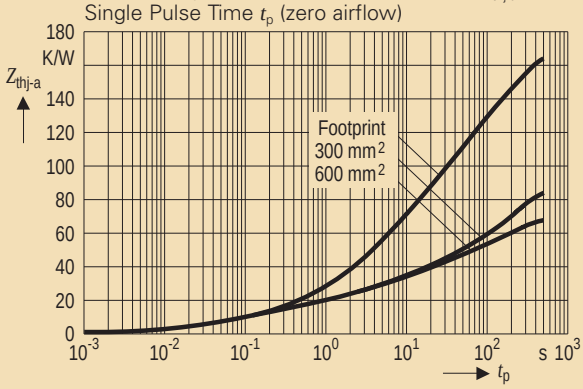
Footprint only; T_a = 298 K; T_{max} = 380 K

Diagrams

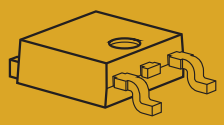
Thermal Resistance Junction to Ambient $R_{thj\text{-}a}$ vs.
PCB Heat Sink Area A (zero airflow)



Thermal Impedance Junction to Ambient $Z_{thj\text{-}a}$ vs.
Single Pulse Time t_p (zero airflow)

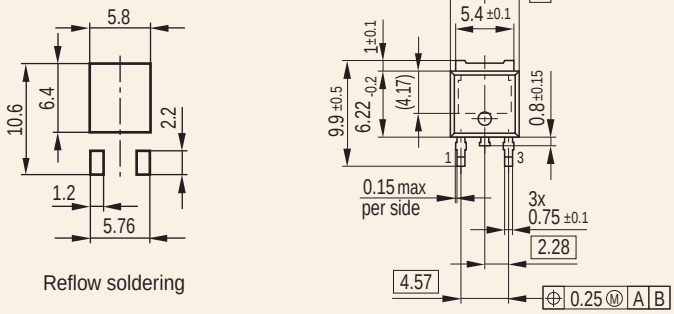


Package and Thermal Information



P-TO252-3-1

Footprint/Dimensions

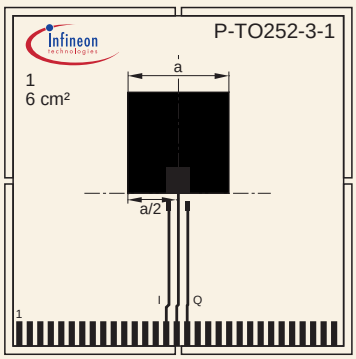


Reflow soldering

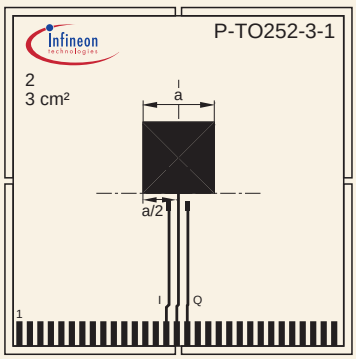
Dimensions in mm

PC-Board

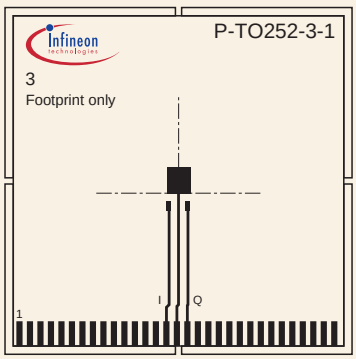
Application-Boards for R_{th} - Measurement



FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 600 mm²; a = 24.49 mm



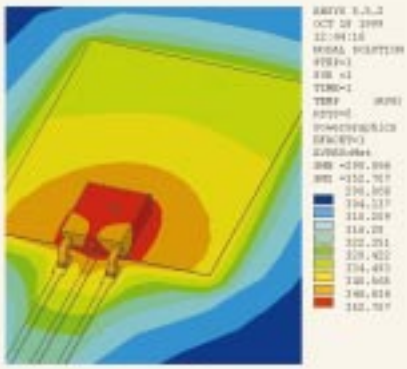
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 300 mm²; a = 17.32 mm



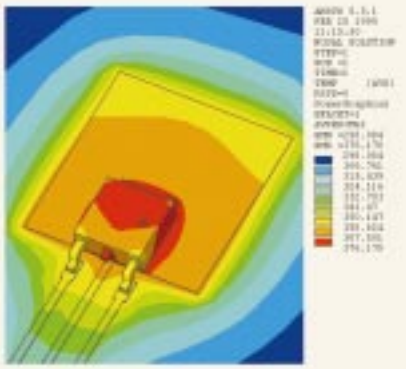
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
Footprint only

Finite Element Method

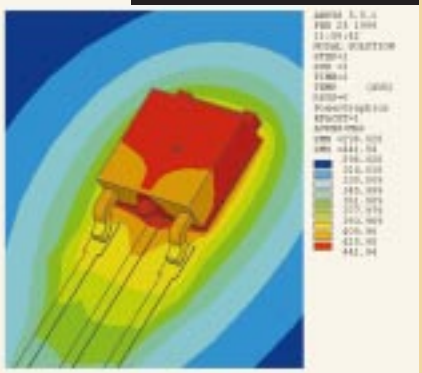
FEM Simulation (chip area ≥ 2 mm²; P_v = 1 W; zero airflow)



A = 600 mm²; T_a = 298 K; T_{max} = 353 K



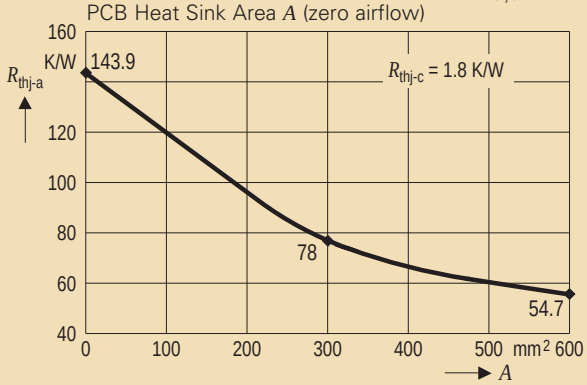
A = 300 mm²; T_a = 298 K; T_{max} = 376 K



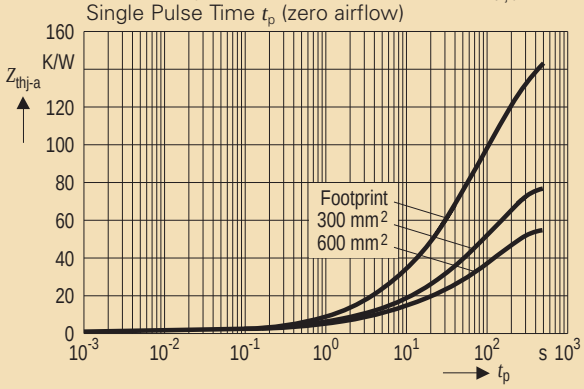
Footprint only; T_a = 298 K; T_{max} = 442 K

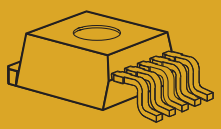
Diagrams

Thermal Resistance Junction to Ambient R_{thj-a} vs.
PCB Heat Sink Area A (zero airflow)



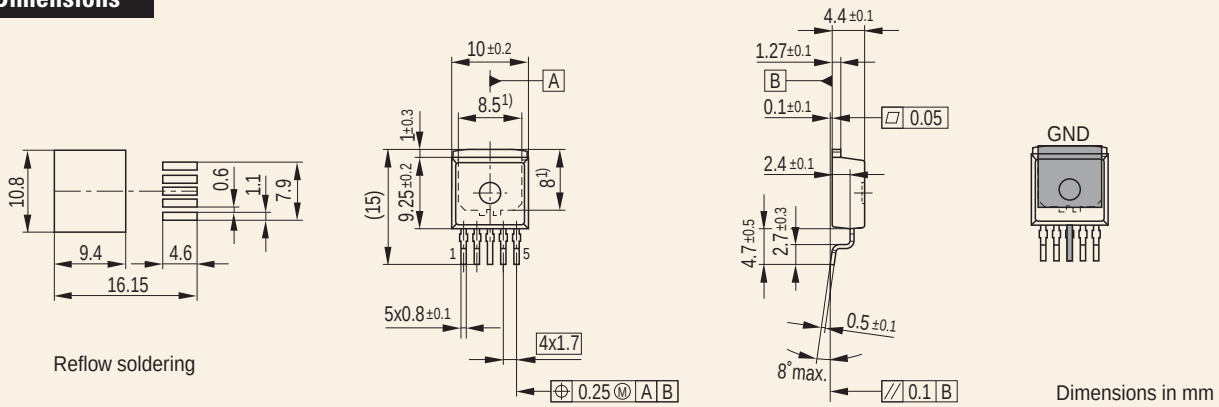
Thermal Impedance Junction to Ambient Z_{thj-a} vs.
Single Pulse Time t_p (zero airflow)





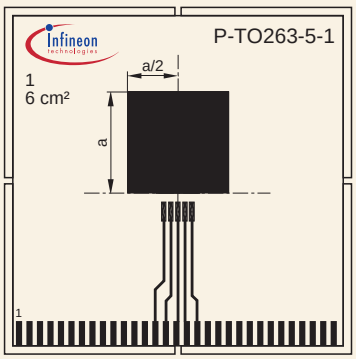
P-TO263-5-1

Footprint/Dimensions

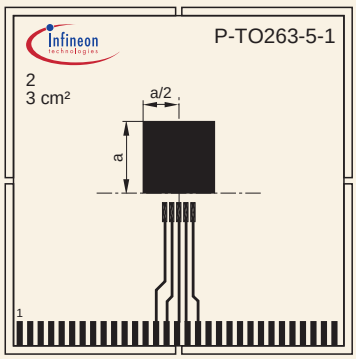


PC-Board

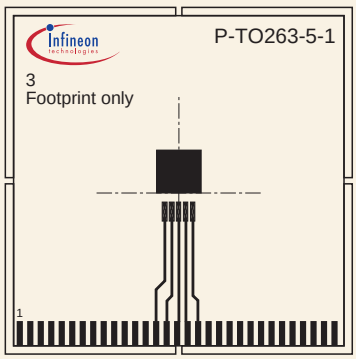
Application-Boards for R_{th} - Measurement



FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 600 mm²; a = 24.49 mm



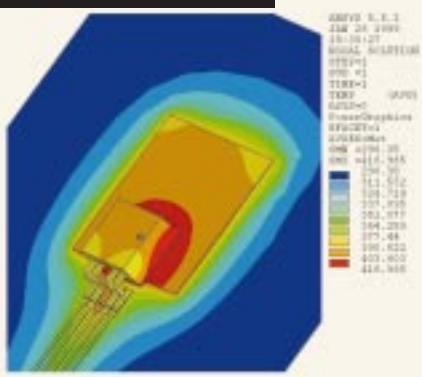
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
A = 300 mm²; a = 17.32 mm



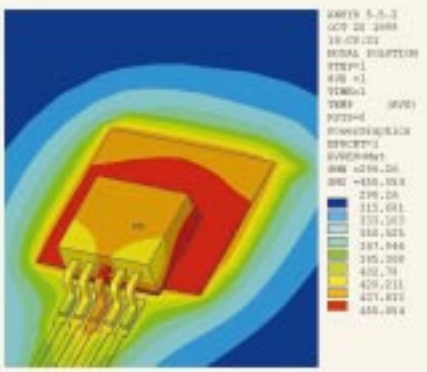
FR4; 80 x 80 x 1.5 mm; 35 µ Cu, 5 µ Sn
Footprint only

Finite Element Method

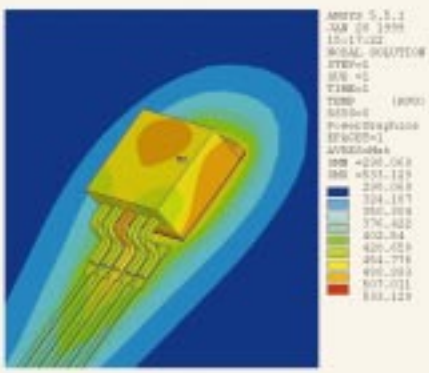
FEM Simulation (chip area ≥ 2 mm²; P_v = 3 W; zero airflow)



A = 600 mm²; T_a = 298 K; T_{max} = 417 K



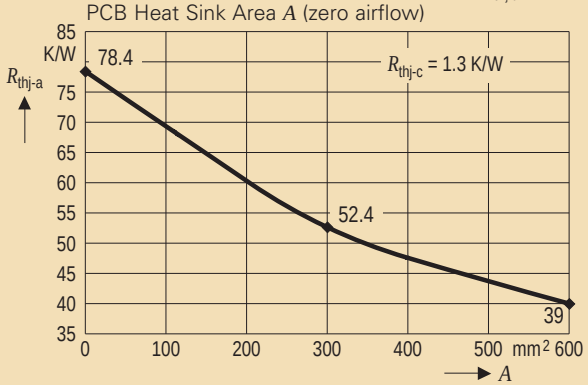
A = 300 mm²; T_a = 298 K; T_{max} = 455 K



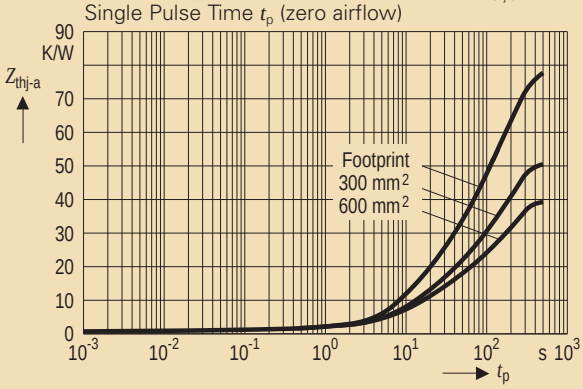
Footprint only; T_a = 298 K; T_{max} = 533 K

Diagrams

Thermal Resistance Junction to Ambient R_{thj-a} vs. PCB Heat Sink Area A (zero airflow)



Thermal Impedance Junction to Ambient Z_{thj-a} vs. Single Pulse Time t_p (zero airflow)



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