

# 74LVT14

## 3.3 V hex inverter Schmitt trigger

Rev. 02 — 25 April 2008

Product data sheet

### 1. General description

The 74LVT14 is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3 V. It is capable of transforming slowly changing input signals into sharply defined, jitter free output signals. In addition, it has a greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive-going and negative-going inputs. The threshold differential (typically 600 mV) is determined internally by resistor ratios and is insensitive to temperature and supply voltage variations.

### 2. Features

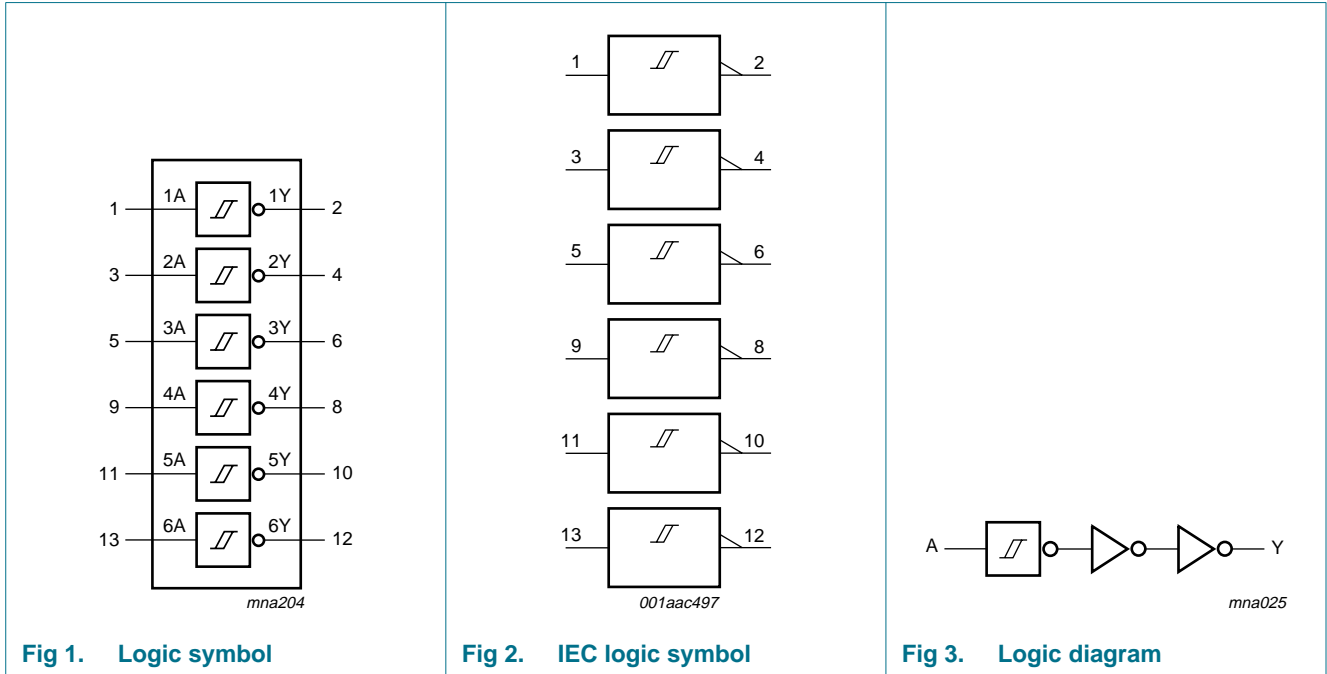
- Different positive and negative going input threshold voltages
- Tolerant of slow input transitions
- High noise immunity
- TTL input and output switching levels
- Output capability: +32 mA/–20 mA
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V

### 3. Ordering information

Table 1. Ordering information

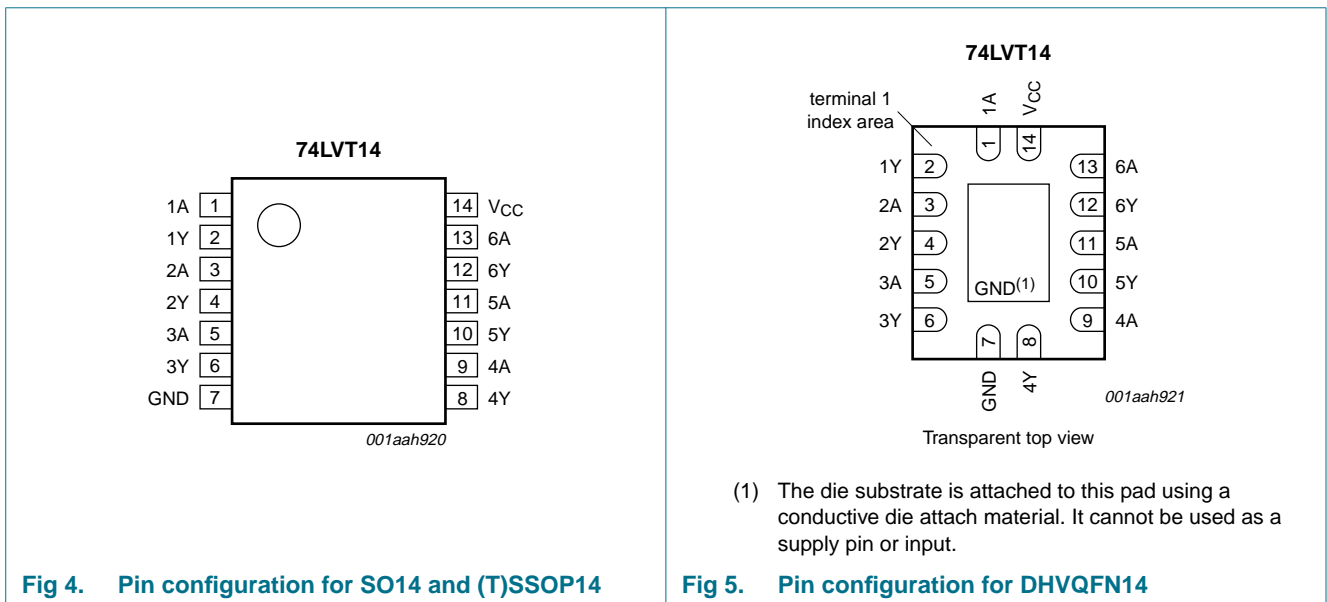
Type number	Package			
	Temperature range	Name	Description	Version
74LVT14D	–40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 7.5 mm	SOT108-1
74LVT14DB	–40 °C to +85 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVT14PW	–40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVT14BQ	–40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 4.5 × 0.85 mm	SOT762-1

### 4. Functional diagram



### 5. Pinning information

#### 5.1 Pinning



## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 6A	1, 3, 5, 9, 11, 13	data input
1Y to 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	positive supply voltage

## 6. Functional description

Table 3. Function selection

Inputs	Output
nA	nY
L	H
H	L

- [1] H = HIGH voltage level;  
L = LOW voltage level.

## 7. Limiting values

Table 4. Limiting values [1]

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
V <sub>I</sub>	input voltage		[2] -0.5	+7.0	V
V <sub>O</sub>	output voltage	output in OFF or HIGH state	[2] -0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
I <sub>O</sub>	output current	output in LOW state	-	64	mA
		output in HIGH state	-32	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j</sub>	junction temperature			+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C	[3]	500	mW

- [1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- [2] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- [3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.  
For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.  
For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.7	-	3.6	V
$V_I$	input voltage		0	-	5.5	V
$I_{OH}$	HIGH-level output current		-20	-	-	mA
$I_{OL}$	LOW-level output current		-	-	32	mA
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	output enabled	0	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
$V_{T+}$	positive-going threshold voltage	$V_{CC} = 3.3$ V; see <a href="#">Figure 7</a>	1.5	1.7	2.0	V
$V_{T-}$	negative-going threshold voltage	$V_{CC} = 3.3$ V; see <a href="#">Figure 7</a>	0.9	1.1	1.3	V
$V_H$	hysteresis voltage	$V_{CC} = 3.3$ V; see <a href="#">Figure 7</a>	0.4	0.6	-	V
$V_{IK}$	input clamping voltage	$V_{CC} = 2.7$ V; $I_{IK} = -18$ mA	-1.2	-	-	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	
$V_{OH}$	HIGH-level output voltage	$V_{CC} = 2.7$ V to 3.6 V; $I_{OH} = -100$ $\mu$ A	$V_{CC} - 0.2$	-	-	V
		$V_{CC} = 2.7$ V; $I_{OH} = -6$ mA	2.4	-	-	V
		$V_{CC} = 3.0$ V; $I_{OH} = -20$ mA	2.0	-	-	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 2.7$ V; $I_{OL} = 100$ $\mu$ A	-	-	0.2	V
		$V_{CC} = 2.7$ V; $I_{OL} = 24$ mA	-	-	0.5	V
		$V_{CC} = 3.0$ V; $I_{OL} = 32$ mA	-	-	0.5	V
$I_I$	input leakage current	$V_{CC} = 0$ V or 3.6 V; $V_I = 5.5$ V	-	-	10	$\mu$ A
		$V_{CC} = 3.6$ V; $V_I = V_{CC}$ or GND	-	-	$\pm 1$	$\mu$ A
$I_{OFF}$	power-off leakage current	$V_{CC} = 0$ V; $V_I$ or $V_O = 0$ V to 4.5 V	-	-	$\pm 100$	$\mu$ A
$I_{CC}$	supply current	$V_{CC} = 3.6$ V; $V_I =$ GND or $V_{CC}$ ; $I_O = 0$ A				
		outputs HIGH	-	-	0.02	mA
		outputs LOW	-	1.5	3	mA
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 3.0$ V to 3.6 V; one input = $V_{CC} - 0.6$ V; other inputs at $V_{CC}$ or GND	<sup>[2]</sup> -	-	0.2	mA
$C_I$	input capacitance	$V_I = 0$ V or 3.0 V	-	3	-	pF

[1] All typical values are measured at  $V_{CC} = 3.3$  V (unless stated otherwise) and  $T_{amb} = 25$  °C.

[2] This is the increase in the supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.

## 10. Dynamic characteristics

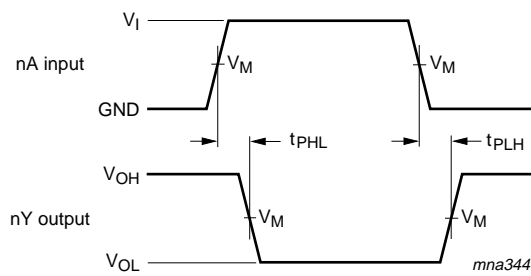
**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
t <sub>PLH</sub>	LOW to HIGH propagation delay	nA to nY				
		V <sub>CC</sub> = 2.7 V	-	-	6.9	ns
		V <sub>CC</sub> = 3.3 V + 0.3 V	1.0	3.8	5.7	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	nA to nY				
		V <sub>CC</sub> = 2.7 V	-	-	4.1	ns
		V <sub>CC</sub> = 3.3 V + 0.3 V	1.0	3.2	4.5	ns

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 3.3 V.

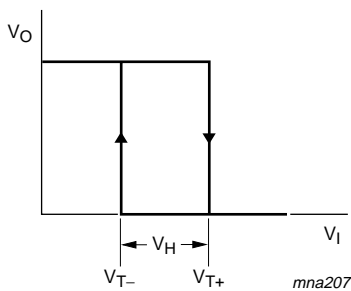
## 11. Waveforms



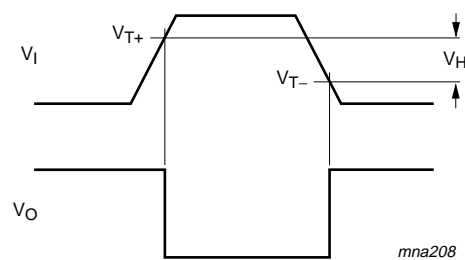
See [Table 8](#) for measurement points.

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage levels that occur with the output load.

**Fig 6. nA Input to nY output propagation delays**



a. Transfer characteristics

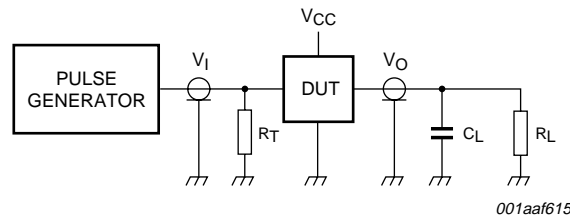
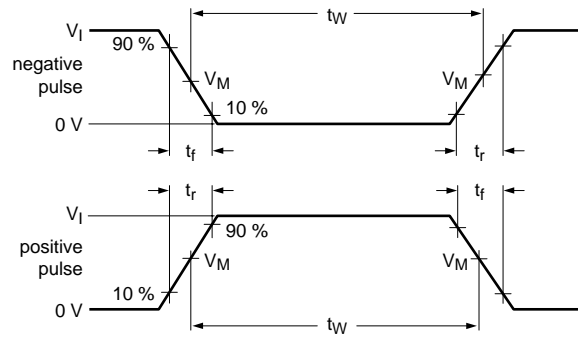


b. Voltage levels

**Fig 7. Definition of VT+, VT- and VH**

Table 8. Measurement points

V <sub>CC</sub>	Input	Output
	V <sub>M</sub>	V <sub>M</sub>
2.7 V to 3.6 V	1.5 V	1.5 V



Test data is given in given in [Table 9](#).

Definitions for test circuit:

R<sub>L</sub> = Load resistance;

C<sub>L</sub> = Load capacitance including jig and probe capacitance;

R<sub>T</sub> = Termination resistance should be equal to output impedance Z<sub>o</sub> of the pulse generator.

Fig 8. Load circuitry for switching times

Table 9. Test data

Supply	Input pulse requirements				Load	
V <sub>CC</sub>	V <sub>I</sub>	Repetition rate	t <sub>W</sub>	t <sub>r</sub> , t <sub>f</sub>	R <sub>L</sub>	C <sub>L</sub>
2.7 V to 3.3 V	2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500 Ω	50 pF

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

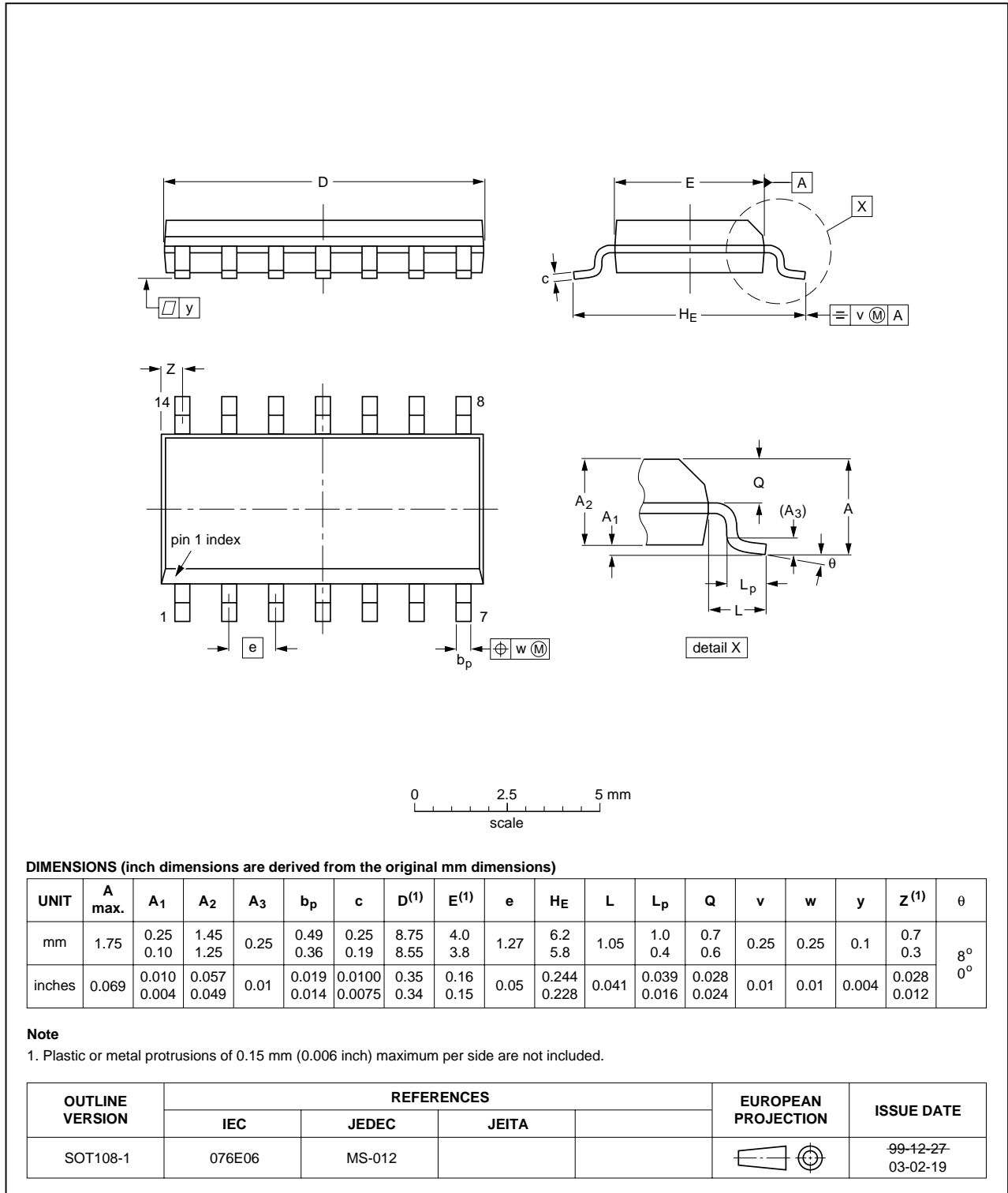


Fig 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

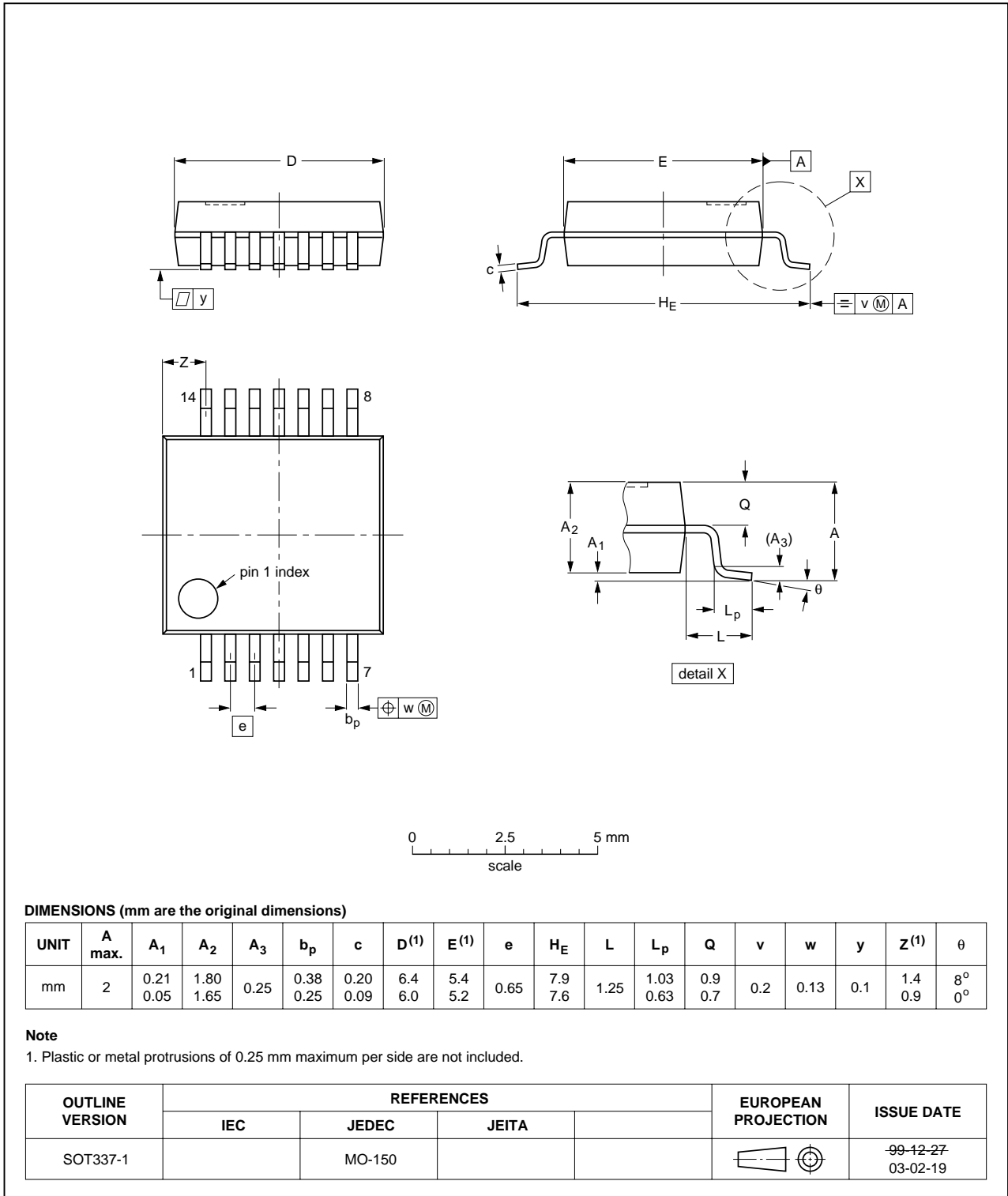


Fig 10. Package outline SOT337-1 (SSOP14)



TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

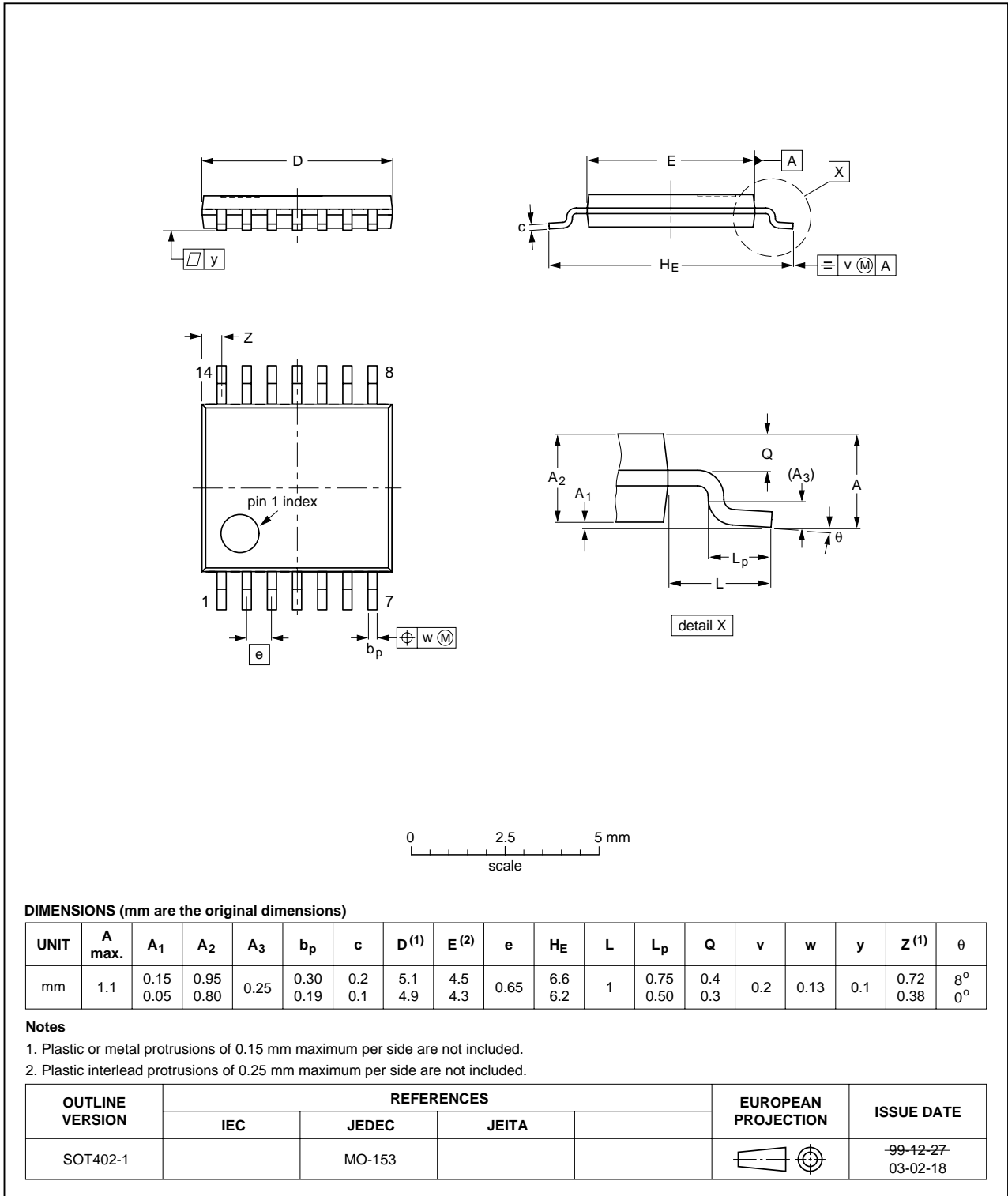


Fig 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

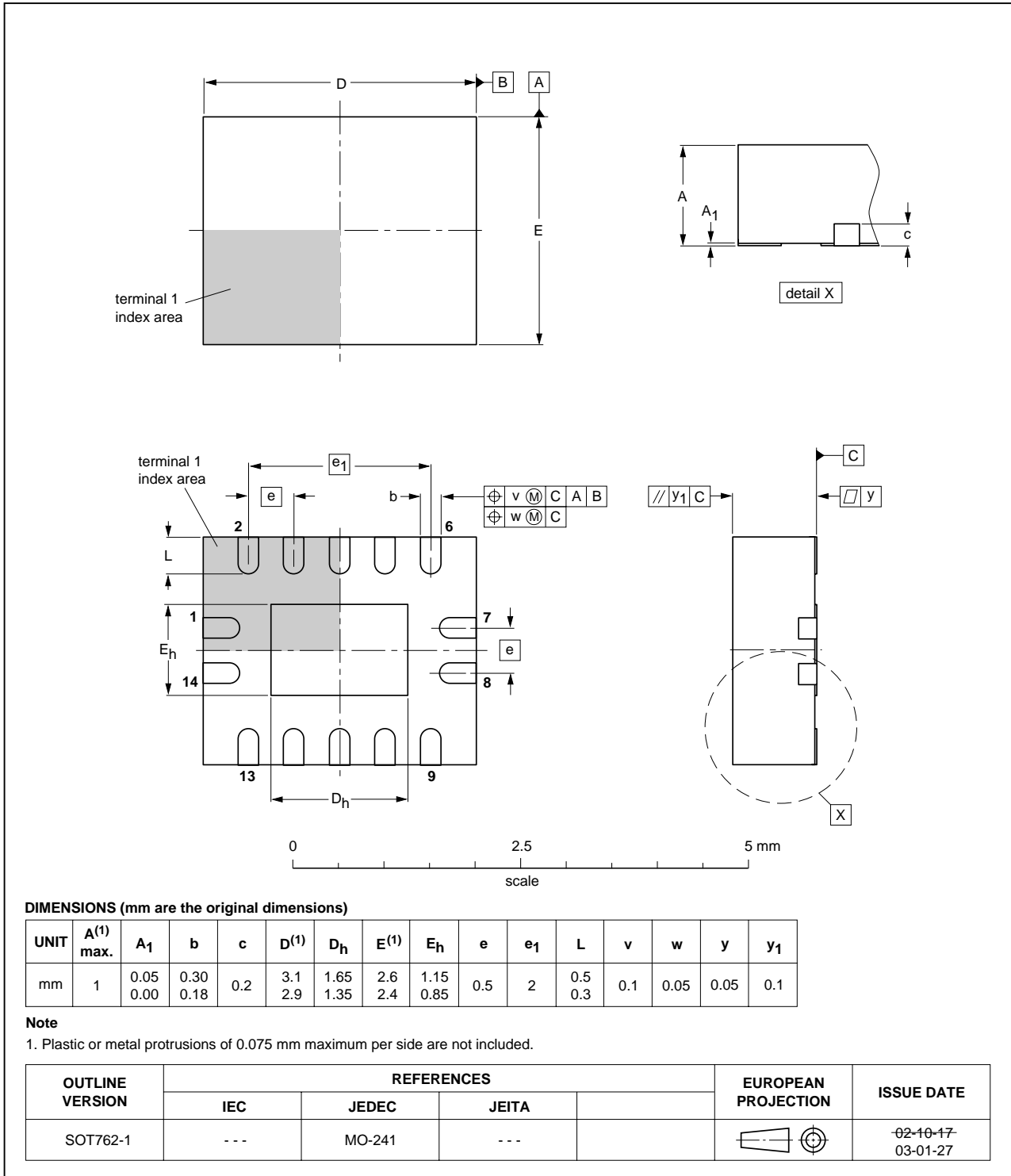


Fig 12. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Integrated Bipolar junction transistors and CMOS
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT14_2	20080425	Product data sheet	-	74LVT14_1
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Quick reference section removed.</li> <li>• DHVQFN14 package added to <a href="#">Section 3 “Ordering information”</a> and <a href="#">Section 12 “Package outline”</a>.</li> <li>• <a href="#">Section 13 “Abbreviations”</a> added.</li> </ul>			
74LVT14_1	19960828	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 15.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 15.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

### 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 17. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>1</b>
<b>4</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>5</b>	<b>Pinning information</b> .....	<b>2</b>
5.1	Pinning .....	2
5.2	Pin description .....	3
<b>6</b>	<b>Functional description</b> .....	<b>3</b>
<b>7</b>	<b>Limiting values</b> .....	<b>3</b>
<b>8</b>	<b>Recommended operating conditions</b> .....	<b>4</b>
<b>9</b>	<b>Static characteristics</b> .....	<b>4</b>
<b>10</b>	<b>Dynamic characteristics</b> .....	<b>5</b>
<b>11</b>	<b>Waveforms</b> .....	<b>5</b>
<b>12</b>	<b>Package outline</b> .....	<b>7</b>
<b>13</b>	<b>Abbreviations</b> .....	<b>11</b>
<b>14</b>	<b>Revision history</b> .....	<b>11</b>
<b>15</b>	<b>Legal information</b> .....	<b>12</b>
15.1	Data sheet status .....	12
15.2	Definitions .....	12
15.3	Disclaimers .....	12
15.4	Trademarks .....	12
<b>16</b>	<b>Contact information</b> .....	<b>12</b>
<b>17</b>	<b>Contents</b> .....	<b>13</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2008.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 25 April 2008

Document identifier: 74LVT14\_2