PIC16(L)F720/721 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F720/721 family devices that you have received conform functionally to the current Device Data Sheet (DS41341**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F720/721 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**).

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F720/721 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A3
PIC16F720	01 1100 000x xxxx	0x3
PIC16LF720	01 1100 010x xxxx	0x3
PIC16F721	01 1100 001x xxxx	0x3
PIC16LF721	01 1100 011x xxxx	0x3

Note 1: The Device ID is located at 2006h. The 5 Least Significant bits comprise the revision ID.

2: Refer to the *"PIC16F720/721 Memory Programming Specification"* (DS41409) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A3
AUSART	OERR Flag	1.1	OERR flag not clearing.	X
AUSART	Interrupts	1.2	Starting the Interrupt Service Routine.	X
Interrupts	Stack Push	2.	Interrupt logic incorrectly pushes two addresses to the stack.	X

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (as applicable).

1. Module: AUSART

1.1 OERR Flag Not Clearing

The OERR flag of the RCSTA register is reset only by either clearing the CREN bit of the RCSTA register or by a device Reset. Clearing the SPEN bit of the RCSTA register does not clear the OERR flag.

Work around

Clear the OERR flag by clearing the CREN bit in lieu of clearing the SPEN bit.

Affected Silicon Revisions

A3							
X							

1.2 Starting the Interrupt Service Routine

When the AUSART is configured for Synchronous mode and either an RCIF or TXIF flag event wakes the device from Sleep, then execution of the Interrupt Service Routine (ISR) will begin immediately after the two instructions following the SLEEP instruction have finished executing.

Work around

Follow the SLEEP instruction with two NOP instructions or two instructions desired to be executed before the ISR begins.

Affected Silicon Revisions

A3							
X							

2. Module: Interrupts

The interrupt logic incorrectly pushes two addresses to the stack when vectoring to the interrupt vector. Specifically, the interrupt vector address 0x4 is incorrectly pushed to the stack after the current PC, at the time the interrupt was received, is pushed. This will cause the stack to overflow if the user program is operating seven calls deep when an interrupt arrives. Because the stack is circular, the overflow causes the first stack address to be overwritten.

Work around

Disable interrupts by clearing the GIE bit in the INTCON register whenever the user program is operating seven calls deep. This ensures that interrupts will not cause the stack to overflow.

Affected Silicon Revisions

A3							
X							

Data Sheet Clarifications

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev. A Document (02/2011)

Original release of this document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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