# EXACT BUS CLOCKING APPLICATION NOTE

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**ADVANCED**

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## CONTENTS

## 1. REFERENCES

[1] Vitesse VSC7135 1.25 Gbits/sec Vitesse Gigabit Ethernet transceiver datasheet.

[2] PMC-970861 Octal 10/100 Mbit/s Ethernet Switch Port Controller Data Sheet (PM3370), Issue 3, June 1998.

[3] PMC-971034 8 port Gigabit EXACT Bus Switching Matrix, Data Sheet (PM3390), Issue 3, June 1998.

[4] PMC-970862 Gigabit Ethernet Switch Port Controller Data Sheet (PM3380), Issue 3, June 1998.

[5] PMC-970215 EXACT Bus Protocol Specification, Issue 3, June 1998.

[6] Hewlett Packard HDMP-1636 Transceiver SERDES Data Sheet.

[7] AMD 79761 GigaPHY SERDES Data Sheet.

## 2. INTRODUCTION

The PMC EXACT advanced switching chipset is based on the EXACT bus, which provide the high speed switching interconnect between the EXACT switching devices in building scalable and flexible switches.

The devices in this generation are the PM3370 (and the PM3371), which is an 8 port 10/100 Ethernet switch port controller; the PM3380, which is a single port Gigabit Ethernet port controller; the PM3390, which is the switch matrix capable of handling 8 EXACT ports to provide a bandwidth of 8 Gbps non-blocking; and the PM3391 which is a 6-EXACT port matrix device. Typical port counts at a system level are 0/8/1, 0/16/2, 0/32/4 etc.

The EXACT bus stands for Ethernet Switching Access Control and Termination. The EXACT bus has a raw bandwidth of 1.25 Gbps in the transmit direction and 1.25 Gbps in the receive direction. Please refer to the PMC-970215 EXACT Protocol Specification for a detail technical description of the EXACT bus operation.

The purpose of this document is to provide a detailed description of the EXACT bus clocking configuration for the PM3370, PM3371, PM3380, PM3390 and PM3391 Ethernet switch port devices.

***Note:*** The timing for the PM3371 is identical to the PM3370. Similarly the timing for the PM3391 is identical to the PM3390. Therefore the description for the PM3370 applies to the PM3371, and the description of the PM3390 applies to the PM3391 throughout this document.

### 2.1 EXACT Clock Modes

The EXACT bus supports two modes of operation: the SERDES mode and the Clear Channel mode. The following sections explain the these clocking modes and the way they are used to support system clocking design.

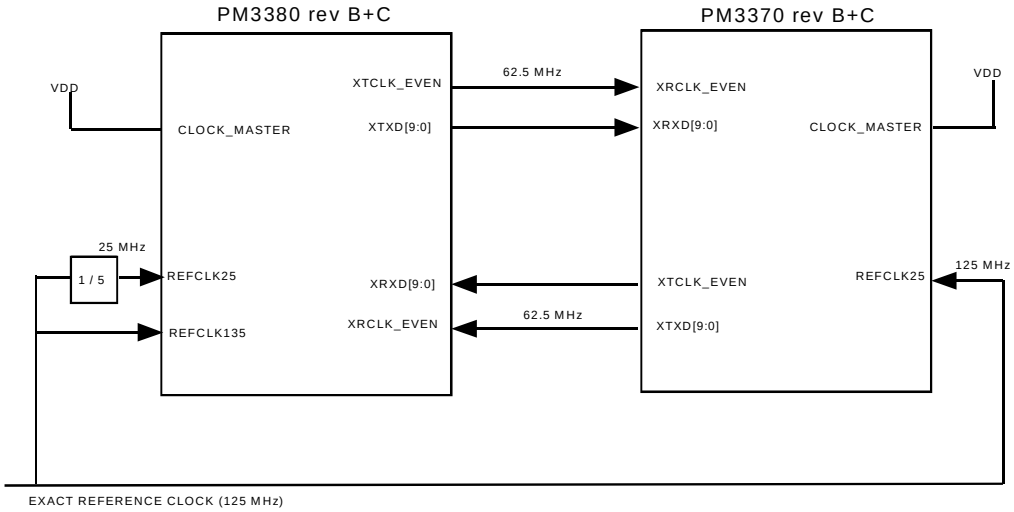
1. **SERDES** – Serializer/de-serializer mode. Typically this mode is used to support stacking between modules to facilitate the transfer of clock and data over moderately electrical distance. Data is encoded in 8B10B linecode and transmitted to the SERDES on every rising edge of a 125MHz transmit clock. Data is received from the SERDES rising edges of complementary receive clocks. The EXACT bus defaults to SERDES mode.

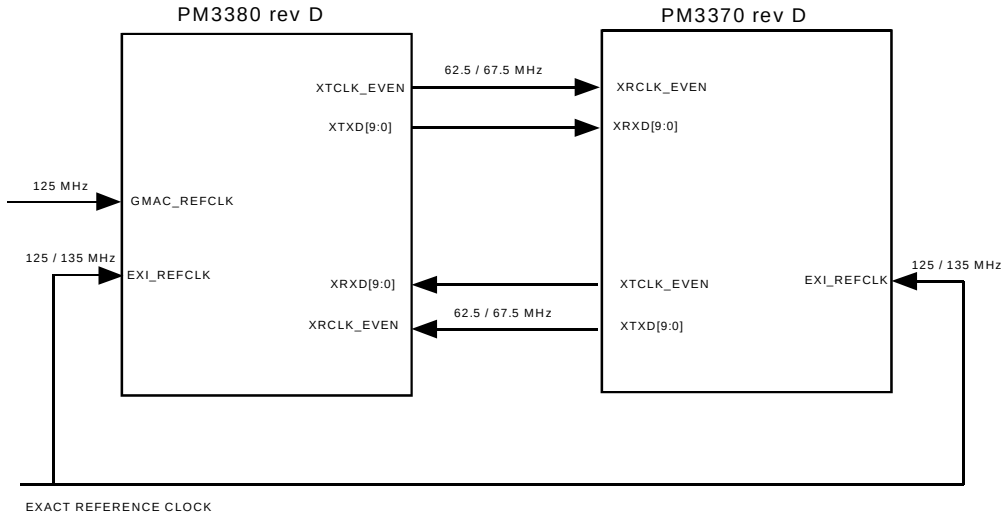
2. **Clear Channel** – Typically this mode is used to support interconnection of EXACT devices in a single EXACT clock domain, such as on one circuit board module. Data bits [7:0] is not encoded, data bit 8 is a control character bit, and bit 9 is the even parity bit. Data is clocked on the rising and falling edges of the transmit and receive clock.

## 2.2 Single Board Applications

In system applications where all chips operate in a single clocking domain such as on a single card, each device uses the same EXACT bus reference clock. The Clear Channel clock mode is used on the EXACT Bus. A local oscillator is used to generate the EXACT bus reference clock. This is conceptually shown in Figure 1 for revisions B, C, and D PM3370 and PM3380 devices. Please see Section 3 for a detail description of clocking connections for revision B, C and D PM3370/3380 devices.

## Figure 1 – EXACT Bus Single Clock Domain Configurations

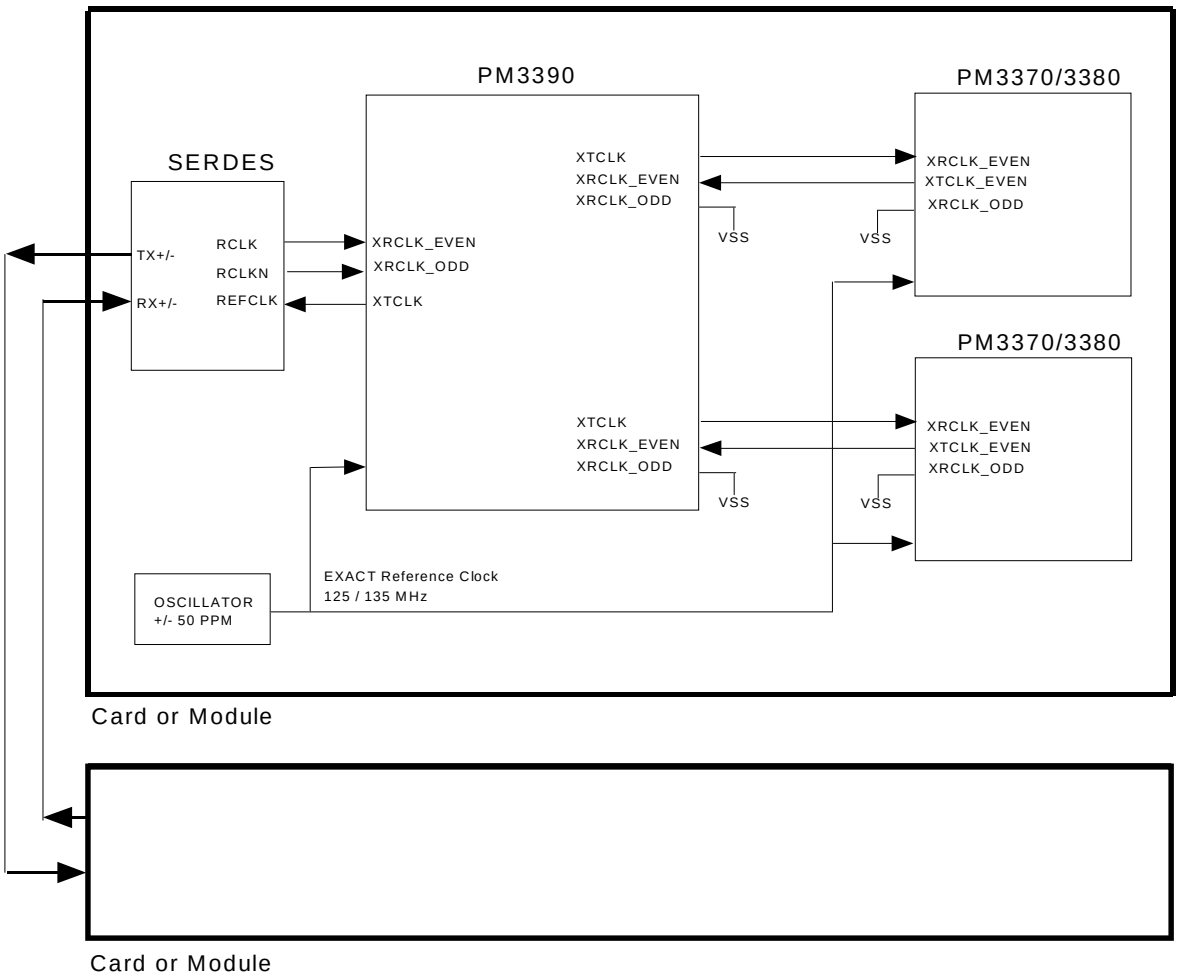


## 2.3 Stacking Applications

In system applications where the EXACT bus needs to span across multiple boards, a SERDES is needed to transfer the EXACT clock and data across boards. Stacking is supported by connecting a SERDES to one of the ports of an PM3390 device. Each board operates in a single EXACT clock domain. The EXACT reference clock on each board is generated by an oscillator. This is conceptually shown in Figure 2.

**Figure 2 – EXACT Bus Stacking Clock Configuration**



# 3. CONFIGURING EXACT DEVICES FOR EXACT BUS CLOCK MODES

This section describes the theory of operation and how to configure the PM3370, PM3380, and PM3390 devices to operate in SERDES and Clear Channel clock modes. The revisions B and C of PM3370 and PM3380 devices can support EXACT reference clock up to 125 MHz only.

## 3.1 Configuring PM3370 / PM3380 Rev B+C Devices

The external clock connections for PM3370 and PM3380 revision B and C devices is shown in Figure 3. In addition the devices are configured by connecting the MCONFIG and DCONFIG words on Memory Interface A and Memory Interface B as described below.

### Configuring SERDES Clock Mode

Following a reset, the PM3380 and PM3370 devices load the MCONFIG and DCONFIG from the external memory interface. The value of the MCONFIG and DCONFIG words are defined by strapping the respective bits of the memory data bus to VDD or VSS via a pull-up/down resistor. Please refer to the device datasheet for a detail description of the function of each control bit.

### DCONFIG Word Format for Memory Interface A

| Device Pin | Register Bit | Function | Value |
|---|---|---|---|
| MDATA_A [31:23] | DCONFIG[15:7] | reserved | 000000000 |
| MDATA_A [22] | DCONFIG[6] | ENTRE | 0 |
| MDATA_A [21:16] | DCONFIG[5:0] | CLKMUX[5:0] | 100100 (for PM3370)<br>000000 (for PM3380) |

### MCONFIG Word Format for Memory Interface A

| Device Pin | Register Bit | Function | Description |
|---|---|---|---|
| MDATA_A [15:9] | MCONFIG[15:9] | reserved | 0000000 |
| MDATA_A [8] | MCONFIG[8] | M2CAS | Not relevant to EXACT clocking. |
| MDATA_A [7:6] | MCONFIG[7:6] | MTYPE3[1:0] | Not relevant to EXACT clocking. |
| MDATA_A [5:4] | MCONFIG[5:4] | MTYPE2[1:0] | Not relevant to EXACT clocking. |
| MDATA_A [3:2] | MCONFIG[3:2] | MTYPE1[1:0] | Not relevant to EXACT clocking. |
| MDATA_A [1:0] | MCONFIG[1:0] | MTYPE0[1:0] | Not relevant to EXACT clocking. |

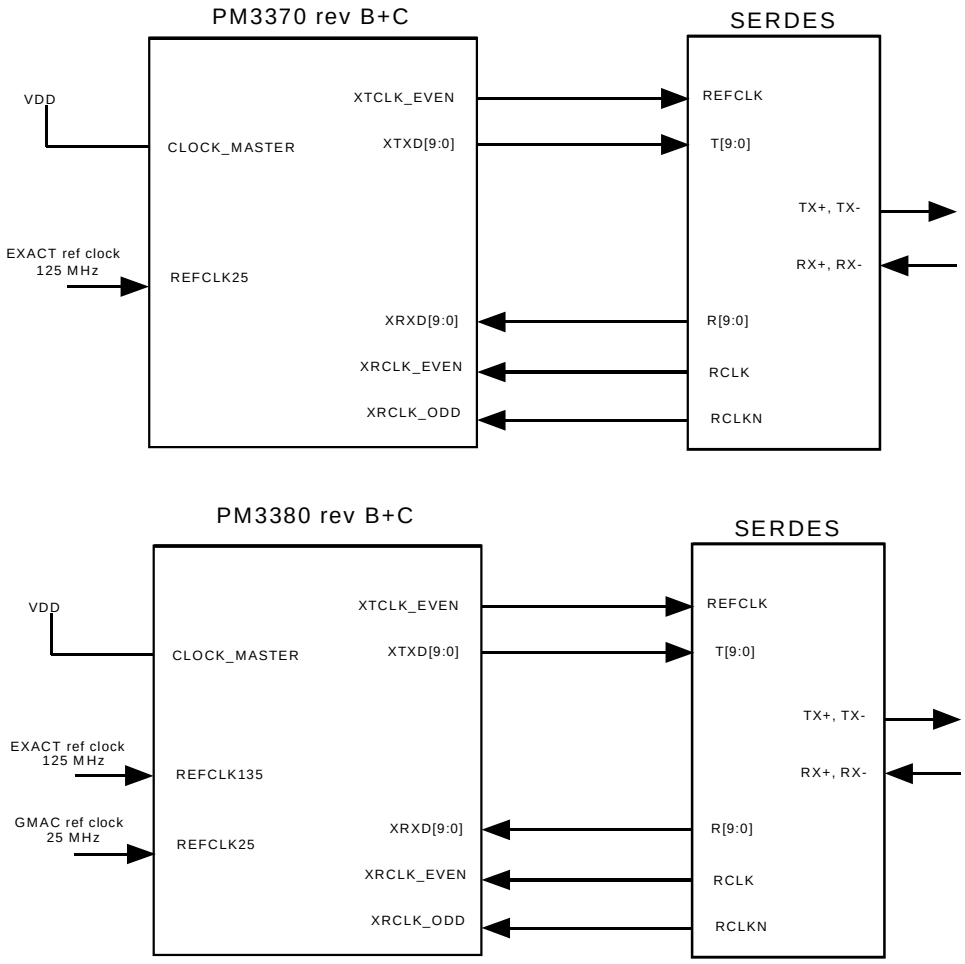
## DCONFIG Word Format for Memory Interface B

| Device Pin | Register Bit | Function | Description |
|---|---|---|---|
| MDATA_B [31:30] | DCONFIG[15:14] | FIRM[1:0] | Not relevant to EXACT clocking. |
| MDATA_B [29] | DCONFIG[13] | RISCHALT | Not relevant to EXACT clocking. |
| MDATA_B [28:23] | DCONFIG[12:7] | CHIPID[5:0] | Not relevant to EXACT clocking |
| MDATA_B [22:16] | DCONFIG[6:0] | RTCDIV[6:0] | Not relevant to EXACT clocking. |

## MCONFIG Word Format for Memory Interface B

| Device Pin | Register Bit | Function | Description |
|---|---|---|---|
| MDATA_B [15] | MCONFIG[15] | RAMDIS | Not relevant to EXACT clocking. |
| MDATA_B [14] | MCONFIG[14] | ROMDIS | Not relevant to EXACT clocking. |
| MDATA_B [13] | MCONFIG[13] | Reserved | 0 |
| MDATA_B [12] | MCONFIG[12] | Reserved | 0 |
| MDATA_B [11] | MCONFIG[11] | EXACTCFG[2] | 0 (for PM3370)<br>1 (for PM3380) |
| MDATA_B [10:9] | MCONFIG[10:9] | EXACTCFG[1:0] | 00 |
| MDATA_B [8] | MCONFIG[8] | M2CAS | Not relevant to EXACT clocking. |
| MDATA_B [7:6] | MCONFIG[7:6] | MTYPE3[1:0] | Not relevant to EXACT clocking. |
| MDATA_B [5:4] | MCONFIG[5:4] | MTYPE2[1:0] | Not relevant to EXACT clocking. |
| MDATA_B [3:2] | MCONFIG[3:2] | MTYPE1[1:0] | Not relevant to EXACT clocking. |
| MDATA_B [1:0] | MCONFIG[1:0] | MTYPE0[1:0] | Not relevant to EXACT clocking. |

## Figure 3 - PM3370 / PM3380 rev B+C connected in SERDES mode



### Configuring Clear Channel Mode

The procedure to configure a PM3370 and PM3380 device to operate in Clear Channel mode is identical to that described for SERDES mode, except that the EXACTCFG[1:0]=10. The connection is shown in Figure 1.

Note that the PM3370/80 rev B+C devices can only support EXACT bus clock up to 125 MHz. In addition the PM3380 rev B+C device uses an internal clock multiplier to generate the required 125 MHz from a 25 MHz clock generated from the125 MHz reference clock.

## 3.2 Configuring PM3370 / PM3380 Revision D Devices

This section describes how to configure Revision D PM3370 and PM3380 devices to operate in SERDES mode and Clear Channel mode. The revision D PM3370/3380 supports up to 135 MHz EXACT reference clock without needing internal clock multiplication.

### Configuring PM3370 / PM3380 rev D in SERDES Mode

Following a reset, the PM3380 and PM3370 devices load the MCONFIG and DCONFIG from the external memory interface. The value of the MCONFIG and DCONFIG words are defined by strapping the respective bits of the memory data bus to VDD or VSS via a pull-up/down resistor. Please refer to the device datasheet for a detail description of the function of each control bit.

## DCONFIG Word Format for Memory Interface A

| Device Pin | Register Bit | Function | Description |
|---|---|---|---|
| MDATA_A [31] | DCONFIG[15] | RAMDIS | Not relevant to EXACT clocking |
| MDATA_A [30] | DCONFIG[14] | ROMDIS | Not relevant to EXACT clocking. |
| MDATA_A [29] | DCONFIG[13] | XRCLKSEL | 0 |
| MDATA_A[28] | DCONFIG[12] | C8B10BN | 0 |
| MDATA_A [27] | DCONFIG[11] | XTCLKSEL | 0 |
| MDATA_A [26] | DCONFIG[10] | EXACT_LPBK | 0 |
| MDATA_A [25:23] | DCONFIG[9:7] | | reserved |
| MDATA_A [22] | DCONFIG[6] | ENTRE | Not relevant to EXACT clocking. |
| MDATA_A [21:16] | DCONFIG[5:0] | | reserved |

## MCONFIG Word Format for Memory Interface A

| Device Pin | Register Bit | Function | Description |
|---|---|---|---|
| MDATA_A [15:0] | MCONFIG[15:0] | | Reserved, or not relevant to EXACT clocking. |

## DCONFIG Word Format for Memory Interface B

| Device Pin | Register Bit | Function | Description |
|---|---|---|---|
| MDATA_B [31:24] | DCONFIG[15:8] | CHIPID[7:0] | Globally unique chip ID used in EXACT bus initialization. |
| MDATA_B [23] | DCONFIG[7] | RISCHALT | Not relevant to EXACT clocking. |
| MDATA_B [22:16] | DCONFIG[6:0] | RTCDIV[6:0] | Not relevant to EXACT clocking. |

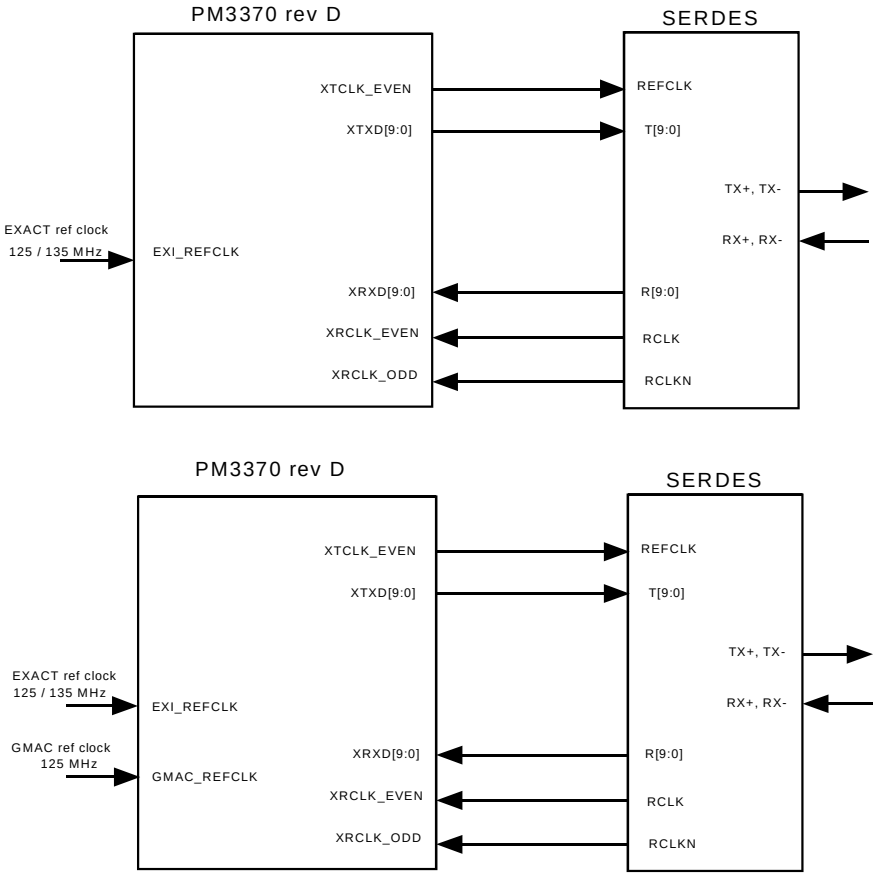
## MCONFIG Word Format for Memory Interface B

| Device Pin | Register Bit | Function | Description |
|---|---|---|---|
| MDATA_B [15:0] | MCONFIG[15:0] | | Reserved or not relevant to EXACT clocking. |

Figure 3 shows how to connect a PM3370 or PM3380 rev D device to operate in SERDES mode. The SERDES device shown in this application is the Vitesse Gigabit Ethernet transceiver (VSC7135).

In SERDES mode, a 125MHz transmit clock (XTCLK_EVEN) that is sampled on the rising edge is sent to the SERDES part. Complementary receive data clocks (XRCLK_EVEN=62.5MHz, XRCLK_ODD=62.5MHz) are provided by the SERDES part, to allow sampling of the incoming data (XRXD[9:0]) on both rising clock edges. The transmit data XTXD[9:0] and receive data XRXD [9:0] is 8B/10B encoded. The 125 MHz ring transmit clock (XTCLK_EVEN) is generated from the input reference clock (EXI_REFCLK).

**Figure 3 - PM3370 / PM3380 rev D connected in SERDES mode**



## Configuring PM3370 / PM3380 rev D in Clear Channel Mode

The MCONFIG and DCONFIG bits are identical to that required for SERDES mode, except bits DCONFIG[11] = XTCLKSEL = 1, DCONFIG[12] = C8B10BN = 1, and DCONFIG[13] = XRCLKSEL = 1.

The connection for a revision D PM3370 and PM3380 device to operate in Clear Channel mode is shown in Figure 1, except that the EXACT bus reference clock is input to the EXI_REFCLK pin, and the CLOCK_MASTER pin is no longer needed.

## 4. EXACT BUS TIMING FOR PM3370 / PM3380

This section provides the timing characteristics and analyzes board level clock skew budget for:

- Revision B+C PM3370 and PM3380 in SERDES and Clear Channel mode

- Revision D PM3370 and PM3380 SERDES and Clear Channel mode

Due to EXACT clock and data delay mismatch in the revision B and rev C PM3370 and PM3380 devices require external delays to be inserted for the EXACT receive and/or transmit clocks. The adjustments and capability are summarized in the following table. The characteristics for interoperating with the PM3390 are still being investigated.

| Operation | Data Rate | Xtclk delay inserted | Xrclk delay inserted | Board skew budget |
|---|---|---|---|---|
| Rev B+C SERDES | 125 MHz | 3 ns | 3 ns | ~ +/- 2 ns in lab condition |
| Rev B+C Non-SERDES | 125 MHz | NA | 3 ns | ~ +/- 2 ns in lab condition |
| Rev D SERDES (HP) | 135 MHz | 0 ns | 0 ns | 0.3 ns sim'ed |
| Rev D Non-SERDES | 135 MHz | 0 ns | 0 ns | 0.5 ns sim'ed |
| Rev D SERDES (HP) | 125 MHz | 0 ns | 0 ns | 0.5 ns sim'ed |
| Rev D Non-SERDES | 125 MHz | 0 ns | 0 ns | 0.5 ns sim'ed |

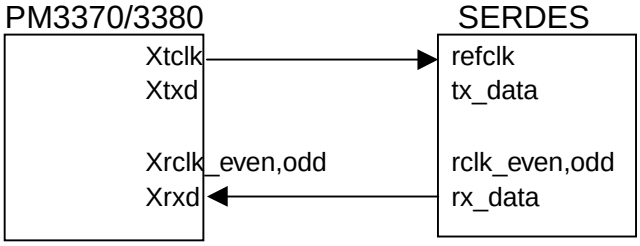
The subsequent analysis assumes a “common” SERDES specification based on the most stringent requirements from the following components:

| | Input to SERDES setup | Input to SERDES hold | Output from SERDES setup | Output from SERDES hold |
|---|---|---|---|---|
| Vitesse | 1.0 | 1.5 | 3.0 | 2.0 |
| Hewlett Packard | 1.5 | 1.0 | 2.5 | 1.5 |
| AMD | 1.5 | 1.0 | 3.0 | 2.0 |
| Common | 1.5 | 1.5 | 2.5 | 1.5 |

## 4.1 PM3370 / PM3380 rev B+C EXACT Timing

Revision B PM3370 and PM3380 devices require external delays to adjust XRCLK and XTCLK due to unmatched clock-data skews in the device. The device can operate in SERDES mode up to 125 MHz data rate in lab condition for SERDES and Clear Channel mode.

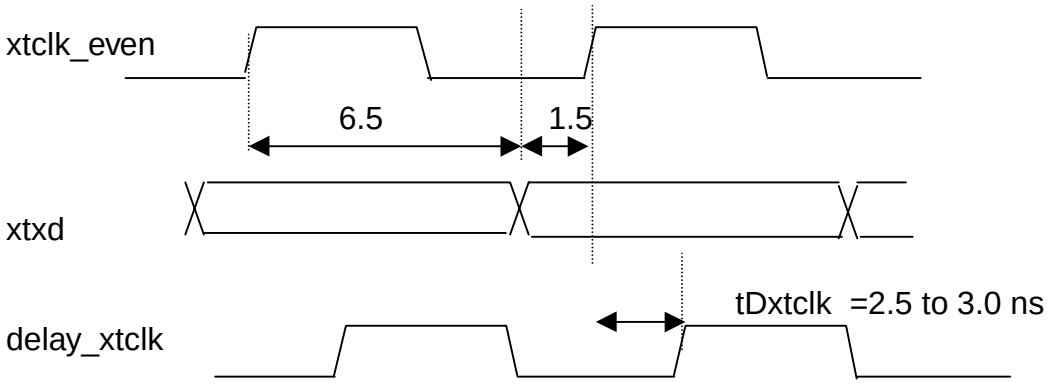
EXACT transmit port is connected to EXACT receive Port as shown below.



## Transmit to SERDES Timing Adjustments

EXACT transmit clock must be delayed by tDxtclk at board level to achieve optimal setup / hold time to interface to SERDES. Since tPxtxd varies with condition, therefore tDxtclk varies with condition. The optimal tDxtclk for lab condition is shown below.

REV B+C Transmit to SERDES In Lab Condition




Choose tDxtclk to maximize board skew budget:

tBS = t(board_skew) = min (tSbs, tHbs)

where

tSbs = t(board_skew_setup)
tHbs = t(board_skew_hold)

Using tDxtclk = 3ns:

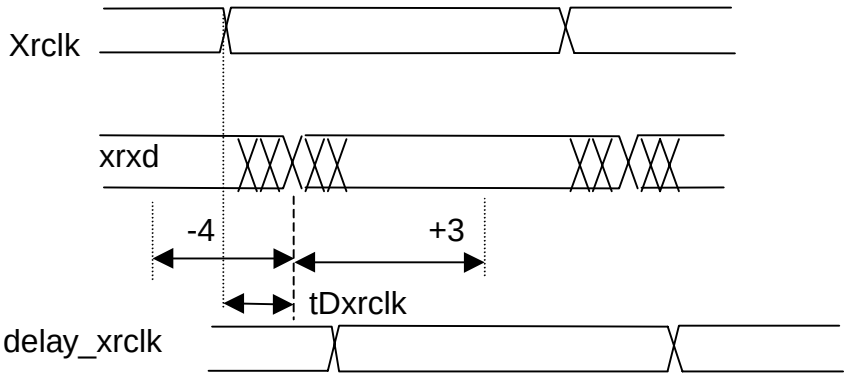
tSbs= T(xtclk) – tPxtxd + tDxtclk - tSserdes = 8.0 - 6.5 + 3.0 -1.5 = 3ns
tHbs= tPxtxd – tHserdes - tDxtclk = 6.5 – 1.5 – 3.0 = 2ns

Hence tDxtclk = 3 ns provides skew budget tBS = 2 ns for transmit to SERDES.

## Receive from SERDES and Clear Channel Timing

EXACT receive clock(s) must be delayed by tDxrclk at board level to achieve optimal setup / hold time and board skew to receive from SERDES.

REV B TX TO SERDES IN LAB CONDITION




The PM337/3380 EXACT input "safe" region is in a region –4 ns and +3 ns centered at the transition of xrxd[9:0]. The optimal placement of xrclk is achieved by delaying xrclk_even and xrclk_odd by delay tDxrclk and place it at the center of the safe region.

For the HP SERDES tDxrclk = 3 ns in lab condition

## 4.2 PM3370 / PM3380 rev D EXACT Interface Timing

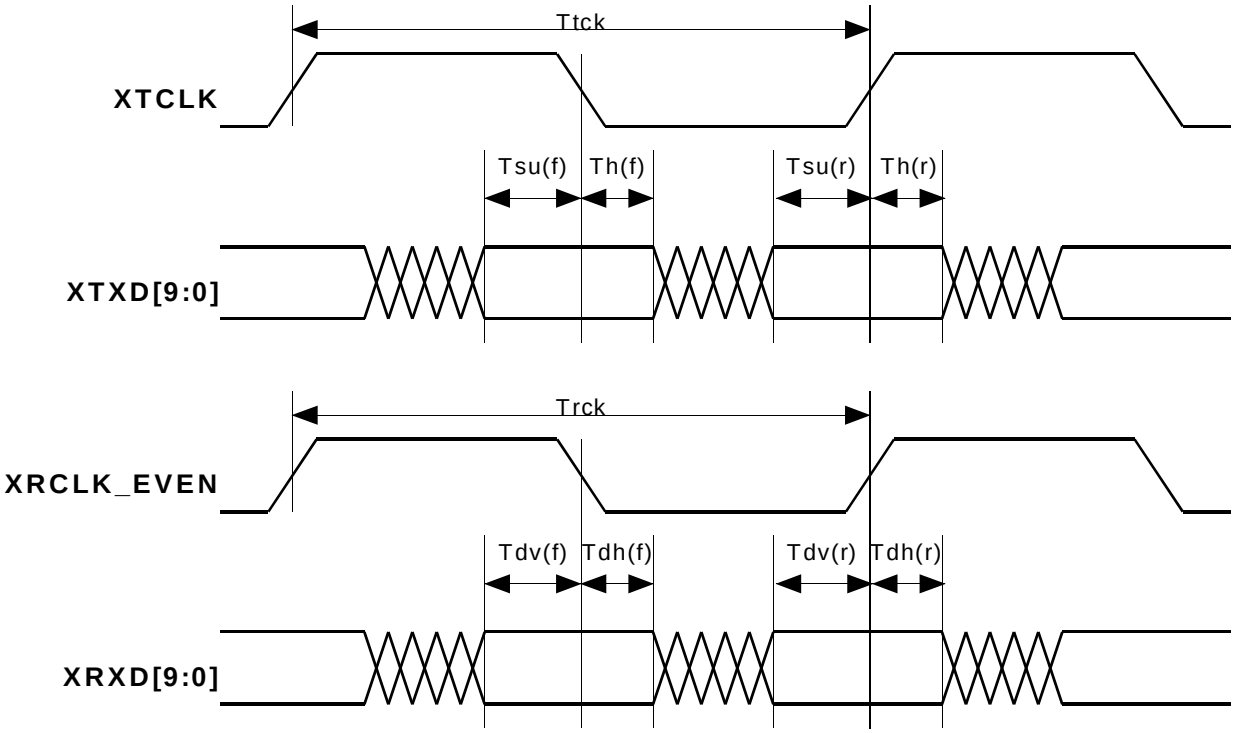
### Timing Characteristics

($T_j$ = -40°C to +125°C, $V_{DD}$ = 3.3 V ±5%)

### Clear Channel mode timing (Load = 30pF)

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{TCK}$ | XTCLK_EVEN Transmit Clock Period | 14.8 | | ns |
| $T_{SU(R)}$ , $T_{SU(F)}$ | Transmit Data Setup Time (valid) Before Edge of XTCLK_EVEN | 1.53 | | ns |
| $T_{H(R)}$ , $T_{H(F)}$ | Transmit Data Hold Time (valid) After Edge of XTCLK_EVEN | 1.76 | | ns |
| $T_{TDC}$ | Transmit Clock Duty Cycle | 40 | 60 | % |
| $T_{RCK}$ | Receive Clock Period of XRCLK_EVEN | 14.8 | | ns |
| $T_{DV(R)}$ , $T_{DV(R)}$ | Receive Data Valid Before Edge of XRCLK_EVEN | 1.0 | - | ns |
| $T_{DH(R)}$ , $T_{DH(R)}$ | Receive Data Hold after Edge of XRCLK_EVEN | 1.0 | - | ns |
| $T_{RDC}$ | Receive Clock Duty Cycle of XRCLK_EVEN | 40 | 60 | % |

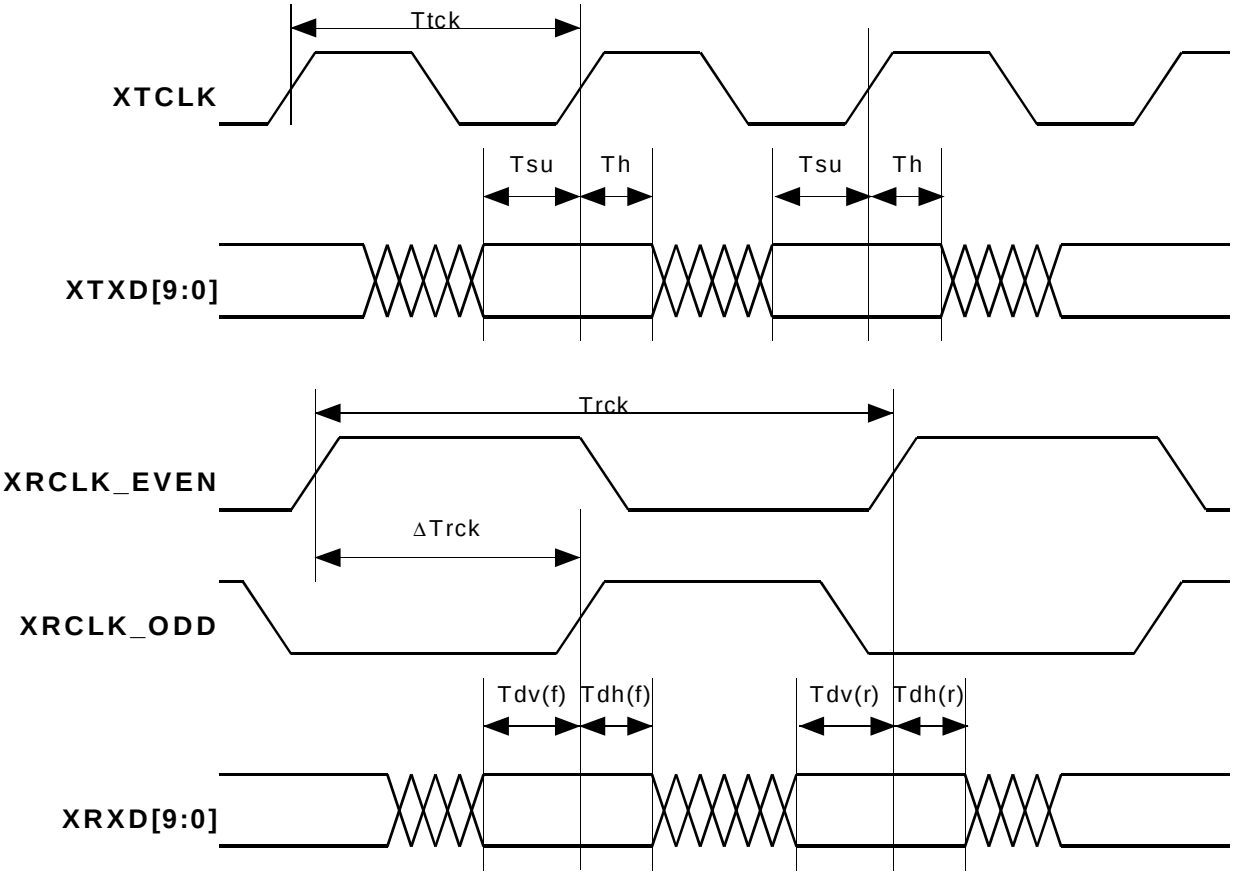
## Clear Channel mode timing



## SERDES mode timing

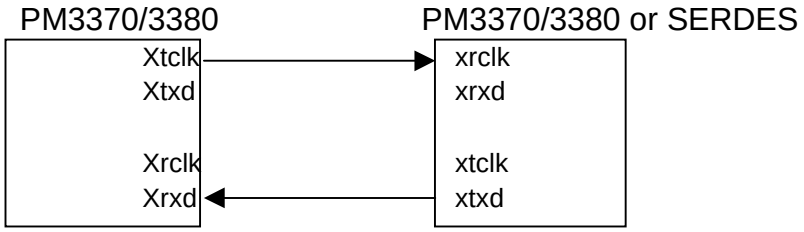
| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{TCK}$ | XTCLK_EVEN Transmit Clock Period | 7.9 | 8.1 | ns |
| $T_{SU}$ | Transmit Data Setup Time (valid) Before XTCLK_EVEN Rising Edge | 2.4 (125 MHz) 1.8 (135 MHz) | - | ns |
| $T_{H}$ | Transmit Data Hold Time (valid) After XTCLK_EVEN Rising Edge | 1.7 | - | ns |
| $T_{TDC}$ | Transmit Clock Duty Cycle | 40 | 60 | % |
| $T_{RCK}$ | Receive Clock Period of XRCLK_EVEN | 15.8 | 16.2 | ns |
| $\Delta T_{RCK}$ | Deviation, XRCLK_EVEN Rise to XRCLK_ODD Rise | -0.5 | +0.5 | ns |
| $T_{DV(R)}$ , $T_{DV(R)}$ | Receive Data Valid Before Edge of XRCLK_EVEN/XRCLK_ODD | 1.0 | - | ns |
| $T_{DH(R)}$ , $T_{DH(R)}$ | Receive Data Hold after Edge of XRCLK_EVEN/XRCLK_ODD | 1.0 | - | ns |
| $T_{RDC}$ | Receive Clock Duty Cycle | 40 | 60 | % |

## SERDES mode timing



## 4.3 PM3370 / PM3380 Rev D EXACT Bus Timing Analysis

EXACT transmit port is connected to EXACT receive port. No external delay is required.




### Worst case SERDES specs for Vitesse, HP, and AMD

The subsequent analysis assumes a “common” SERDES timing specification based on the most stringent timing requirements for the following components:

| part | tS1serdes | tH1serdes | tS2serdes | tH2serdes |
|---|---|---|---|---|
| Vitesse | 1.0 | 1.5 | 3.0 | 2.0 |
| HP | 1.5 | 1.0 | 2.5 | 1.5 |
| AMD | 1.5 | 1.0 | 3.0 | 2.0 |
| Common | 1.5 | 1.5 | 2.5 | 1.5 |

**Note** the timing requirement for a 135 MHz SERDES is assumed to be the same as a 125 MHz SERDES.

## Board Level Skew

Let

tBS = t(board_skew)
tSbs = t(board_skew_setup)
tHbs = t(board_skew_hold)

### *Clear-Channel Mode*

In Clear Channel mode the PM3370/80 devices are connected directly to one another:

tSbs = tSU – tdv = 1.53 – 1.0 = 0.53 ns
tHbs = tH – tdv = 1.76 – 1.0 = 0.76 ns
tBS = min (0.53, 0.76) = 0.53 ns

Hence the allowable board skew in Clear Channel mode = 0.5 ns.

### *SERDES Mode*

In SERDES mode, the timing differs when operating with a 125MHz SERDES or a 135MHz SERDES. Note that the timing specification for a 135MHz SERDES is assumed to be the same as a 125MHz SERDES. The Hewlett Packard SERDES provides marginally more time for board skew.

#### *Output to SERDES at 135 MHz*

tSbs= Tsu – tS1serdes = 1.8 – 1.5 = 0.3 ns (135 MHz)
tHbs= Th – tH1serdes = 1.7 – 1.5 = 0.2 ns (worst case SERDES)
tHbs= Th – tH1serdes = 1.7 – 1.0 = 0.7 ns (HP SERDES)

tBS= min (0.3, 0.2) = 0.2 ns (135M worst case SERDES)
tBS= min (0.3, 0.7) = 0.3 ns (135M with HP SERDES)

### *Output to SERDES at 125 MHz*

tSbs= Tsu – tS1serdes = 2.4 – 1.5 = 0.9 ns (125 MHz)
tHbs= Th – tH1serdes = 1.7 – 1.5 = 0.2 ns (worst case SERDES)
tHbs= Th – tH1serdes = 1.7 – 1.0 = 0.7 ns (HP SERDES)

tBS= min (0.9, 0.2) = 0.2 ns (125M worst case SERDES)
tBS= min (0.9, 0.7) = 0.7 ns (125M with HP SERDES)

### *Input from SERDES at 125/135 MHz*

tSbs = tS2serdes – Tdv = 2.5 – 1.0 = 1.0 ns
tHbs= tT2serdes – tdv = 1.5 – 1.0 = 0.5 ns
tBS= min (1.0, 0.5) = 0.5 ns

If the board level skew budget is the minimum of the skew associated with input and output to the SERDES, then:

1. In Clear Channel mode, board skew = 0.5 ns.

2. In 125MHz SERDES mode, board skew = 0.5 ns using HP SERDES. This is limited by the board skew input from SERDES.

3. In 135MHz SERDES mode, board skew = 0.3 ns using HP SERDES. This is limited by the board skew output to SERDES.

## CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

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