MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14512

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-CHANNEL DATA SELECTOR

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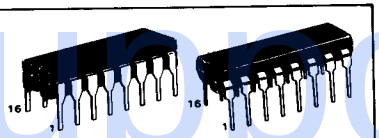
The MC14512 is an 8-channel data selector constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- High Fanout > 50
- Single Supply Operation — Positive or Negative
- 3-State Output (Logic "1", Logic "0", High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

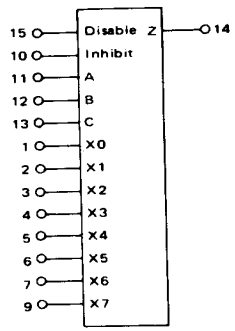
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

C	B	A	INHIBIT	DISABLE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
ϕ	ϕ	ϕ	1	0	0
ϕ	ϕ	ϕ	ϕ	1	High Impedance

ϕ = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device) (V_{OH} = 2.5 Vdc) Source (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0	−0.62	–	−0.50	−1.7	–	−0.35	–	mAdc
		10	−0.62	–	−0.50	−0.9	–	−0.35	–	
		15	−1.8	–	−1.5	−3.5	–	−1.1	–	
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	mAdc
		10	1.1	–	0.90	2.0	–	0.65	–	
		15	4.2	–	3.4	7.8	–	2.4	–	
Output Drive Current (CL/CP Device) (V_{OH} = 2.5 Vdc) Source (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0	−0.23	–	−0.20	−1.7	–	−0.16	–	mAdc
		10	−0.23	–	−0.20	−0.9	–	−0.16	–	
		15	−0.69	–	−0.60	−3.5	–	−0.48	–	
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
		10	0.60	–	0.50	2.0	–	0.40	–	
		15	1.8	–	1.5	7.8	–	1.2	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.8 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.6 µA/kHz) f + I_{DD}							
		15	I_T = (2.4 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

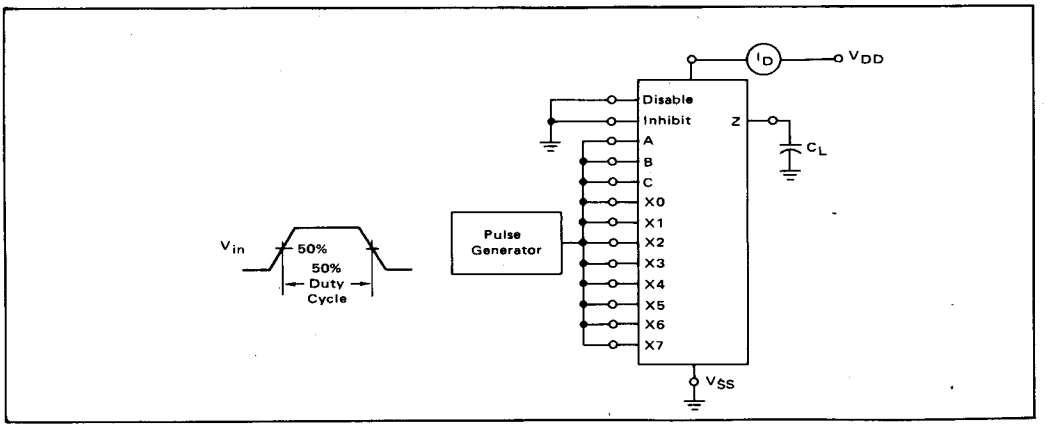
*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Typ	Max		Unit
			All Types	AL Device	CL/CP Device	
Output Rise Time	t_r					ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	70	175	200	
t_r = (1.5 ns/pF) C_L + 12 ns		10	35	75	110	
t_r = (1.1 ns/pF) C_L + 8 ns		15	25	55	80	
Output Fall Time	t_f					ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	70	175	200	
t_f = (0.75 ns/pF) C_L + 24 ns		10	35	75	110	
t_f = (0.55 ns/pF) C_L + 17 ns		15	25	55	80	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (0.9 ns/pF) C_L + 211 ns		5.0	225	500	750	
t_{PLH} = (0.3 ns/pF) C_L + 70 ns		10	75	175	200	
t_{PLH} = (0.23 ns/pF) C_L + 54 ns		15	57	130	150	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (2.7 ns/pF) C_L + 184 ns		5.0	225	500	750	
t_{PHL} = (0.9 ns/pF) C_L + 61 ns		10	75	175	200	
t_{PHL} = (0.68 ns/pF) C_L + 47 ns		15	57	130	150	
3-State Output Delay Times	$t_{"1"H}$, $t_{"0"H}$,	5.0	50	125	150	ns
"1" or "0" to High Z, and	$t_{"H"1}$, $t_{H"0"}$	10	25	75	100	
High Z to "1" or "0"		15	19	60	75	

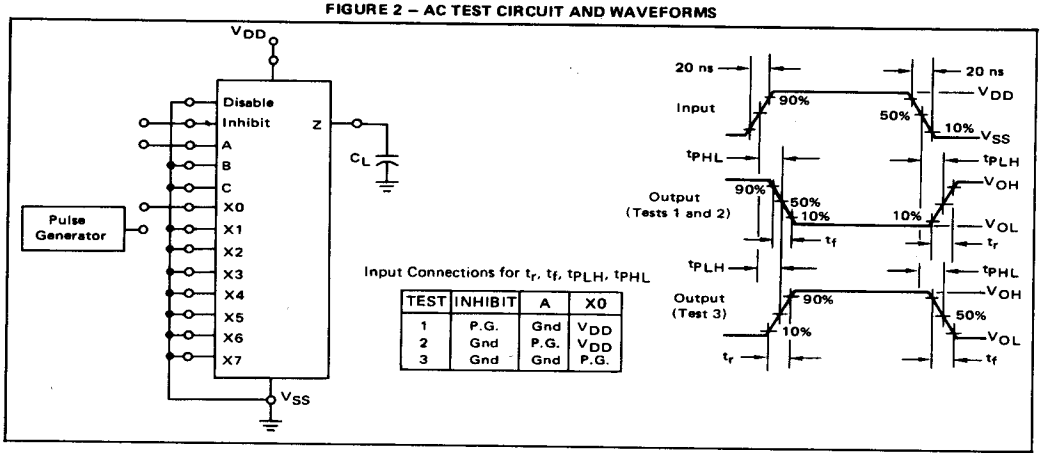
*The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

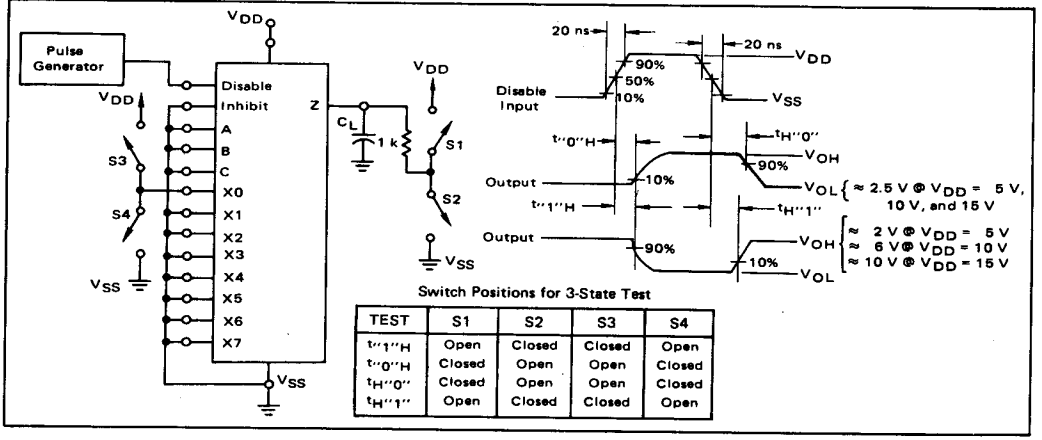
FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



Input Connections for t_r, t_f, t_{PLH}, t_{PHL}

TEST	INHIBIT	A	X0
1	P.G.	Gnd	V_{DD}
2	Gnd	P.G.	V_{DD}
3	Gnd	Gnd	P.G.

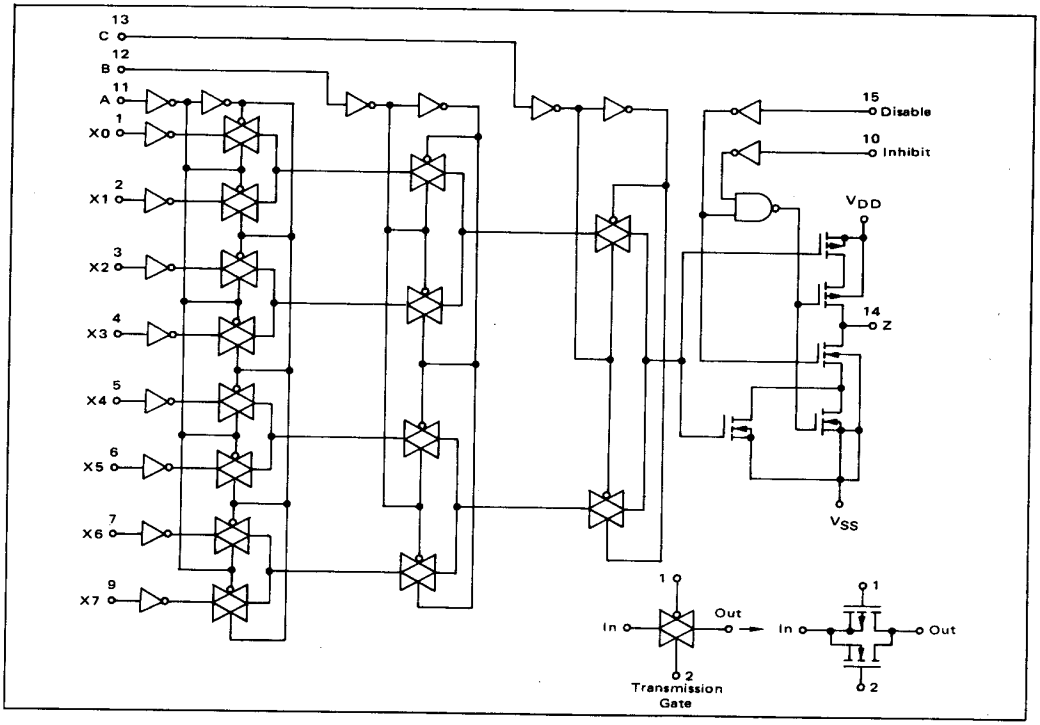
FIGURE 3 – 3-STATE AC TEST CIRCUIT AND WAVEFORM



Switch Positions for 3-State Test

TEST	S1	S2	S3	S4
$t_{r}"1"H$	Open	Closed	Closed	Open
$t_{r}"0"H$	Closed	Open	Open	Closed
$t_{H}"0"$	Closed	Open	Open	Closed
$t_{H}"1"$	Open	Closed	Closed	Open

LOGIC DIAGRAM



3-STATE MODE OF OPERATION

Output terminals of several MC14512 8-Bit Data Selectors can be connected to a single data bus as shown. One MC14512 is selected by the 3-state control, and the remaining devices are disabled into a high impedance "off" state. The number of 8-bit data selectors, N, that may be connected to a bus line is determined from the output drive current, I_{OD}, 3-state or disable output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs), and can be calculated by:

$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic states of the bus line.