

Megohm Center-Tap Chip Resistor



Product may not be to scale

The CTM resistor chips extends the resistance range to 10M in a center tap configuration while keeping the die size relatively small.

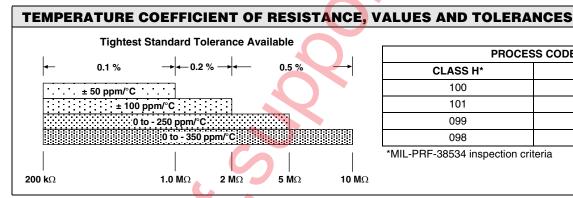
The CTMs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTMs are 100 % electrically tested and visually inspected to MIL-STD-883.

FEATURES

- · Wire bondable
- Resistance range total: 200 k Ω to 10 M Ω
- · Center tap
- Chip size: 0.040 inches square
- · Resistor material: Tantalum nitride, self-passivating
- · Moisture resistant

APPLICATIONS

Vishay EFI CTM tapped megohm resistor chips are designed for hybrid packages requiring high value, two resistor combinations.



PROCESS CODE				
CLASS H*	CLASS K*			
100	130			
101	131			
099	129			
098	128			

*MIL-PRF-38534 inspection criteria

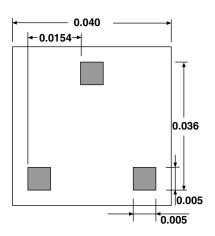
STANDARD ELECTRICAL SPECIFICATIONS				
PARAMETER				
TCR Tracking Between Resistors	± 5 ppm/°C			
Ratio/Ratio, R _A /R _B : Tolerance	1 ± 1 % standard			
Noise	- 12 dB typ.			
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 % max. Δ <i>R/R</i>			
Stability, 1000 h, + 125 °C, 10 mW	± 0.5 % max. absolute ± 0.005 % ratio			
perating Temperature Range - 55 °C to + 125 °C				
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.25 % max. Δ <i>R</i> / <i>R</i>			
High Temperature Exposure, + 150 °C, 100 h	\pm 0.5 % max. $\Delta R/R$			
Dielectric Voltage Breakdown	200 V			
Insulation Resistance	10 ¹² min.			
Operating Voltage	100 V max.			
DC Power Rating at + 70 °C (Derated to Zero at + 175 °C)	20 mW each resistor			
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	± 0.25 % max. Δ <i>R</i> / <i>R</i>			

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Revision: 14-Mar-08

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DIMENSIONS in inches



SCHEMATIC

$$R_{T} = R_{A} + R_{B}$$

$$R_{A} \qquad R_{B}$$

MECHANICAL SPECIFICATIONS in inches				
PARAMETER				
Chip Size	0.040 x 0.040 ± 0.002 (1.02 x 1.02 ± 0.05 mm)			
Chip Thickness	0.010 ± 0.002 (0.254 ± 0.05 mm)			
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO ₂			
Resistor Material	Tantalum nitride, self-passivating			
Bonding Pad Size	0.005 x 0.005 (0.127 x 0.127 mm)			
Number of Pads	3			
Pad Material	10 kÅ minimum aluminum			
Backing	None, lapped semiconductor silicon			

Options: Gold back for eutectic die attach

Custom ratios available up to 4:1 R_A/R_B - consult Vishay EFI Sales

Consult Applications Engineer

ORDERING INFORMATION

W	CTM	101	2000	3	F
INSPECTION/	PRODUCT	PROCESS	RESISTANCE	MULTIPLIER	TOLERANCE
PACKAGING	FAMILY	CODE	VALUE	CODE	CODE
W = 100 % visually inspected		See Process Code	Use first 4 digits	2 = 100	B = 0.1 %
parts in matrix trays per		table	significant digits of the	3 = 1000	C = 0.2 %
MIL-STD-883			resistance (R_{T})	4 = 10 000	D = 0.5 %
X = Sample, visually inspected					F = 1.0 %
parts loaded in matrix					G = 2.0 %
rays (4 % AQL)					H = 2.5 %
,					J = 5.0 %
					K = 10 %

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Vishay

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