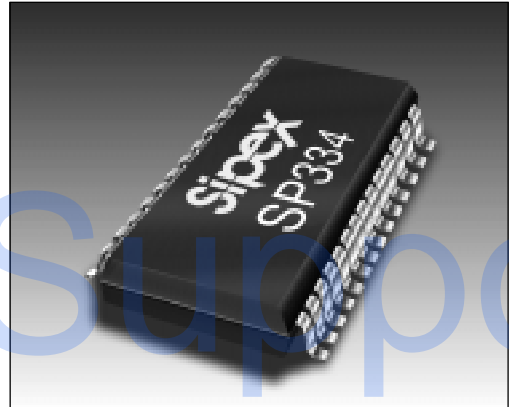


Programmable RS-232/RS-485 Transceiver

- +5V Only Operation
- Software Programmable RS-232 or RS-485 Selection
- Three RS-232 Drivers and Five Receivers in RS-232 Mode
- Two RS-485 Full-Duplex Transceivers in RS-485 Mode
- Full Differential Driver Tri-State (Hi-Z) Control
- Receiver Output Tri-State Control

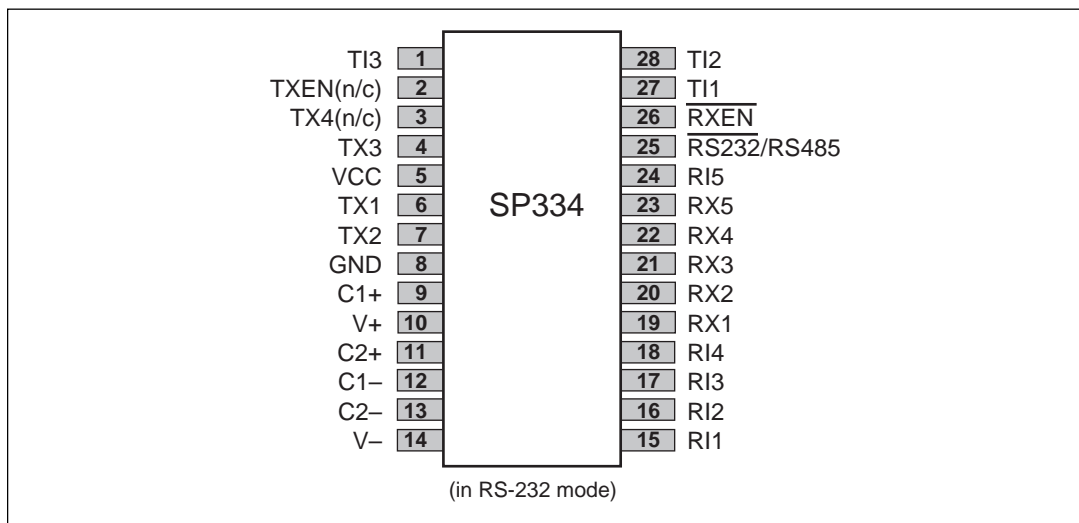


Now available in Lead Free

DESCRIPTION...

The **SP334** is a programmable RS-232 and/or RS-485 transceiver IC. The **SP334** contains three drivers and five receivers when selected in RS-232 mode; and two drivers and two receivers when selected in RS-485 mode.

The RS-232 transceivers can typically operate at 230kbps while adhering to the RS-232 specifications. The RS-485 transceivers can operate up to 10Mbps while adhering to the RS-485 specifications. The RS-485 drivers can be disabled (High-Z output) by the TXEN enable pin. The RS-232 and RS-485 receiver outputs can be disabled by the RXEN enable pin.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V _{CC}	+7V
Storage Temperature.....	-65°C to +150°C
Power Dissipation	
28-pin Plastic DIP.....	1000mW
28-pin Plastic SOIC.....	1000mW

Package Derating:

28-pin Plastic DIP

∅_{JA}.....40°C/W

28-pin Plastic SOIC

∅_{JA}.....40°C/W

SPECIFICATIONS

Typically 25°C @ V_{CC} = +5V unless otherwise noted.

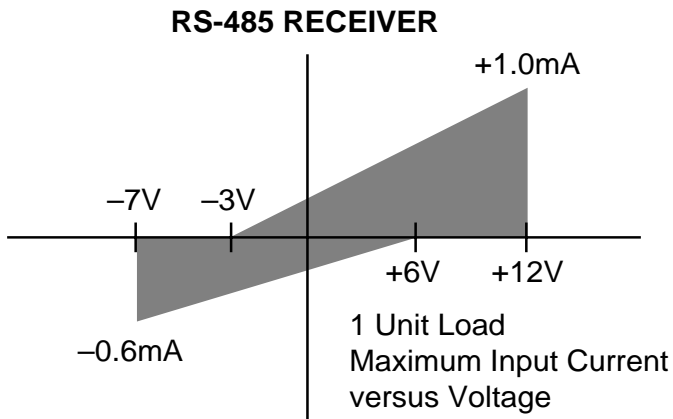
	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS					
V _{IL}			0.8	Volts	
V _{IH}	2.0			Volts	
LOGIC OUTPUTS					
V _{OL}			0.4	Volts	I _{OUT} = -3.2mA I _{OUT} = 1.0mA 0.4V ≤ V _{OUT} ≤ +2.4V
V _{OH}	2.4			Volts	
Output Tri-state Leakage		10		μA	
RS-232 DRIVER					
DC Characteristics					
HIGH Level Output	+5.0		+15	Volts	R _L =3kΩ, V _{IN} =0.8V
LOW Level Output	-15.0		-5.0	Volts	R _L =3kΩ, V _{IN} =2.0V
Open Circuit Voltage	-15		+15	Volts	
Short Circuit Current			±100	mA	V _{OUT} = 0V
Power Off Impedance	300			Ω	V _{CC} = 0V, V _{out} = ±2.0V
AC Characteristics					
Slew Rate			30	V/μs	R _L =3kΩ, C _L = 50pF V _{CC} = +5.0V, T _A @ +25°C
Transition Time			1.56	μs	R _L =3kΩ, C _L =2500pF ; between ±3V, T _A @ +25°C
Maximum Data Rate	120	235		kbps	R _L =3kΩ, C _L =2500pF
Propagation Delay					
t _{PHL}		2	8	μs	Measured from 1.5V of V _{IN} to 50% of V _{OUT} ; R _L =3kΩ
t _{PLH}		2	8	μs	
RS-232 RECEIVER					
DC Characteristics					
HIGH Threshold		1.7	3.0	Volts	V _{IN} = +15V to -15V
LOW Threshold	0.8	1.2		Volts	
Receiver Open Circuit Bias			+2.0	Volts	
Input Impedance	3	5	7	kΩ	
AC Characteristics					
Maximum Data Rate	120	235		kbps	
Propagation Delay					
t _{PHL}		0.25	1	μs	Measured from 50% of V _{IN} to 1.5V of V _{OUT} .
t _{PLH}		0.25	1	μs	
RS-485 DRIVER					
DC Characteristics					
Open Circuit Voltage			6.0	Volts	R _L =54Ω, C _L =50pF
Differential Output	1.5		5.0	Volts	

SPECIFICATIONS

Typically 25°C @ V_{CC} = +5V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-485 DRIVER Balance Common-Mode Output Output Current Short Circuit Current AC Characteristics Maximum Data Rate Output Transition Time Propagation Delay t_{PHL} t_{PLH} Driver Output Skew	28.0		±0.2 3.0 ±250	Volts Volts mA mA	$ V_{-} - V_{+} $ $R_L=54\Omega$ Terminated in -7V to +10V $R_L=54\Omega$ Rise/fall time, 10%-90% See Figures 3A & 5 $R_{DIFF}=54\Omega, C_{L1}=C_{L2}=100pF$ $R_{DIFF}=54\Omega, C_{L1}=C_{L2}=100pF$ per figure 5, $t_{SKEW} = t_{DPLH} - t_{DPLH} $
RS-485 RECEIVER DC Characteristics Inputs Common Mode Range Receiver Sensitivity Input Impedance AC Characteristics Maximum Data Rate Propagation Delay t_{PHL} t_{PLH} Differential Receiver Skew	-7.0 12	 15	 +12.0 ±0.2 10 130 130 10	Volts Volts kΩ Mbps ns ns ns	$-7V \leq V_{CM} \leq +12V$ $-7V \leq V_{CM} \leq +12V$ See Figures 3A & 7 $R_{DIFF}=54\Omega, C_{L1}=C_{L2}=100pF$ $R_{DIFF}=54\Omega, C_{L1}=C_{L2}=100pF$ $t_{SKEW} = t_{PLH} - t_{PHL} ; R_{DIFF}=54\Omega,$ $C_{L1}=C_{L2}=100pF, \text{ see Figure 8}$
ENABLE TIMING RS-485 Driver Enable Time Enable to Low Enable to High Disable Time Disable From Low Disable From High RS-485 Receiver Enable Time Enable to Low Enable to High Disable Time Disable From Low Disable From High					See Figures 4 & 6 $C_L=15pF, S_1 \text{ Closed}$ $C_L=15pF, S_2 \text{ Closed}$ See Figures 4 & 6 $C_L=15pF, S_1 \text{ Closed}$ $C_L=15pF, S_2 \text{ Closed}$ See Figures 2 & 8 $C_L=15pF, S_1 \text{ Closed}$ $C_L=15pF, S_2 \text{ Closed}$ See Figures 2 & 8 $C_L=15pF, S_1 \text{ Closed}$ $C_L=15pF, S_2 \text{ Closed}$
POWER REQUIREMENTS Supply Voltage V _{CC} Supply Current I _{CC} No Load (T _x Disabled) No Load (RS-232 Mode) No Load (RS-485 Mode)	+4.75		+5.25	Volts mA mA mA	TXEN = 0V RS232/RS485 = 0V RS232/RS485 = +5V
ENVIRONMENTAL Operating Temperature Commercial (.C..) Industrial (.E..) Storage Temperature	0 -40 -65		+70 +85 +150	°C °C °C	

RECEIVER INPUT GRAPH



TEST CIRCUITS

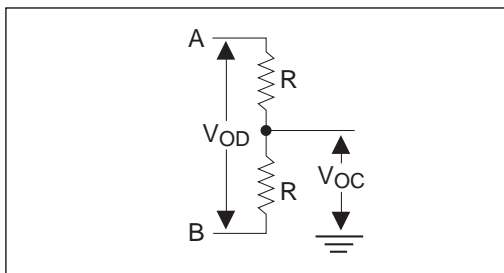


Figure 1. Driver DC Test Load Circuit

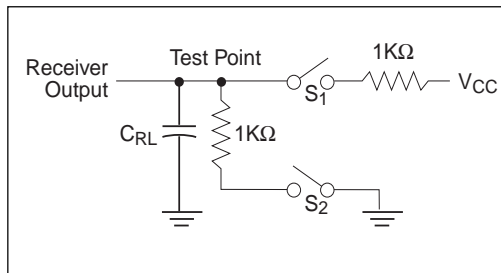


Figure 2. Receiver Timing Test Load Circuit

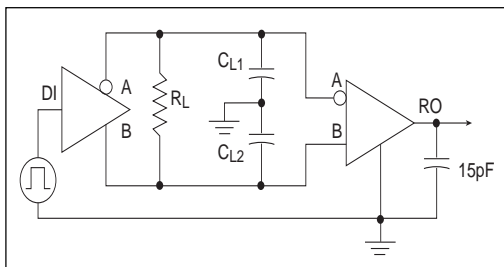


Figure 3a. Driver/Receiver Timing Test Circuit

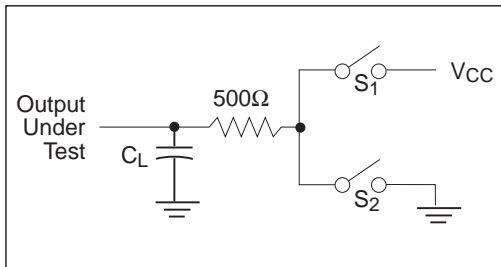


Figure 4. Driver Timing Test Load #2 Circuit

SWITCHING WAVEFORMS

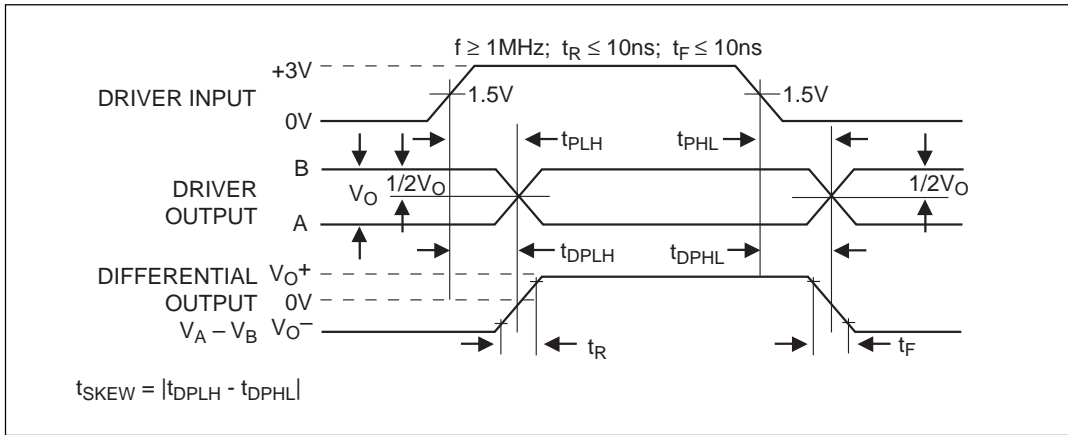


Figure 5. Driver Propagation Delays

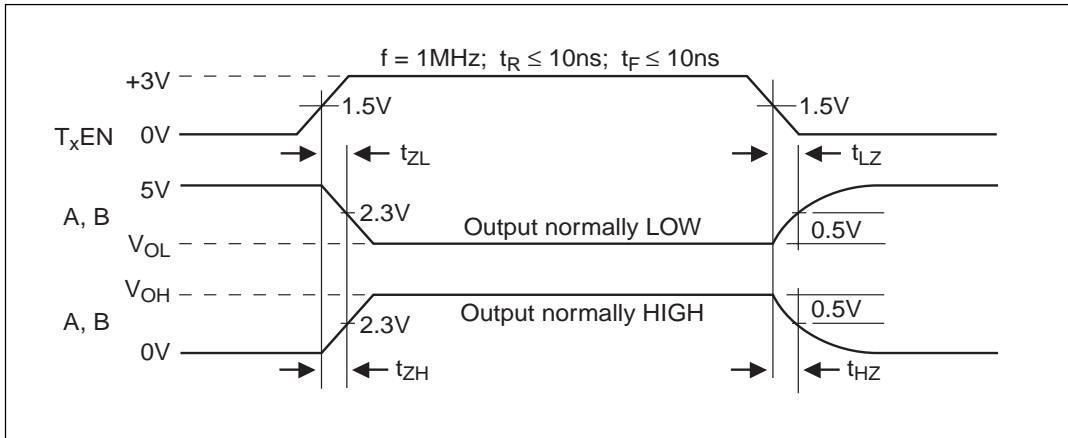


Figure 6. Driver Enable and Disable Times

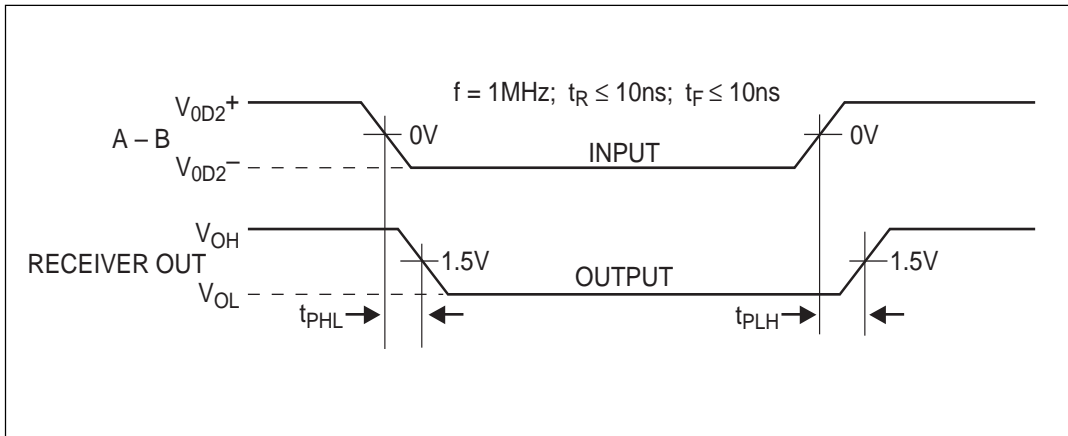


Figure 7. Receiver Propagation Delays

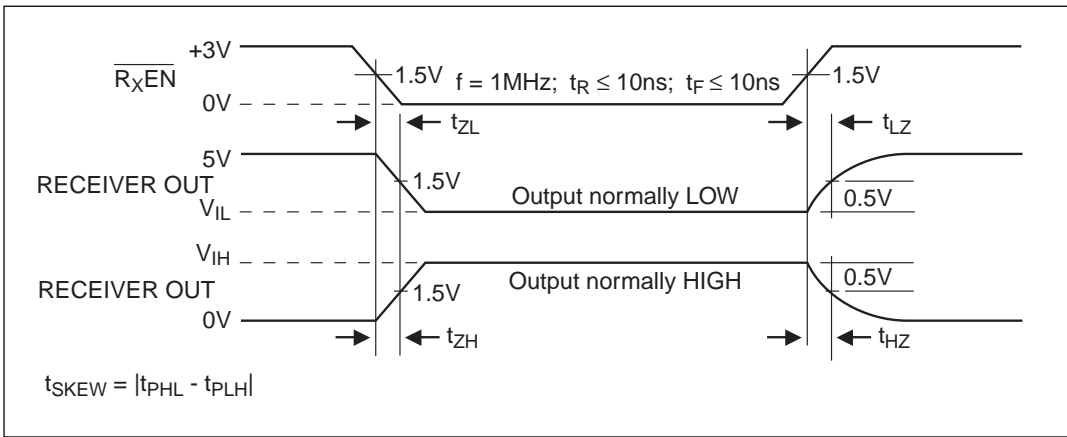


Figure 8. Receiver Enable and Disable Times

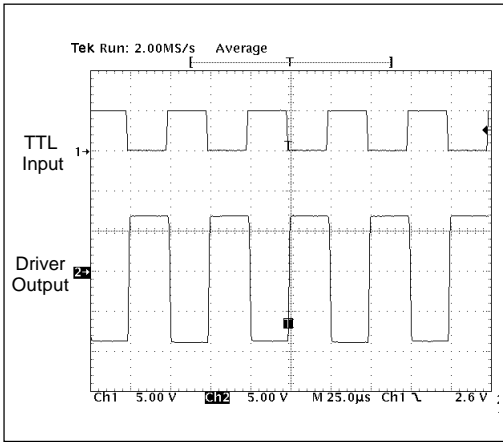


Figure 9. Typical RS-232 Driver Output

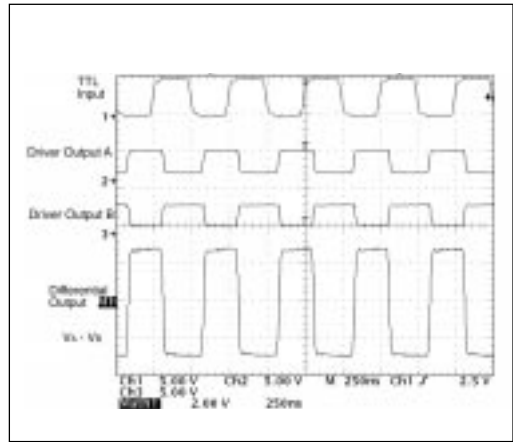


Figure 10. Typical RS-485 Driver Output

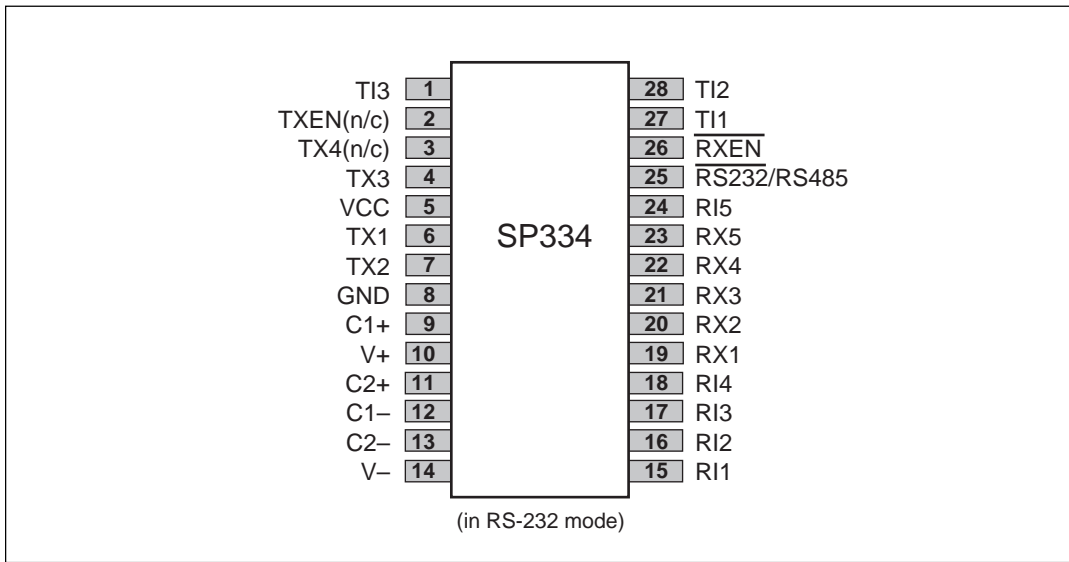


Figure 11. SP334 Pinout

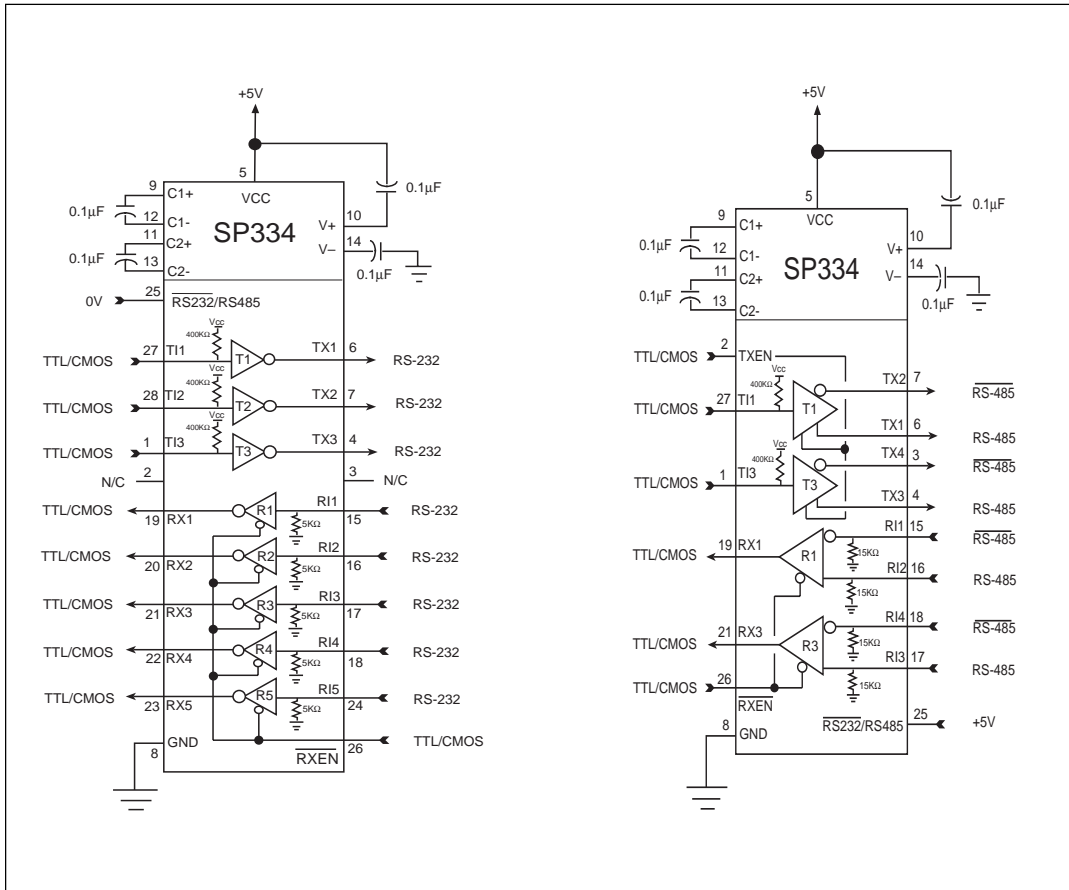


Figure 12. Typical Operating Circuit

THEORY OF OPERATION

The **SP334** is made up of four separate circuit blocks — the charge pump, drivers, receivers, and decoder. Each of these circuit blocks is described in more detail below.

Charge-Pump

The charge pump is a **Sipex**-patented design (U.S. 5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 10V power supplies. Figure 17(a) shows the waveform found on the positive side of capacitor C₂, and figure 17(b) shows the negative side of capacitor C₂. There is a free-running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C₁ and C₂ are initially charged to +5V. C₁⁺ is then switched to ground and charge on C₁⁻ is transferred to C₂⁻. Since C₂⁺ is connected to +5V, the voltage potential across capacitor C₂ is now 10V.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C₂ to the V_{SS} storage capacitor and the positive terminal of C₂ to ground, and transfers the generated -10V to C₃. Simultaneously, the positive side of capacitor C₁ is switched to +5V and the negative side is connected to ground.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C₁ produces -5V in the negative terminal of C₁, which is applied to the negative side of capacitor C₂. Since C₂⁺ is at +5V, the voltage potential across C₂ is 10V.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C₂ to ground and transfers the generated 10V across C₂ to C₄, the V_{DD} storage capacitor. Again, simultaneously with this, the positive side of

capacitor C₁ is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V⁺ and V⁻ are separately generated from V_{CC} in a no-load condition, V⁺ and V⁻ will be symmetrical. Older charge pump approaches that generate V⁻ from V⁺ will show a decrease in the magnitude of V⁻ compared to V⁺ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors must be a minimum of 0.1μF with a 16V breakdown rating.

External Power Supplies

For applications that do not require +5V only, external supplies can be applied at the V⁺ and V⁻ pins. The value of the external supply voltages must be no greater than ±10V. The current drain for the ±10V supplies is used for RS232. For the RS-232 driver the current requirement will be 3.5mA per driver. The external power supplies should provide a power supply sequence of +10V, then +5V, followed by -10V.

Drivers

The **SP334** has three independent RS-232 single-ended drivers and two differential RS-485 drivers. Control for the mode selection is done by the $\overline{\text{RS-232/RS-485}}$ select pin. The drivers are pre-arranged such that for each mode of

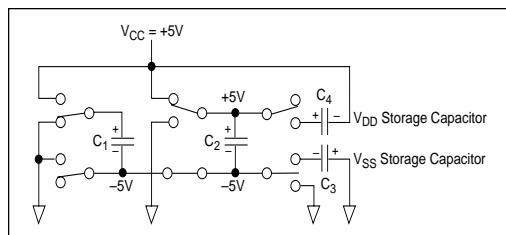


Figure 13. Charge Pump Phase 1.

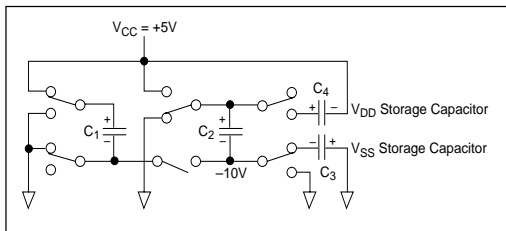


Figure 14a. Charge Pump Phase 2.

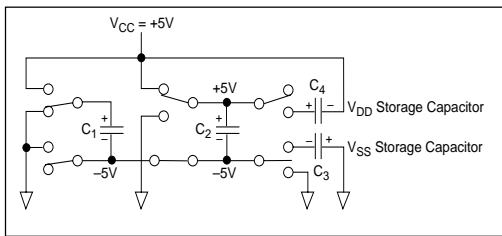


Figure 15. Charge Pump Phase 3.

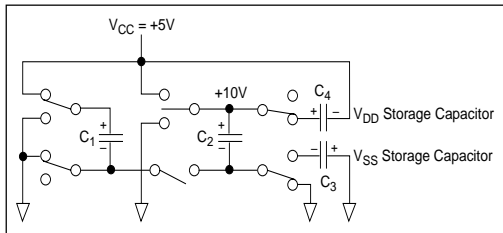


Figure 16. Charge Pump Phase 4.

operation the relative position and functionality of the drivers are set up to accommodate the selected interface mode. As the mode of the drivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line signal levels. Unused driver inputs can be left floating; however, to ensure a desired state with no input signal, pull-up resistors to +5V or pull-down resistors to ground are suggested. Since the driver inputs are both TTL or CMOS compatible, any value resistor less than 100kΩ will suffice.

When in RS-232 mode, the single-ended RS-232 drivers produce compliant RS-232E and ITU V.28 signals. Each of the three drivers output single-ended bipolar signals in excess of

±5V with a full load of 3kΩ and 2500pF applied as specified. These drivers can also operate at least 120kbps.

When programmed to RS-485 mode, the differential RS-485 drivers produce compliant RS-485 signals. Each RS-485 driver outputs a unipolar signal on each output pin with a magnitude of at least 1.5V while loaded with a worst case of 54Ω between the driver's two output pins. The signal levels and drive capability of the RS-485 drivers allow the drivers to also comply with RS-422 levels. The transmission rate for the differential drivers is 10Mbps.

Receivers

The SP334 has five single-ended receivers when programmed for RS-232 mode and two differential receivers when programmed for RS-485 mode.

Control for the mode selection is done by the same select pin as the drivers. As the operating mode of the receivers is changed, the electrical characteristics will change to support the requirements of the appropriate serial standard. Unused receiver inputs can be left floating without causing oscillation. To ensure a desired state of the receiver output, a pull-up resistor of 100kΩ to +5V should be connected to the inverting input for a logic low, or the non-inverting input for a logic high. For single-ended receivers, a pull-down resistor to ground of 5kΩ is internally connected, which will ensure a logic high output.

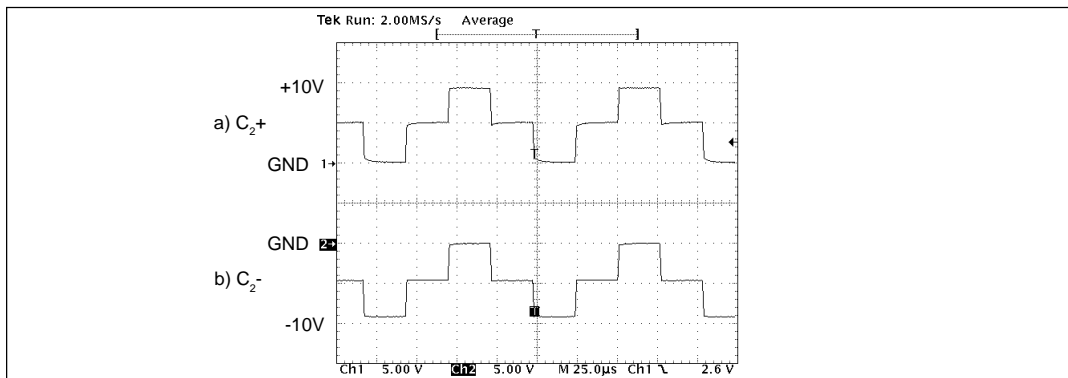
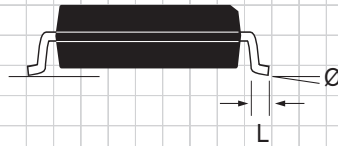
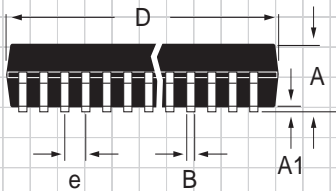
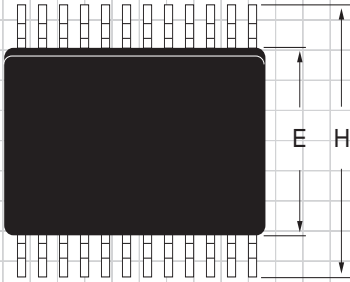


Figure 17. Charge Pump Waveforms

**PACKAGE: 28-PIN PLASTIC
SMALL OUTLINE (SOIC)**



DIMENSIONS (Inches) Minimum/Maximum (mm)	28-PIN
A	0.093/0.104 (2.352/2.649)
A1	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)
D	0.698/0.706 (17.73/17.93)
E	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP334CT	0°C to +70°C	28-pin Plastic SOIC
SP334ET	-40°C to +85°C	28-pin Plastic SOIC

Please consult the factory for pricing and availability on a Tape-On-Reel option.

Now available in Lead Free. To order add "-L" to the part number.
Example: SP488A = normal, SP488A-L = Lead free



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