Implement 3.3Vdual using AIC1521 and AIC1117 for PCI Supply on IAPC Motherboard

Stanley Chen

Introduction

Today, PCs need to remain constantly connected to the outside world, but at the same time consume minimum power. Even looking "idle", it is still possible to receive a message from the Internet or an incoming fax or a phone call. The PC must go from "sleep" mode to "on" mode automatically, that is, an Instantly Available PC (IAPC)

An IAPC appears to be "off", but it can come back to its full ready state within a couple of seconds and respond to the waking-up in time and service the request. In order to meet these requirements, the ACPI (Advanced Configuration and Power Interface) has been defined by Intel, Microsoft, and Toshiba.

The "sleep" state of an IAPC is called "Suspend to RAM", also means the state of S3. This is implemented by utilizing:

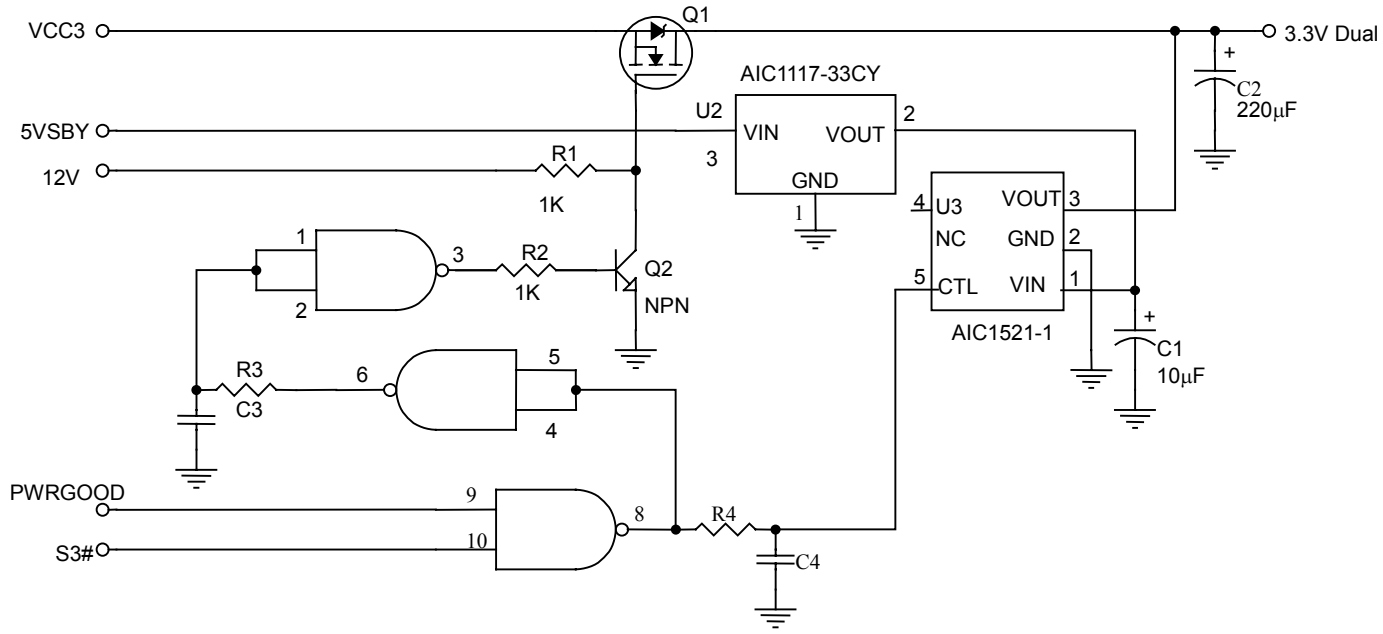
- ✓ Split power planes in the system design
- ✓ An auxiliary power sources (V_{AUX}) for dual mode power distribution.

However, as the PCI 2.2 fully supports the ACPI power management, a new additional signal was defined as a power source. Which delivers power to the PCI add-in card for generation of power management events when the main power to the card has been turned off by software, that is, $3.3V_{DUAL}$ (pin #A14)

Operation Description

The $3.3V_{DUAL}$ output is intended to power subsystem such as the computer's PCI (Peripheral Component Interconnect) slot. $3.3V_{DUAL}$ is generated by two parts, one from V_{CC3}, and the other from $5V_{SBY}$. Which is shown in figure 1.

When main power V_{CC3} is provided, the MOSFET Q1 is turned on as a switch, so that input and output are connected. When main power not provided, the power switch AIC1521 is controlled by control logic, then connecting the AIC1117 LDO output, which is generating regulated 3.3V, as an output, from $5V_{SBY}$. The MOSFET Q1 must be connected as shown in the figure 1 that is to avoid back-feed.



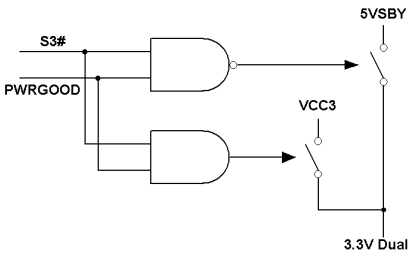
- R3=6.2kΩ , R4=100kΩ , C3=0.1µF , C4=0.001µF
- AIC1117-33 = SOT-223 package
- AIC1521-1 = SOT-89-5

Figure 1. AIC1117 + AIC1521 IAPC 3.3Vdual for MB solution

The state of the switches is controlled by the S3# and PWRGOOD (PWR_OK) lines. Figure 2 below illustrates a simplified block diagram with the truth table in table 1.

0	1	Both
1	0	$5V_{SBY}$
1	1	V_{CC3}

Table 1 The 3.3Vdual output truth table



S3#	PWRGOOD	$3.3V_{DUAL}$ from
0	0	$5V_{SBY}$

ATX timing

To speak of the power sources for MB, the ATX power is currently the mainstream in PC industry.

According to ATX specification 2.03, the Time of PS_ON, PWR_OK, and Germane voltage rails should be as figure 3 below:

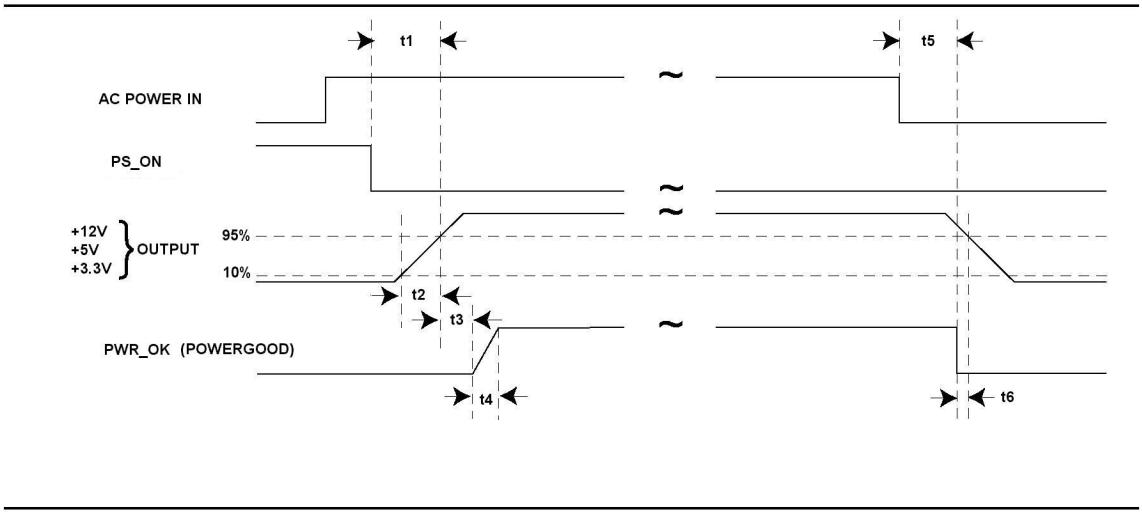


Figure 3 Power Supply Timing

Time	Description	Typical value
t1	Power on time	＜500ms
t2	Rise time	0.1ms＜t2＜20ms
t3	Power OK delay	100ms＜t3＜500ms
t4	Power OK rise time	T4＜10ms
t5	AC loss to PWR_OK hold-up time	T5＞16 ms
t6	Power-down warning	t6＞1ms

t3 is the time which the 3.3V、5V and 12V are above the under voltage threshold (usually 95%). And PWR-OK is pulled high after t3. t6 is the time which PWR_OK is pulled low before 3.3V、5V and 12V falls below its under voltage threshold .

The power OK delay should be less than 500ms and power OK hold-up time more than 16ms for all of the SPS powers. Basically, those are the most important parameters for $3.3V_{DUAL}$ output switched between 2 sources.

Figure 4 shows once the system wakes up from sleeping (S3) state, the PS_ON is pulled low so that the DC output rises after a period of time, that is, power-on time.

The following two figures show the relationship between DC output and PS_ON :

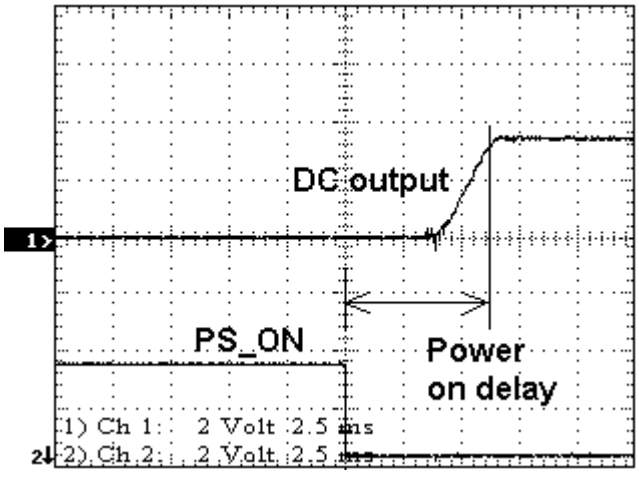


Figure 4 From S3 to S0

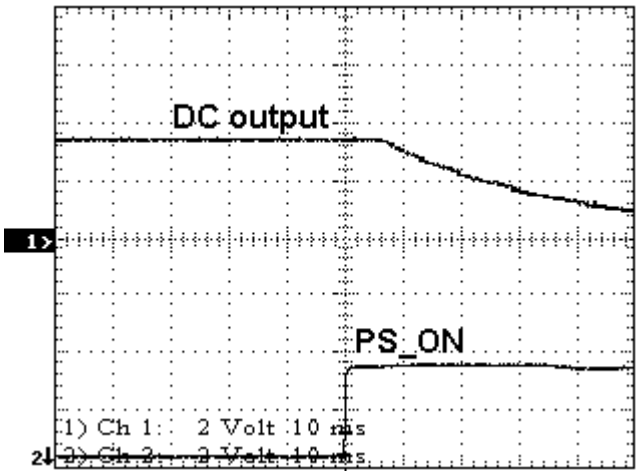


Figure 5 From S0 to S3

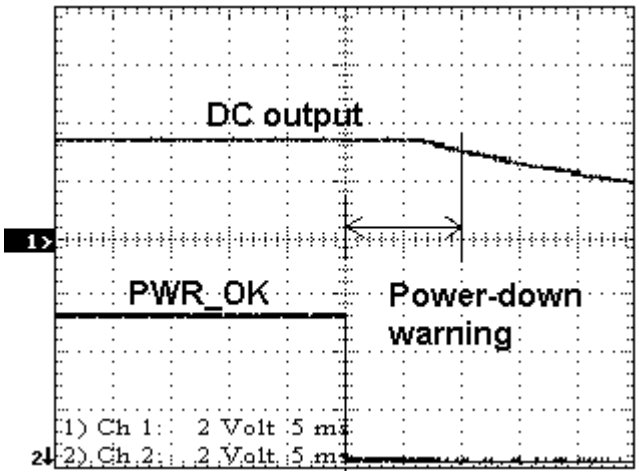


Figure 7 From S0 to S3

After a while, the PWR_OK rises to logic high that is to indicate the power status of DC output. The power OK delay is to ensure the stability of DC output quality. Note that an important parameter, called Power-down warning, is to pull the PWR_OK low before the failure of DC output, as shown in the two figures below:

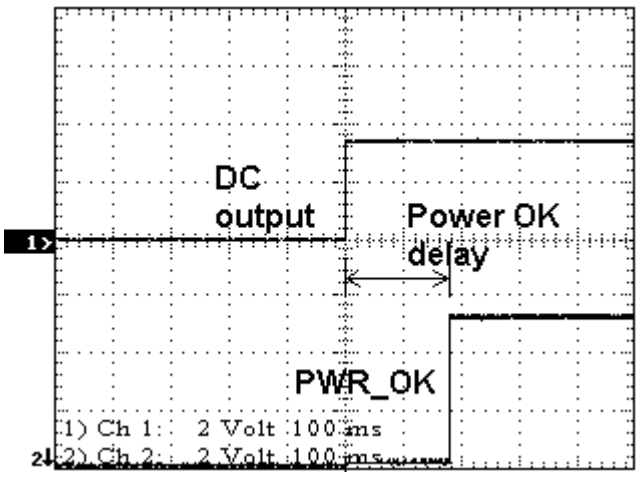


Figure 6 From S3 to S0

IAPC Application

The AIC1521-1 implemented here is a 500mA-power switch, which is originally used as an integrated high-side power switch for self-powered and bus-powered USB application. Now it's implemented as a pure switch due to its continuous 800mA current guaranteed for switching the 3.3V LDO output, which is considered as one of the sources of the 3.3Vdual output application in motherboard (IAPC function). However, the AIC1117 implemented here is quite a widespread used LDO in industry, which provides 800mA continuous output current with low dropout and fast transient response.

R3,C3,R4, and C4 form a delay function, which causes an overlap between two sources. When one source switches to the other the unacceptable drop by the switching would no longer exist, even smaller output capacitor attached.

Figure 8 and Figure 9 show the transit from S3 to S0 with 700us delay (R4,C4) and from S0 to S3 with 1ms delay (R3,C3) transitions, respectively, for 300mA output current from an active load (Chroma 63010).

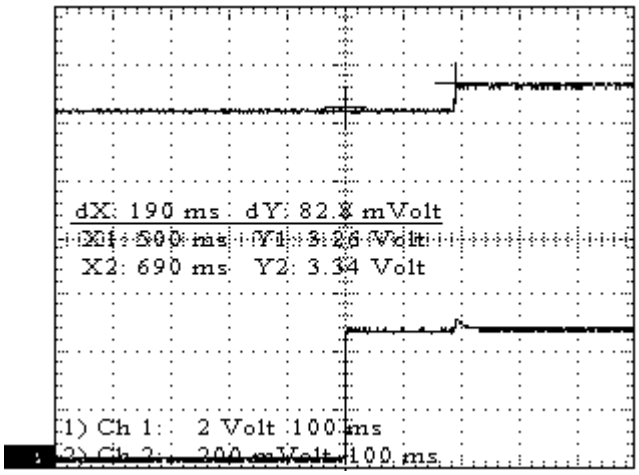


Figure 8 From S3 to S0

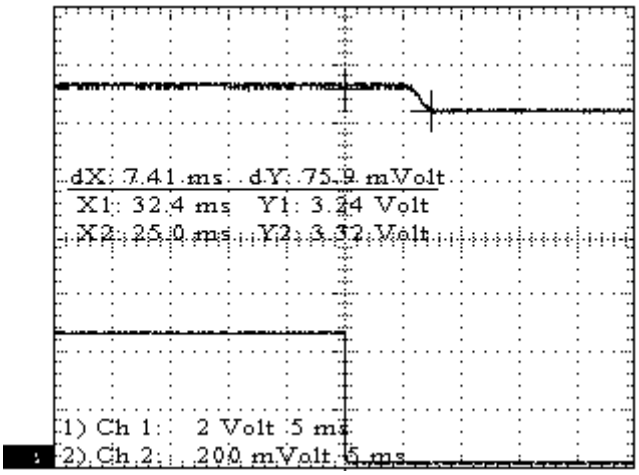


Figure 9 From S0 to S3

75mV variation is far less than the 5% range of $3.3V_{DUAL}$ specified.

Figure 10 and figure 11 show the transit from S3 to S0 with 700us delay (R4,C4) and from S0 to S3 with 1ms delay (R3,C3) transitions, respectively, for 800mA output current from an active load (Chroma 63010).

The 800mA capability has already covered the maximum output capibility of $5V_{SBY}$ (720mA) from ATX power in application of 800mA. 140mV variation is still under the 5% tolerance.

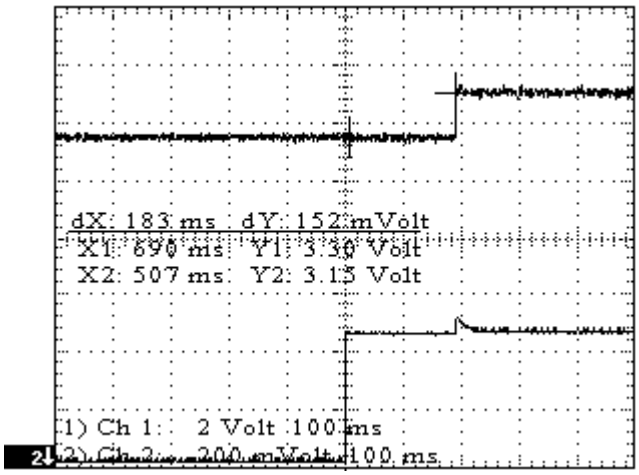


Figure 10 From S3 to S0

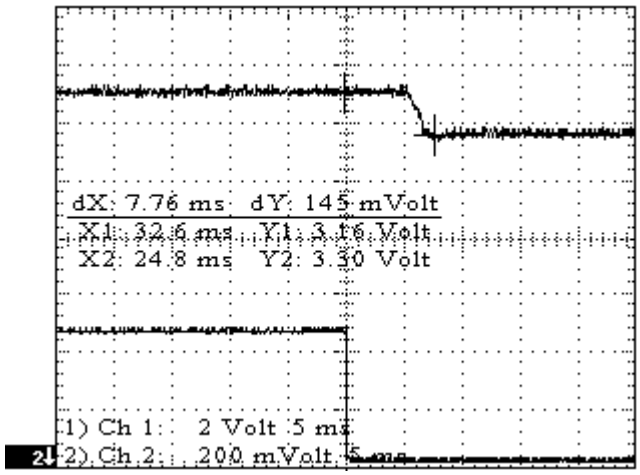


Figure 11 From S0 to S3

Conclusion

Instantly Available PCs require unique Power Management devices to provide regulated voltage sources and intelligent switches between power sources.

This solution allows motherboard manufactures to meet the power requirement of IAPC for not only providing the outstanding performance but also reducing the total BOM cost, as the components are so easy to get in market.

Keeping the output capacitor, which is larger than 220uF and as close as possible to output node, ensures the stability of the system. It is highly recommended.

Got any questions? Call AIC for applications assistance.

References

I. AIC1521 data sheet power switch from Analog Integrated Corp.
II. AIC1117 data sheet LDO from Analog Integrated Corp.
III. IAPC system power delivery requirements and recommendations Rev1.0 from Intel Corp.
IV. PCI power management interface specification Rev1.1 from PCISIG