

## Introduction

The Xilinx Automotive (XA) Spartan™-3 family of Field-Programmable Gate Arrays is specifically designed to meet the needs of high volume, cost-sensitive automotive consumer electronic applications. The four-member family offers densities ranging from 50,000 to five million system gates, as shown in [Table 1](#).

XA devices are available in both the extended-temperature Q-grade (-40°C to +125°C) and industrial I-grade (-40°C to +100°C) and are qualified to the industry-recognized AEC-Q100 standard.

The XA Spartan-3 family builds on the success of the earlier XA Spartan-II family by increasing the amount of logic resources, the capacity of internal RAM, the total number of I/Os, and the overall level of performance as well as by improving clock management functions. Numerous enhancements derive from state-of-the-art Virtex™-II technology. These Spartan-3 enhancements, combined with advanced process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3 FPGAs are ideally suited to a wide range of advanced automotive electronics modules and systems ranging from the latest driver assistance and infotainment systems to reconfigurable instrument clusters and ECU gateways.

The Spartan-3 family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

## Features

- AEC-Q100 device qualification and full PPAP support available in both extended temperature Q-grade and I-grade.
- Guaranteed to meet full electrical specifications over  $T_j = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ .
- Revolutionary 90-nanometer process technology
- Very low cost, high-performance logic solution for high-volume, automotive applications
  - 326 MHz system clock rate
  - Three power rails: for core (1.2V), I/Os (1.2V to 3.3V), and auxiliary purposes (2.5V)
- SelectIO™ signaling

- Up to 333 I/O pins
- 622 Mb/s data transfer rate per I/O
- Seventeen single-ended signal standards
- Seven differential signal standards including LVDS
- Termination by Digitally Controlled Impedance
- Signal swing ranging from 1.14V to 3.45V
- Double Data Rate (DDR) support
- Logic resources
  - Abundant logic cells with shift register capability
  - Wide multiplexers
  - Fast look-ahead carry logic
  - Dedicated 18 x 18 multipliers
  - JTAG logic compatible with IEEE 1149.1/1532
- SelectRAM™ hierarchical memory
  - Up to 576 Kbits of total block RAM
  - Up to 120 Kbits of total distributed RAM
- Digital Clock Manager (up to four DCMs)
  - Clock skew elimination
  - Frequency synthesis
- Fully supported by Xilinx ISE development system
  - Synthesis, mapping, placement and routing
- MicroBlaze™ processor, CAN, LIN, PCI, and other cores
- Pb-free packaging options
- Additionally, Xilinx and all of our production partners are qualified to QS-9000, moving to TS16949 in 2005.

Table 1: Summary of Spartan-3 FPGA Attributes

| Device   | System Gates | Logic Cells | CLB Array<br>(One CLB = Four Slices) |         |            | Distributed RAM (bits <sup>1</sup> ) | Block RAM (bits <sup>1</sup> ) | Dedicated Multipliers | DCMs | Maximum User I/O | Maximum Differential I/O Pairs |
|----------|--------------|-------------|--------------------------------------|---------|------------|--------------------------------------|--------------------------------|-----------------------|------|------------------|--------------------------------|
|          |              |             | Rows                                 | Columns | Total CLBs |                                      |                                |                       |      |                  |                                |
| XA3S50   | 50K          | 1,728       | 16                                   | 12      | 192        | 12K                                  | 72K                            | 4                     | 2    | 63               | 56                             |
| XA3S200  | 200K         | 4,320       | 24                                   | 20      | 480        | 30K                                  | 216K                           | 12                    | 4    | 173              | 76                             |
| XA3S400  | 400K         | 8,064       | 32                                   | 28      | 896        | 56K                                  | 288K                           | 16                    | 4    | 173              | 116                            |
| XA3S1000 | 1M           | 17,280      | 48                                   | 40      | 1,920      | 120K                                 | 432K                           | 24                    | 4    | 333              | 175                            |

**Notes:**

1. By convention, one Kb is equivalent to 1,024 bits.

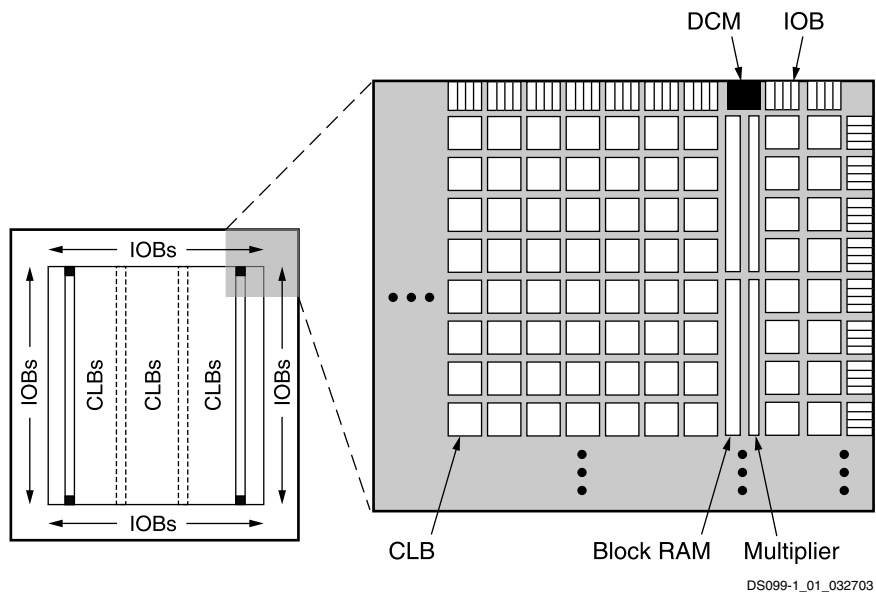
## Architectural Overview

The Spartan-3 family architecture consists of five fundamental programmable functional elements:

- Configurable Logic Blocks (CLBs) contain RAM-based Look-Up Tables (LUTs) to implement logic and storage elements that can be used as flip-flops or latches. CLBs can be programmed to perform a wide variety of logical functions as well as to store data.
- Input/Output Blocks (IOBs) control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Twenty-four different signal standards, including seven high-performance differential standards, are available as shown in [Table 2](#). Double Data-Rate (DDR) registers are included. The Digitally Controlled Impedance (DCI) feature provides automatic on-chip terminations, simplifying board designs.
- Block RAM provides data storage in the form of 18-Kbit dual-port blocks.
- Multiplier blocks accept two 18-bit binary numbers as inputs and calculate the product.
- Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase shifting clock signals.

These elements are organized as shown in [Figure 1](#). A ring of IOBs surrounds a regular array of CLBs. The XA3S50 has a single column of block RAM embedded in the array. Those devices ranging from the XA3S200 to the XA3S1000 have two columns of block RAM. Each column is made up of several 18K-bit RAM blocks; each block is associated with a dedicated multiplier. The DCMs are positioned at the ends of the outer block RAM columns.

The Spartan-3 family features a rich network of traces and switches that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



**Notes:**

1. The XA3S50 has only the block RAM column on the far left. The recommended memory for storing the configuration data is the low-cost XA Platform Flash PROM family device/package combination, which comprises the XAF00S PROMs for serial configuration.

*Figure 1: Spartan-3 Family Architecture*

## Configuration

Spartan-3 FPGAs are programmed by loading configuration data into robust static memory cells that collectively control all functional elements and routing resources. Before powering on the FPGA, configuration data is stored externally in a PROM or some other nonvolatile medium either on or off the board. After applying power, the configuration data is written to the FPGA using any of five different modes: Master Parallel, Slave Parallel, Master Serial, Slave Serial and Boundary Scan (JTAG). The Master and Slave Parallel modes use an 8-bit wide SelectMAP™ port.

The recommended memory for storing the configuration data is the low-cost Xilinx Platform Flash PROM family,

which includes the XCF00S PROMs for serial configuration and the higher density XCF00P PROMs for parallel or serial configuration.

## I/O Capabilities

The SelectIO feature of Spartan-3 devices supports 17 single-ended standards and seven differential standards as listed in Table 2. Many standards support the DCI feature, which uses integrated terminations to eliminate unwanted signal reflections. Table 3 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

Table 2: Signal Standards Supported by the Spartan-3 Family

| Standard Category   | Description                                | V <sub>CCO</sub> (V) | Class         | Symbol     | DCI Option |
|---------------------|--|----------------------|---------------|------------|------------|
| <b>Single-Ended</b> |  |                      |               |            |            |
| GTL                 | Gunning Transceiver Logic                  | N/A                  | Terminated    | GTL        | Yes        |
|                     |  |                      | Plus          | GTLP       | Yes        |
| HSTL                | High-Speed Transceiver Logic               | 1.5                  | I             | HSTL_I     | Yes        |
|                     |  |                      | III           | HSTL_III   | Yes        |
|                     |  | 1.8                  | I             | HSTL_I_18  | Yes        |
|                     |  |                      | II            | HSTL_II_18 | Yes        |
| LVCMOS              | Low-Voltage CMOS                           | 1.2                  | N/A           | LVCMOS12   | No         |
|                     |  | 1.5                  | N/A           | LVCMOS15   | Yes        |
|                     |  | 1.8                  | N/A           | LVCMOS18   | Yes        |
|                     |  | 2.5                  | N/A           | LVCMOS25   | Yes        |
|                     |  | 3.3                  | N/A           | LVCMOS33   | Yes        |
| LVTTTL              | Low-Voltage Transistor-Transistor Logic    | 3.3                  | N/A           | LVTTTL     | No         |
| PCI                 | Peripheral Component Interconnect          | 3.0                  | 33 MHz        | PCI33_3    | No         |
| SSTL                | Stub Series Terminated Logic               | 1.8                  | N/A           | SSTL18_I   | Yes        |
|                     |  | 2.5                  | I             | SSTL2_I    | Yes        |
|                     |  |                      | II            | SSTL2_II   | Yes        |
| <b>Differential</b> |  |                      |               |            |            |
| LDT (ULVDS)         | Lightning Data Transport (HyperTransport™) | 2.5                  | N/A           | LDT_25     | No         |
| LVDS                | Low-Voltage Differential Signaling         |                      | Standard      | LVDS_25    | Yes        |
|                     |  |                      | Bus           | BLVDS_25   | No         |
|                     |  |                      | Extended Mode | LVDSEXT_25 | Yes        |
| LVPECL              | Low-Voltage Positive Emitter-Coupled Logic | 2.5                  | N/A           | LVPECL_25  | No         |
| RSDS                | Reduced-Swing Differential Signaling       | 2.5                  | N/A           | RSDS_25    | No         |

Table 3: Spartan-3 XA I/O Chart

| Device   | Available User I/Os and Differential (Diff) I/O Pairs |      |        |      |        |      |        |      |
|----------|---|------|--------|------|--------|------|--------|------|
|          | VQG100  |      | PQG208 |      | FTG256 |      | FGG456 |      |
|          | User  | Diff | User   | Diff | User   | Diff | User   | Diff |
| XA3S50   | 63  | 29   | 124    | 56   | -      | -    | -      | -    |
| XA3S200  | 63  | 29   | 141    | 62   | 173    | 76   | -      | -    |
| XA3S400  | -   | -    | 141    | 62   | 173    | 76   | -      | -    |
| XA3S1000 | -   | -    | -      | -    | -      | -    | 333    | 149  |

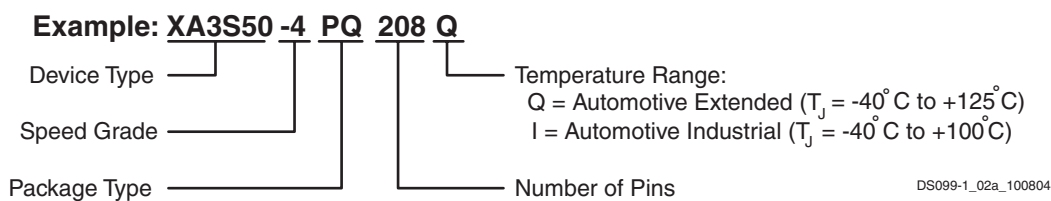
**Notes:**

- All device options listed in a given package column are pin-compatible.

**Ordering Information**

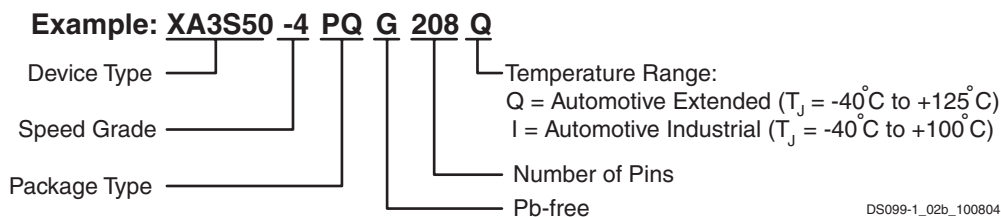
Spartan-3 FPGAs are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a special 'G' character in the ordering code.

**Standard Packaging**



**Pb-Free Packaging**

For additional information on Pb-free packaging, see [XAPP427: Xilinx Lead Free Packages](#).



| Device   | Speed Grade |                      | Package Type / Number of Pins |  | Temperature Range ( $T_J$ ) |  |
|----------|-------------|----------------------|-------------------------------|--|-----------------------------|--|
|          |             |                      |                               |  |                             |  |
| XA3S50   | -4          | Standard Performance | VQ(G)100                      | 100-pin Very Thin Quad Flat Pack (VQFP)          | I                           | Automotive Industrial<br>( $-40^\circ\text{C}$ to $+100^\circ\text{C}$ ) |
| XA3S200  |             |                      | PQ(G)208                      | 208-pin Plastic Quad Flat Pack (PQFP)            | Q                           | Automotive Extended<br>( $-40^\circ\text{C}$ to $+125^\circ\text{C}$ )   |
| XA3S400  |             |                      | FT(G)256                      | 256-ball Fine-Pitch Thin Ball Grid Array (FTBGA) |                             |  |
| XA3S1000 |             |                      | FG(G)456                      | 456-ball Fine-Pitch Ball Grid Array (FBGA)       |                             |  |

## Revision History

| Date     | Version No. | Description             |
|----------|-------------|-------------------------|
| 10/18/04 | 1.0         | Initial Xilinx release. |

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## The Spartan-3 Family Data Sheet

DS099-1, *Spartan-3 FPGA Family: Introduction and Ordering Information* (Module 1)

DS099-2, *Spartan-3 FPGA Family: [Functional Description](#)* (Module 2)

DS099-3, *Spartan-3 FPGA Family: [DC and Switching Characteristics](#)* (Module 3)

DS099-4, *Spartan-3 FPGA Family: [Pinout Descriptions](#)* (Module 4)