19-3558; Rev 2; 10/05

27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Serializer

General Description

The MAX9217 digital video parallel-to-serial converter serializes 27 bits of parallel data into a serial data stream. Eighteen bits of video data and 9 bits of control data are encoded and multiplexed onto the serial interface, reducing the serial data rate. The data enable input determines when the video or control data is serialized.

The MAX9217 pairs with the MAX9218 deserializer to form a complete digital video serial link. Interconnect can be controlled-impedance PC board traces or twisted-pair cable. Proprietary data encoding reduces EMI and provides DC balance. DC balance allows AC-coupling, providing isolation between the transmitting and receiving ends of the interface. The LVDS output is internally terminated with 100Ω.

ESD tolerance is specified for ISO 10605 with ±10kV contact discharge and ±30kV air discharge.

The MAX9217 operates from a +3.3V core supply and features a separate input supply for interfacing to 1.8V to 3.3V logic levels. This device is available in 48-lead Thin QFN and TQFP packages and is specified from -40°C to +85°C.

Applications

Navigation System Display

In-Vehicle Entertainment System

Video Camera

LCD Displays

Features

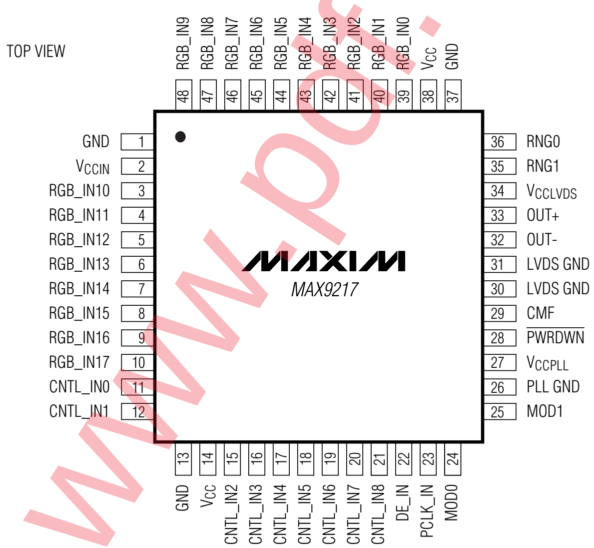
- **Proprietary Data Encoding for DC Balance and Reduced EMI**
- **Control Data Sent During Video Blanking**
- **Five Control Data Inputs Are Single-Bit-Error Tolerant**
- **Programmable Phase-Shifted LVDS Signaling Reduces EMI**
- **Output Common-Mode Filter Reduces EMI**
- **Greater than 10m STP Cable Drive**
- **Wide ±2% Reference Clock Tolerance**
- **ISO 10605 ESD Protection**
- **Separate Input Supply Allows Interface to 1.8V to 3.3V Logic**
- **+3.3V Core Supply**
- **Space-Saving Thin QFN and TQFP Packages**
- **-40°C to +85°C Operating Temperature**

Ordering Information

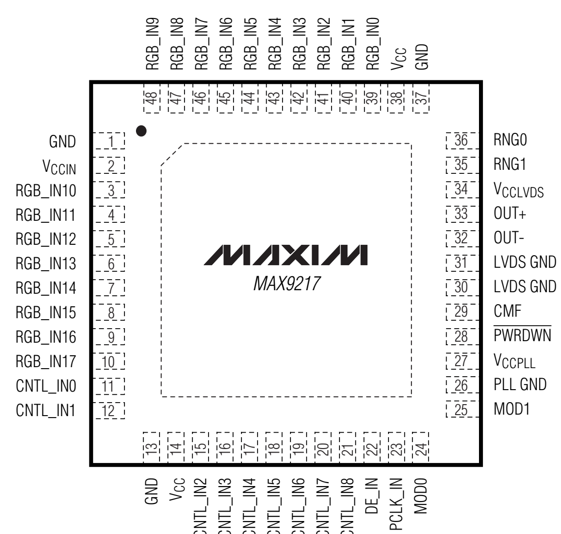
PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9217ECM	-40°C to +85°C	48 TQFP	C48-5
MAX9217ETM	-40°C to +85°C	48 Thin QFN-EP*	T4866-1

*EP = Exposed pad.

Pin Configurations



TQFP



THIN QFN-EP

ABSOLUTE MAXIMUM RATINGS

$V_{CC\_}$ to _GND..-0.5V to +4.0V
Any Ground to Any Ground...................................-0.5V to +0.5V
OUT+, OUT- to LVDS GND ....-0.5V to +4.0V
OUT+, OUT- Short Circuit to LVDS GND
or V_{CCLVDS}..Continuous
OUT+, OUT- Short Through 0.125µF (or smaller),
25V Series Capacitor..-0.5V to +16V
RGB_IN[17:0], CNTL_IN[8:0], DE_IN,
RNG0, RNG1, MOD0, MOD1, PCLK_IN,
$\overline{PWRDWN}$, CMF to GND......................-0.5V to (V_{CCIN} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
48-Lead TQFP (derate 20.8mW/°C above +70°C) 1667mW
48-Lead Thin QFN (derate 37mW/°C above +70°C) .2963mW

ESD Protection
Human Body Model (R_D = 1.5kΩ, C_S = 100pF)
All Pins to GND...±2kV
ISO 10605 (R_D = 2kΩ, C_S = 330pF)
Contact Discharge (OUT+, OUT-) to GND.....................±10kV
Air Discharge (OUT+, OUT-) to GND............................±30kV
Storage Temperature Range ....-65°C to +150°C
Junction Temperature ....+150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC\_}$ = +3.0V to +3.6V, R_L = 100Ω ±1%, $\overline{PWRDWN}$ = high, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (RGB_IN[17:0], CNTL_IN[8:0], DE_IN, PCLK_IN, $\overline{PWRDWN}$, RNG_, MOD_)						
High-Level Input Voltage	V_{IH}	V_{CCIN} = 1.71V to <3V	$0.65V_{CCIN}$		V_{CCIN} + 0.3	V
			2		V_{CCIN} + 0.3	
Low-Level Input Voltage	V_{IL}	V_{CCIN} = 1.71V to <3V	-0.3		$0.3V_{CCIN}$	V
			-0.3		+0.8	
Input Current	I_{IN}	V_{IN} = -0.3V to (V_{CCIN} + 0.3V), V_{CCIN} = 1.71V to 3.6V, $\overline{PWRDWN}$ = high or low	-70		+70	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA			-1.5	V
LVDS OUTPUTS (OUT+, OUT-)						
Differential Output Voltage	V_{OD}	Figure 1	250	335	450	mV
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 1			20	mV
Common-Mode Voltage	V_{OS}	Figure 1	1.125	1.29	1.375	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}	Figure 1			20	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0 or 3.6V	-15	±8	+15	mA
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0		5.5	15	mA
Output High-Impedance Current	I_{OZ}	$\overline{PWRDWN}$ = low or $V_{CC\_}$ = 0; OUT+ = 0, OUT- = 3.6V	-1		+1	µA
		$\overline{PWRDWN}$ = low or $V_{CC\_}$ = 0; OUT+ = 3.6V, OUT- = 0				

DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC\_}$ = +3.0V to +3.6V, R_L = 100Ω ±1%, $\overline{PWRDWN}$ = high, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Output Resistance	R_O			78	110	147	Ω
Worst-Case Supply Current	I_{CCW}	R_L = 100Ω ± 1%, C_L = 5pF, continuous 10 transition words, modulation off	3MHz		15	25	mA
			5MHz		18	25	
			10MHz		23	28	
			20MHz		33	39	
			35MHz		50	70	
Power-Down Supply Current	I_{CCZ}	(Note 3)				50	µA

AC ELECTRICAL CHARACTERISTICS

($V_{CC\_}$ = +3.0V to +3.6V, R_L = 100Ω ±1%, C_L = 5pF, $\overline{PWRDWN}$ = high, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PCLK_IN TIMING REQUIREMENTS						
Clock Period	t_T	Figure 2	28.57		333.00	ns
Clock Frequency	f_{CLK}		3		35	MHz
Clock Frequency Difference from Deserializer Reference Clock	Δf_{CLK}		-2		+2	%
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T, Figure 2	35	50	65	%
Clock Transition Time	t_R, t_F	Figure 2			2.5	ns
SWITCHING CHARACTERISTICS						
Output Rise Time	t_{RISE}	20% to 80%, V_{OD} ≥ 250mV, modulation off, Figure 3		215	350	ps
Output Fall Time	t_{FALL}	80% to 20%, V_{OD} ≥ 250mV, modulation off, Figure 3		206	350	ps
Input Setup Time	t_{SET}	Figure 4	3			ns
Input Hold Time	t_{HOLD}	Figure 4	3			ns
Serializer Delay	t_{SD}	Figure 5	3.15 x t_T		3.2 x t_T	ns
PLL Lock Time	t_{LOCK}	Figure 6			16385 x t_T	ns
Power-Down Delay	t_{PD}	Figure 7			1	µs

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AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC\_}$ = +3.0V to +3.6V, R_L = 100Ω ±1%, C_L = 5pF, $\overline{PWRDWN}$ = high, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Peak-to-Peak Output Offset Voltage	V_{OSp-p}	700Mbps data rate, CMF open, Figure 8		22	70	mV
		700Mbps data rate, CMF 0.1µF to ground, Figure 8		12	50	

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{OD}, ΔV_{OD}, and ΔV_{OS}.

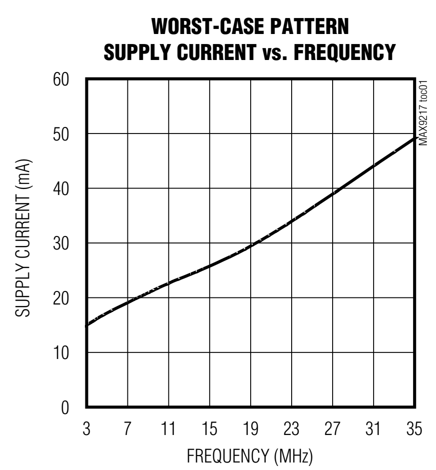
Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at T_A = +25°C.

Note 3: All LVTTL/LVCMOS inputs, except $\overline{PWRDWN}$ at ≤ 0.3V or ≥ V_{CCIN} - 0.3V. $\overline{PWRDWN}$ is ≤ 0.3V.

Note 4: AC parameters are guaranteed by design and characterization and are not production tested. Limits are set at ±6 sigma.

Typical Operating Characteristics

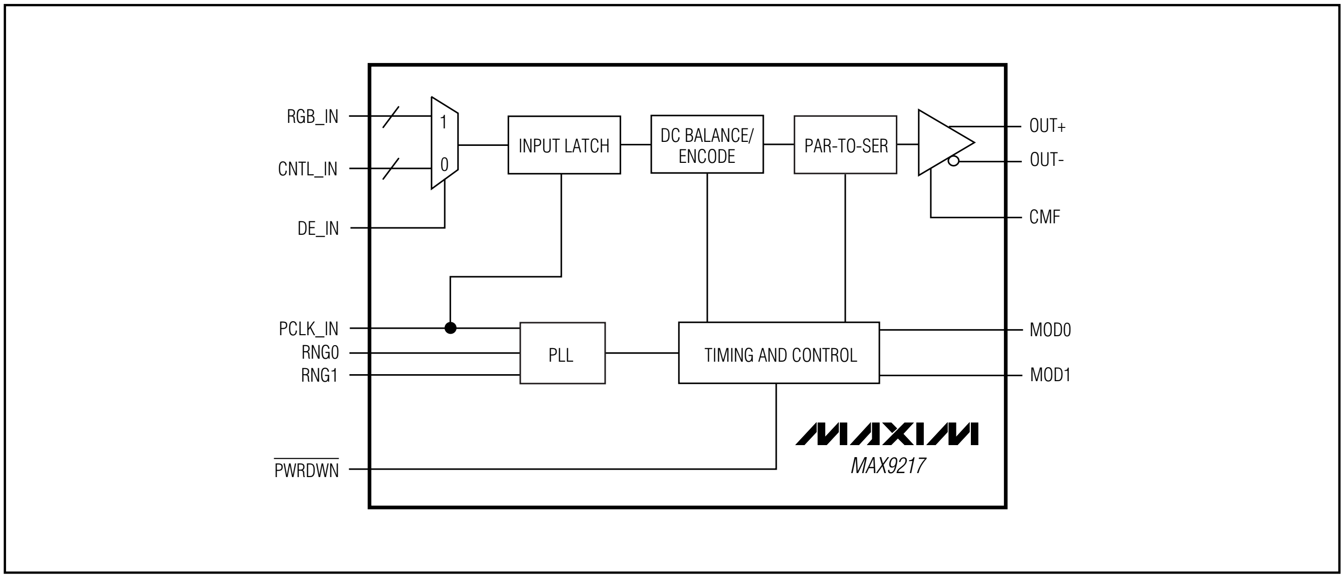
(T_A = +25°C, $V_{CC\_}$ = +3.3V, R_L = 100Ω, modulation off, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1, 13, 37	GND	Input Buffer Supply and Digital Supply Ground
2	V_{CCIN}	Input Buffer Supply Voltage. Bypass to GND with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
3–10, 39–48	RGB_IN[17:0]	LVTTL/LVCMOS Red, Green, and Blue Digital Video Data Inputs. Eighteen data bits are loaded into the input latch on the rising edge of PCLK_IN when DE_IN is high. Internally pulled down to GND.
11, 12, 15–21	CNTL_IN[8:0]	LVTTL/LVCMOS Control Data Inputs. Control data are latched on the rising edge of PCLK_IN when DE_IN is low. Internally pulled down to GND.
14, 38	V_{CC}	Digital Supply Voltage. Bypass to GND with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
22	DE_IN	LVTTL/LVCMOS Data Enable Input. Logic-high selects RGB_IN[17:0] to be latched. Logic-low selects CNTL_IN[8:0] to be latched. DE_IN must be switching for proper operation. Internally pulled down to GND.
23	PCLK_IN	LVTTL/LVCMOS Parallel Clock Input. Latches data and control inputs and provides the PLL reference clock. Internally pulled down to GND.
24	MOD0	LVTTL/LVCMOS Modulation Rate Input. Selects the phase-modulation step size. Internally pulled down to GND.
25	MOD1	LVTTL/LVCMOS Modulation Rate Input. Selects the phase-modulation step size. Internally pulled down to GND.
26	PLL GND	PLL Supply Ground
27	V_{CCPLL}	PLL Supply Voltage. Bypass to PLL GND with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
28	$\overline{PWRDWN}$	LVTTL/LVCMOS Power-Down Input. Internally pulled down to GND.
29	CMF	Common-Mode Filter. Optionally connect a capacitor between CMF and ground to filter common-mode switching noise.
30, 31	LVDS GND	LVDS Supply Ground
32	OUT-	Inverting LVDS Serial Data Output
33	OUT+	Noninverting LVDS Serial Data Output
34	V_{CCLVDS}	LVDS Supply Voltage. Bypass to LVDS GND with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
35	RNG1	LVTTL/LVCMOS Frequency Range Select Input. Set to the frequency range that includes the PCLK_IN frequency as shown in Table 3. Internally pulled down to GND.
36	RNG0	LVTTL/LVCMOS Frequency Range Select Input. Set to the frequency range that includes the PCLK_IN frequency as shown in Table 3. Internally pulled down to GND.
EP	GND	Exposed Pad (Thin QFN Package Only). Connect Thin QFN exposed pad to PC board GND.

Functional Diagram



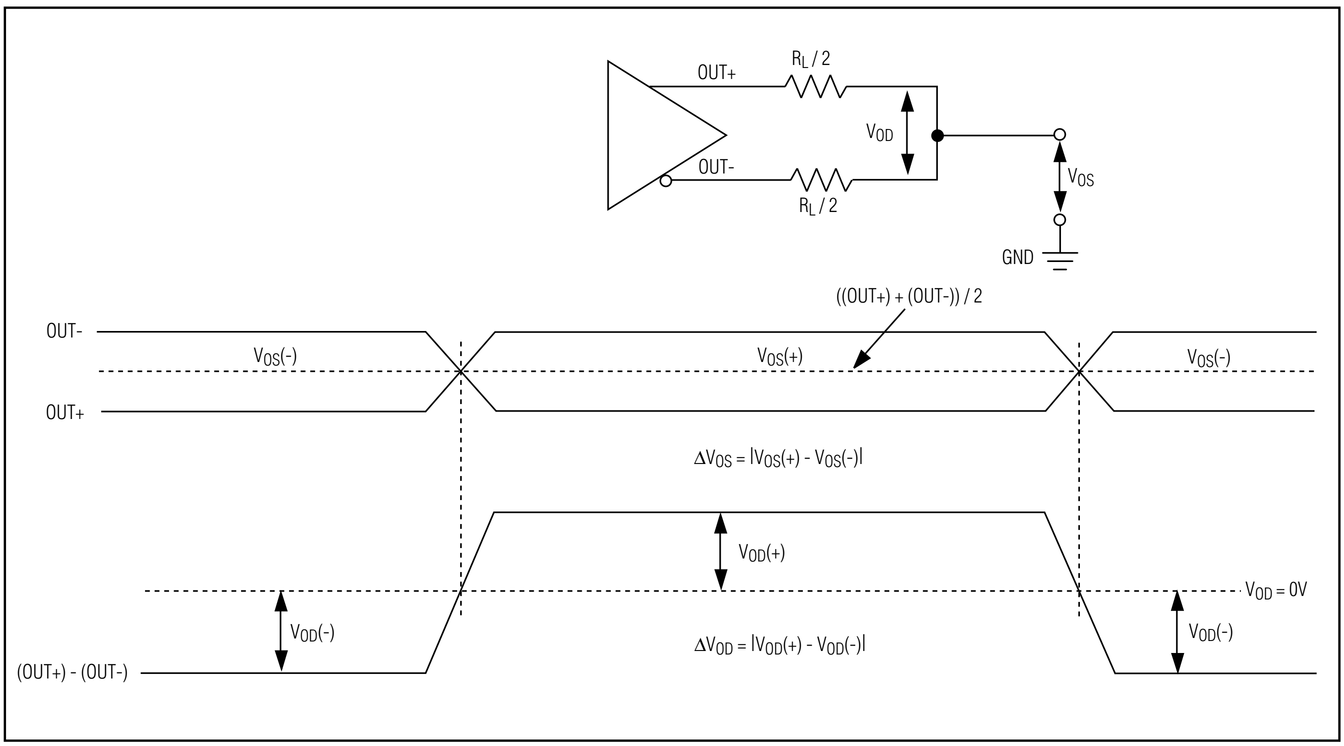


Figure 1. LVDS DC Output Load and Parameters

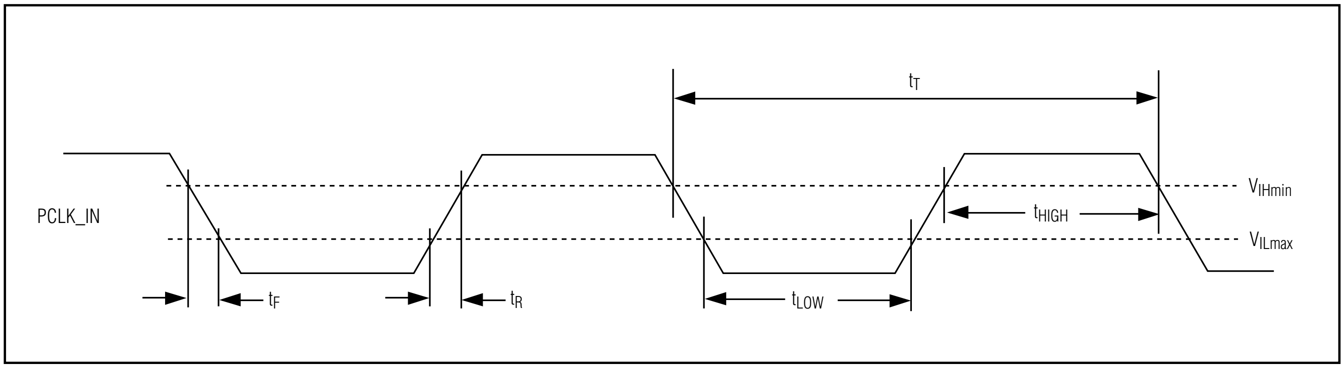


Figure 2. Parallel Clock Requirements

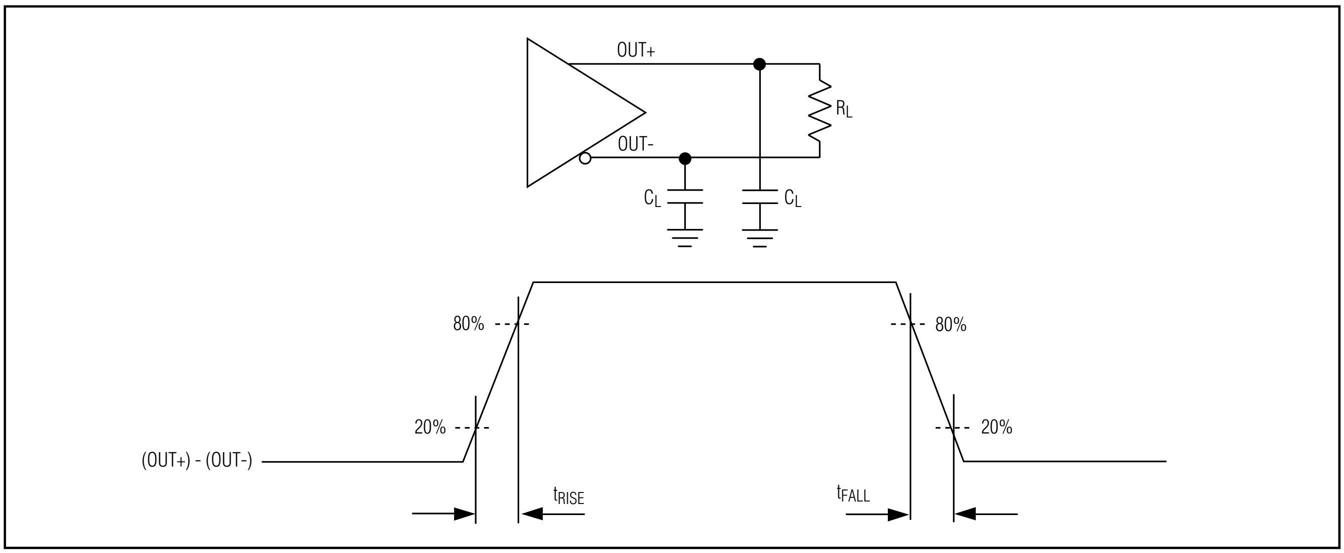


Figure 3. Output Rise and Fall Times

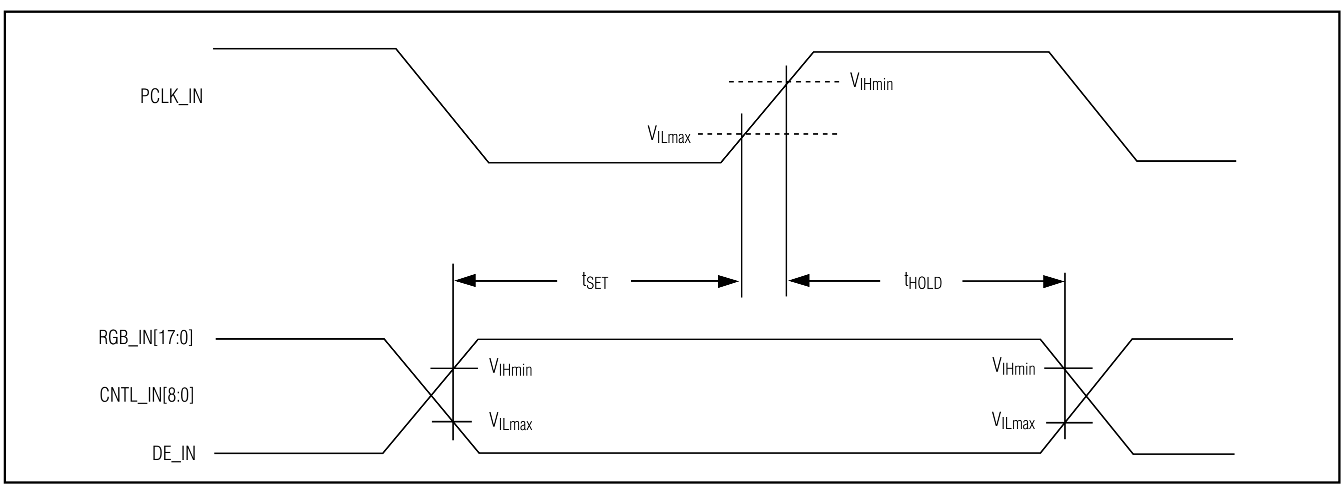


Figure 4. Synchronous Input Timing

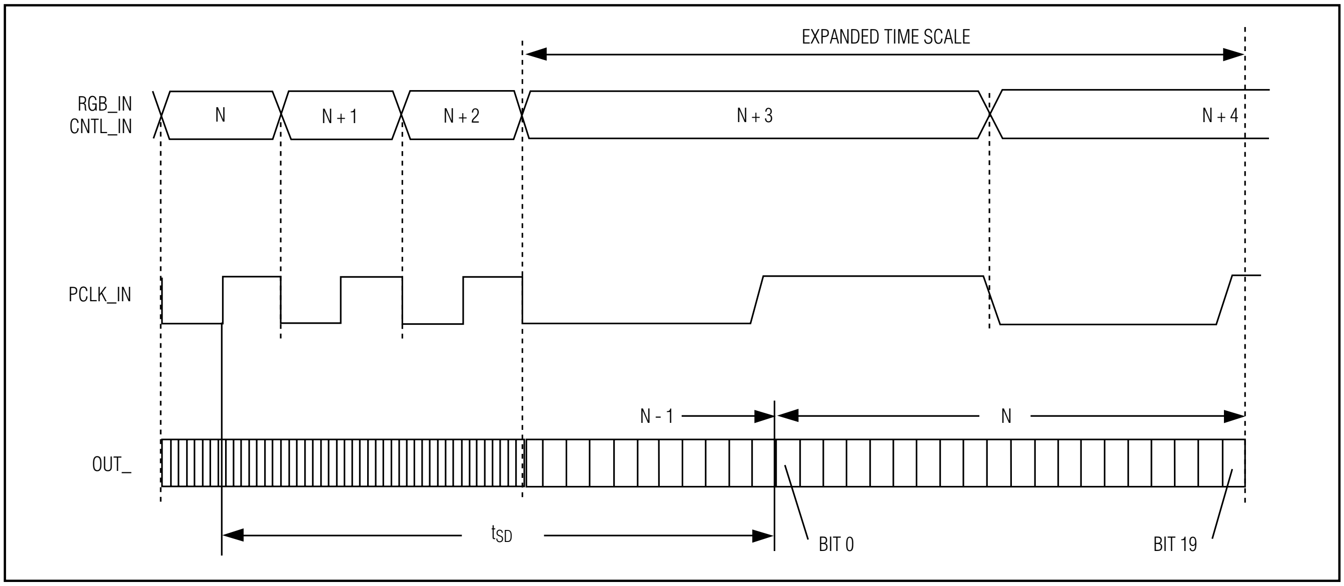


Figure 5. Serializer Delay

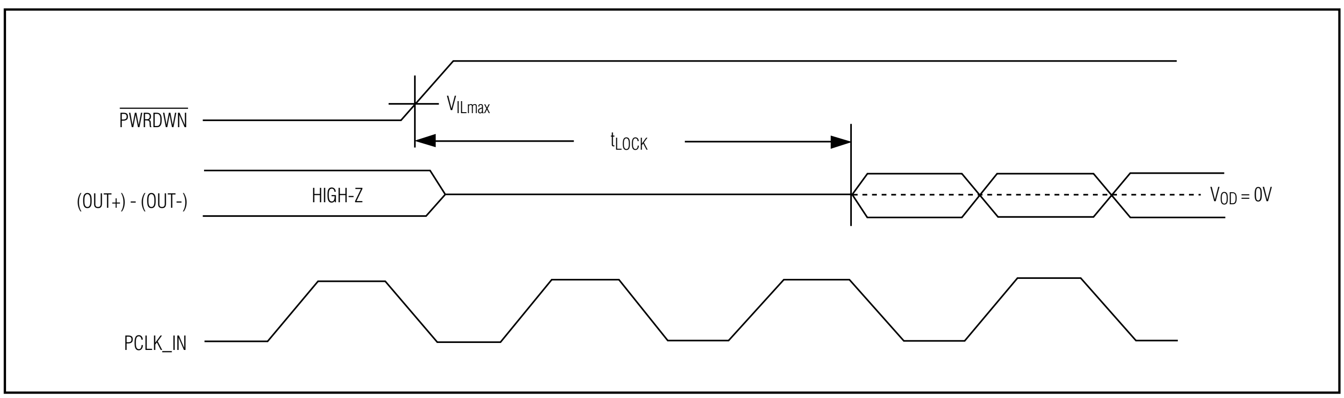


Figure 6. PLL Lock Time

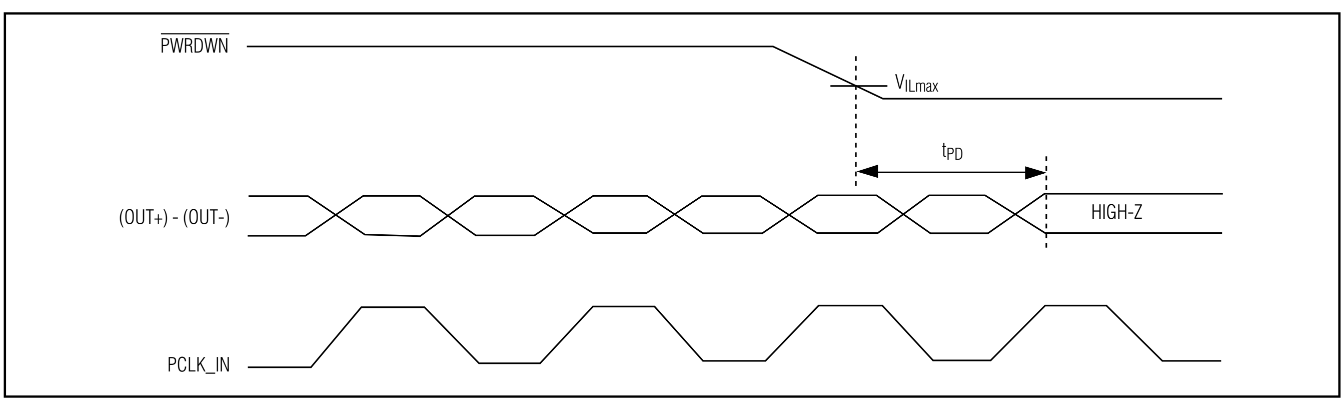


Figure 7. Power-Down Delay

Figure 8. Peak-to-Peak Output Offset Voltage

Detailed Description

The MAX9217 DC-balanced serializer operates at a parallel clock frequency of 3MHz to 35MHz, serializing 18 bits of parallel video data RGB_IN[17:0] when the data enable input DE_IN is high, or 9 bits of parallel control data CNTL_IN[8:0] when DE_IN is low. The RGB video input data are encoded using 2 overhead bits, EN0 and EN1, resulting in a serial word length of 20 bits (Table 1). Control inputs are mapped to 19 bits and encoded with 1 overhead bit, EN0, also resulting in a 20-bit serial word. Encoding reduces EMI and maintains DC balance across the serial cable. Two transition words, which contain a unique bit sequence, are inserted at the transition boundaries of video-to-control and control-to-video phases.

Control data inputs C0 to C4 are mapped to 3 bits each in the serial control word (Table 2). At the deserializer, 2 or 3 bits at the same state determine the state of the recovered bit, providing single bit-error tolerance for C0 to C4. Control data that may be visible if an error occurs, such as VSYNC and HSYNC, can be connected to these inputs. Control data inputs C5 to C8 are mapped to 1 bit each.

Table 1. Serial Video Phase Word Format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
EN0	EN1	S0	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17

Bit 0 is the LSB and is serialized first. EN[1:0] are encoding bits. S[17:0] are encoded symbols.

Table 2. Serial Control Phase Word Format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
EN0	C0	C0	C0	C1	C1	C1	C2	C2	C2	C3	C3	C3	C4	C4	C4	C5	C6	C7	C8

Bit 0 is the LSB and is serialized first. C[8:0] are the control inputs.

27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Serializer

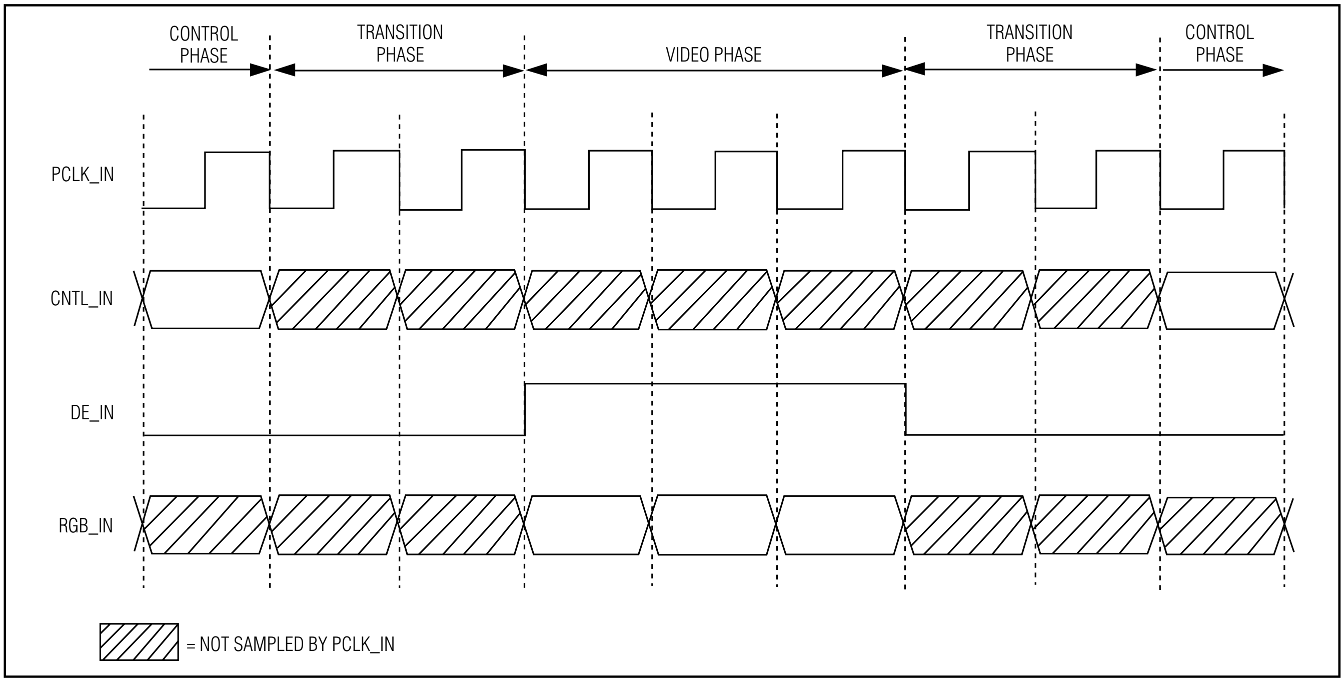


Figure 9. Transition Timing

Transition Timing

The transition words require interconnect bandwidth and displace control data. Therefore, control data is not sampled (see Figure 9):

- Two clock cycles before DE_IN goes high.
- During the video phase.
- Two clock cycles after DE_IN goes low.

The last sampled control data are latched at the deserializer control data outputs during the transition and video phases. Video data are latched at the deserializer RGB data outputs during the transition and control phases.

Applications Information

AC-Coupling Benefits

AC-coupling increases the common-mode voltage to the voltage rating of the capacitor. Two capacitors are sufficient for isolation, but four capacitors—two at the serializer output and two at the deserializer input—provide protection if either end of the cable is shorted to a high voltage. AC-coupling blocks low-frequency ground shifts and common-mode noise. The MAX9217 serializer can also be DC-coupled to the MAX9218 deserializer.

Figure 10 shows an AC-coupled serializer and deserializer with two capacitors per link, and Figure 11 is the AC-coupled serializer and deserializer with four capacitors per link.

Selection of AC-Coupling Capacitors

See Figure 12 for calculating the capacitor values for AC-coupling, depending on the parallel clock frequency. The plot shows capacitor values for two- and four-capacitor-per-link systems. For applications using less than 18MHz clock frequency, use 0.125µF capacitors.

Frequency-Range Setting RNG[1:0]

The RNG[1:0] inputs select the operating frequency range of the MAX9217 serializer. An external clock within this range is required for operation. Table 3 shows the selectable frequency ranges and corresponding data rates for the MAX9217.

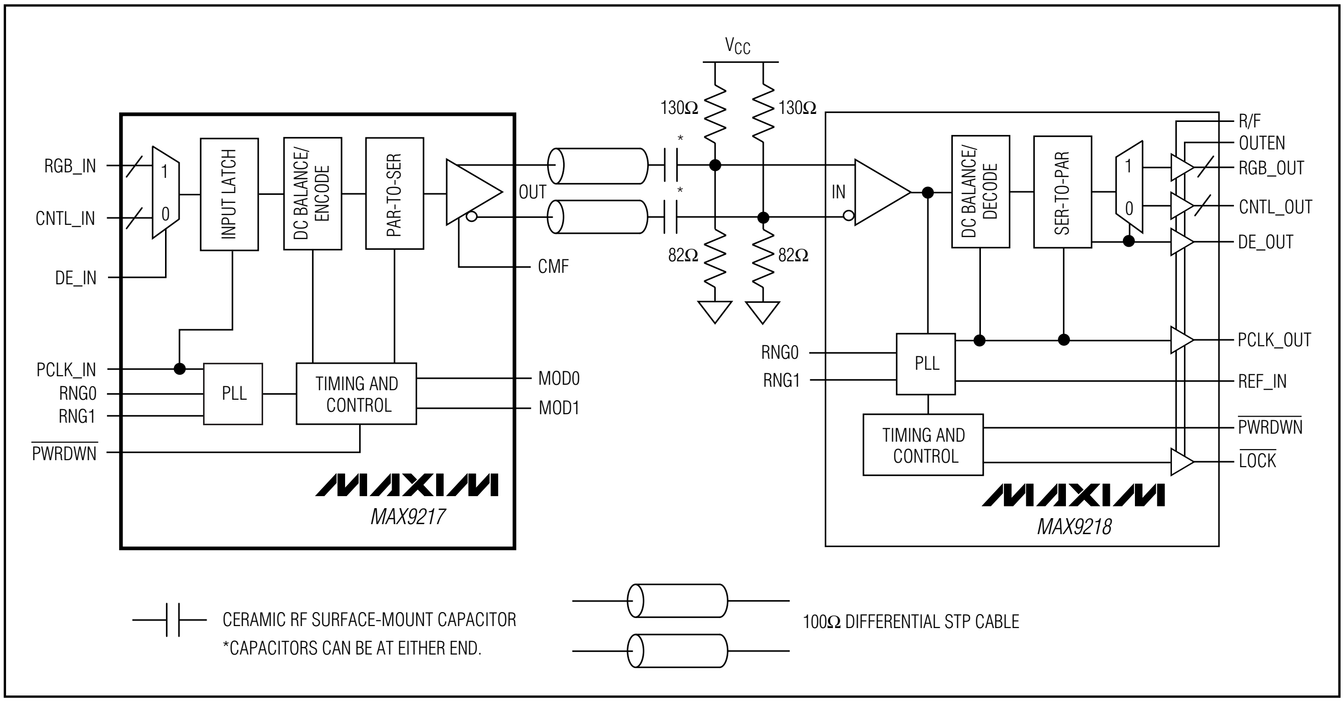


Figure 10. AC-Coupled Serializer and Deserializer with Two Capacitors per Link

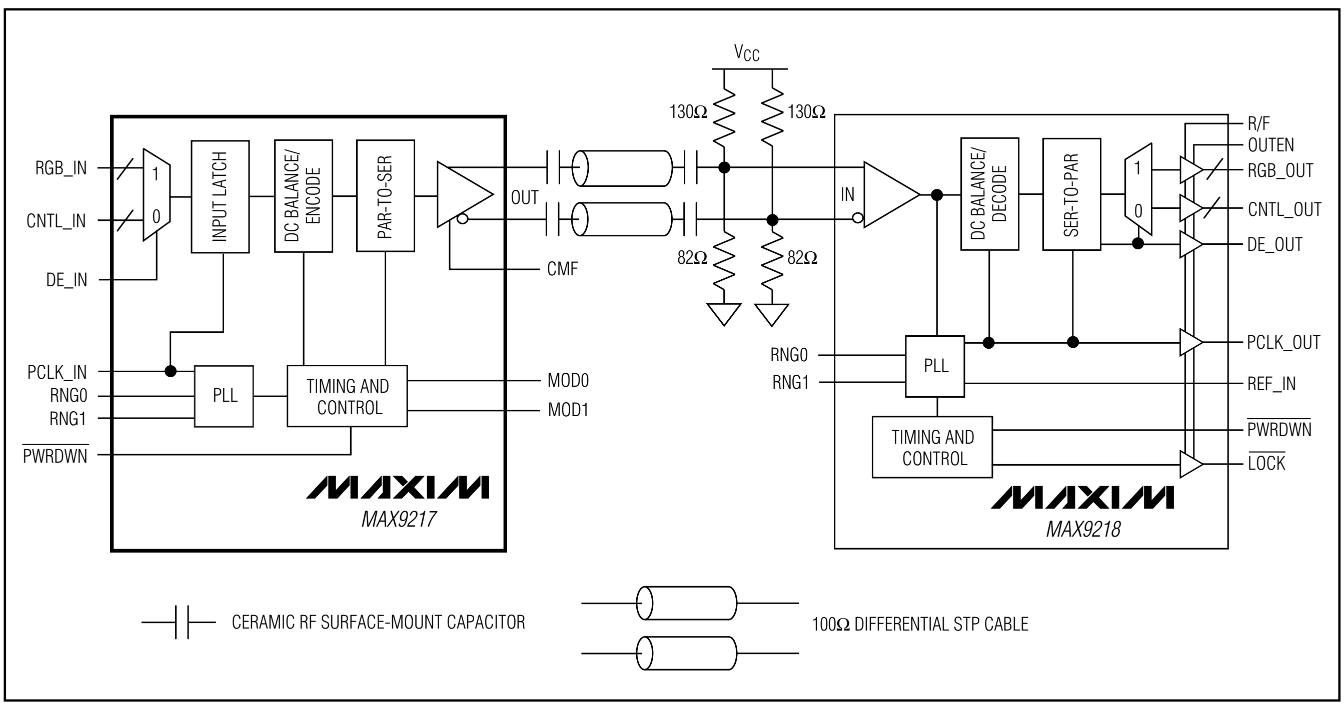


Figure 11. AC-Coupled Serializer and Deserializer with Four Capacitors per Link

27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Serializer

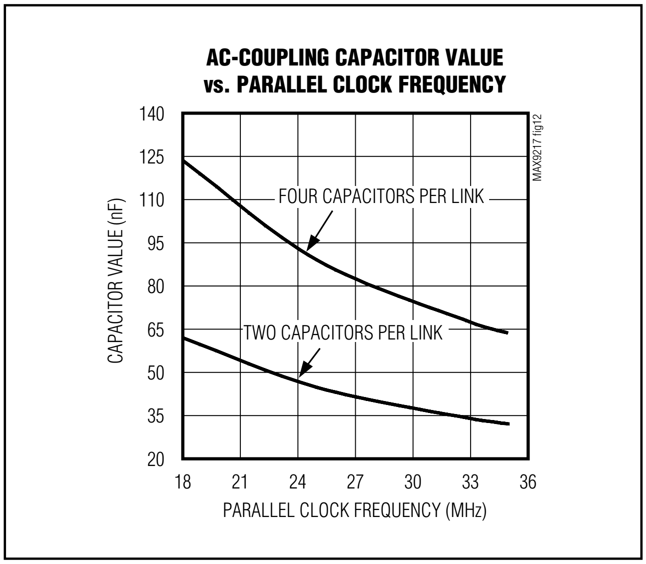


Figure 12. AC-Coupling Capacitor Values vs. Clock Frequency of 18MHz to 35MHz

Phase-Modulation Setting MOD[1:0]

The serial output edges can be phase shifted (modulated) to reduce EMI. Table 4 shows the available settings for phase modulation. Two shift amplitudes are available. The parallel clock frequency should be 10MHz or higher for the highest amplitude (MOD1 = 1, MOD0 = 0).

Termination

The MAX9217 has an integrated 100Ω output-termination resistor. This resistor damps reflections from induced noise and mismatches between the transmission line impedance and termination resistors at the deserializer input. With $\overline{\text{PWRDWN}}$ = low or with the supply off, the output termination is switched out and the LVDS output is high impedance.

Common-Mode Filter

The integrated 100Ω output termination is made up of two 50Ω resistors in series. The junction of the resistors is connected to the CMF pin for connecting an optional common-mode filter capacitor. Connect the filter capacitor to ground close to the MAX9217 as shown in Figure 13. The capacitor shunts common-mode switching current to ground to reduce EMI.

Table 3. Parallel Clock Frequency Range Select

RNG1	RNG0	PARALLEL CLOCK (MHz)	SERIAL DATA RATE (Mbps)
0	0	3 to 5	60 to 100
0	1	5 to10	100 to 200
1	0	10 to 20	200 to 400
1	1	20 to 35	400 to 700

Table 4. Modulation Rate Function Table

MOD1	MOD0	SIMULATED PEAK POWER REDUCTION (dB)
0	0	0 (off)
0	1	2.5
1	0	4.5
1	1	(reserved)

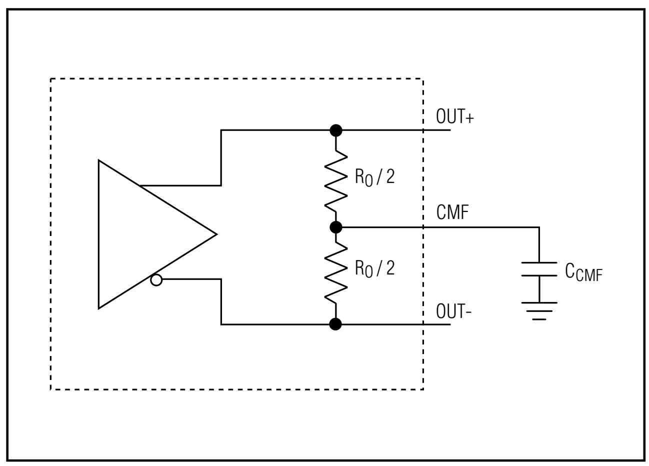


Figure 13. Common-Mode Filter Capacitor Connection

Power-Down and Power-Off

Driving $\overline{PWRDWN}$ low stops the PLL, switches out the integrated 100Ω output termination, and puts the output in high impedance to ground and differentially. With $\overline{PWRDWN}$ ≤ 0.3V and all LVTTL/LVCMOS inputs ≤ 0.3V or ≥ V_{CCIN} - 0.3V, supply current is reduced to 50µA or less.

Driving $\overline{PWRDWN}$ high starts PLL lock to PCLK_IN and switches in the 100Ω output termination resistor. The LVDS output is not driven until the PLL locks. The LVDS output is high impedance to ground and 100Ω differential. The 100Ω integrated termination pulls OUT+ and OUT- together while the PLL is locking so that V_{OD} = 0V.

If V_{CC} = 0, the output resistor is switched out and the LVDS outputs are high impedance to ground and differentially.

PLL Lock Time

The PLL lock time is set by an internal counter. The lock time is 16,385 PCLK_IN cycles. Power and clock should be stable to meet the lock-time specification.

Input Buffer Supply

The single-ended inputs (RGB_IN[17:0], CNTL_IN[8:0], DE_IN, RNG0, RNG1, MOD0, MOD1, PCLK_IN, and $\overline{PWRDWN}$) are powered from V_{CCIN}. V_{CCIN} can be connected to a 1.71V to 3.6V supply, allowing logic inputs with a nominal swing of V_{CCIN}. If no power is applied to V_{CCIN} when power is applied to V_{CC}, the inputs are disabled and $\overline{PWRDWN}$ is internally driven low, putting the device in the power-down state.

Power-Supply Circuits and Bypassing

The MAX9217 has isolated on-chip power domains. The digital core supply (V_{CC}) and single-ended input supply (V_{CCIN}) are isolated but have a common ground (GND). The PLL has separate power and ground (V_{CCPLL} and V_{CCPLL} GND) and the LVDS input also has separate power and ground (V_{CCLVDS} and V_{CCLVDS} GND). The grounds are isolated by diode connections. Bypass each V_{CC}, V_{CCIN}, V_{CCPLL}, and V_{CCLVDS} pin with high-frequency, surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.

LVDS Output

The LVDS output is a current source. The voltage swing is proportional to the termination resistance. The output is rated for a differential load of 100Ω ±1%.

Cables and Connectors

Interconnect for LVDS typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

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Board Layout

Separate the LVTTL/LVCMOS inputs and LVDS output to prevent crosstalk. A four-layer PC board with separate layers for power, ground, and signals is recommended.

ESD Protection

The MAX9217 ESD tolerance is rated for Human Body Model and ISO 10605. ISO 10605 specifies ESD tolerance for electronic systems. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 14). The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 15).

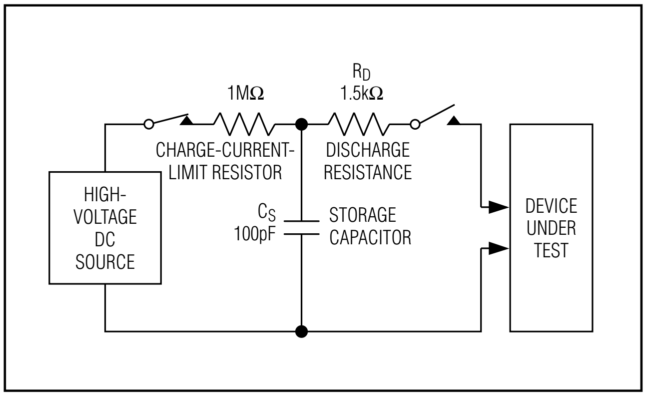


Figure 14. Human Body ESD Test Circuit

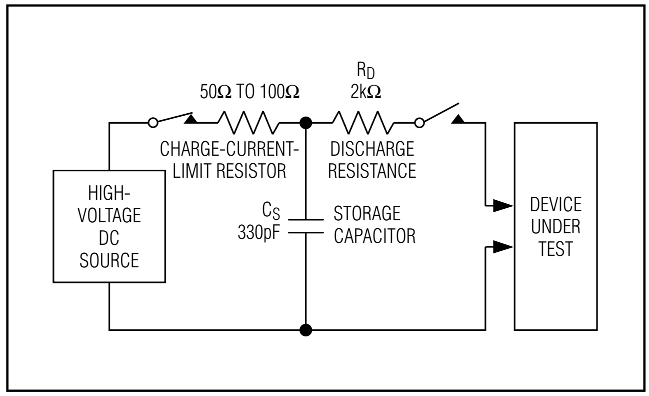


Figure 15. ISO 10605 Contact-Discharge ESD Test Circuit

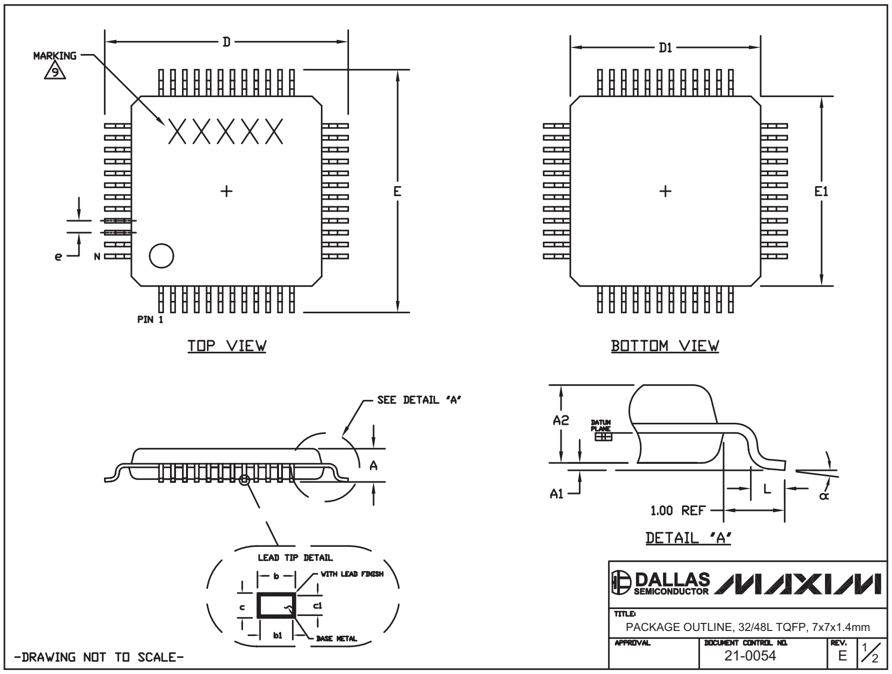
Chip Information

TRANSISTOR COUNT: 16,608

PROCESS: CMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. NUMBER OF LEADS ARE SHOWN FOR REFERENCE ONLY.

JEDEC VARIATION

	BBA		BBC	
	MIN.	MAX.	MIN.	MAX.
A	--	1.60	--	1.60
A_1	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D_1	6.90	7.10	6.90	7.10
E	8.90	9.10	8.90	9.10
E_1	6.90	7.10	6.90	7.10
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
b1	0.30	0.40	0.17	0.23
c	0.09	0.20	0.09	0.20
c1	0.09	0.16	0.09	0.16
N	32		48	
α	0°	7°	0°	7°

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 32/48L TQFP, 7x7x1.4mm

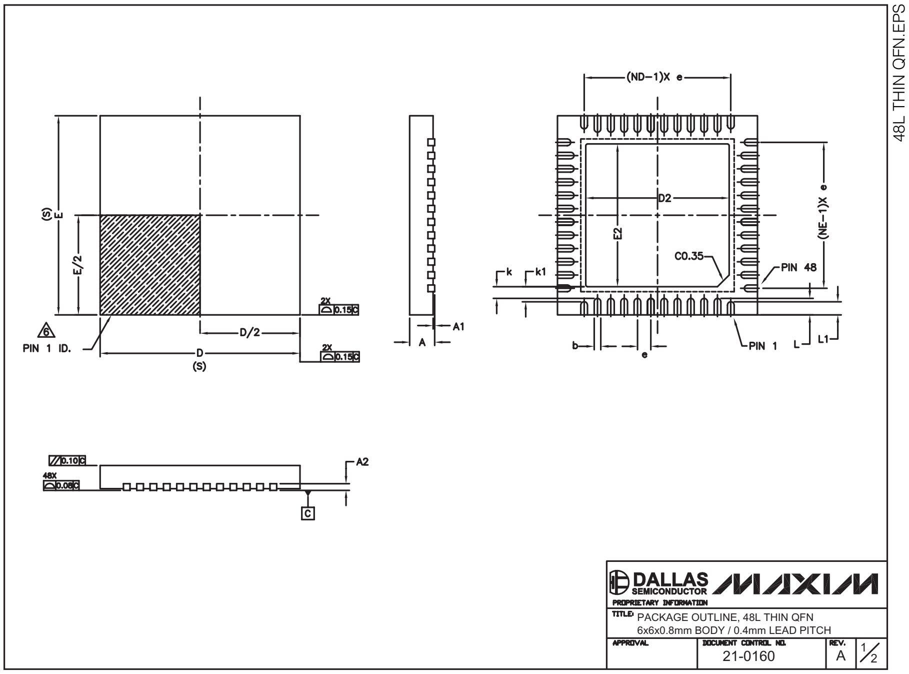
APPROVAL | DOCUMENT CONTROL NO. 21-0054 | REV. E | 2/2

-DRAWING NOT TO SCALE-

27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Serializer

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. REFER TO JEDEC MO-220.
6. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
7. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

	COMMON DIMENSIONS		
SYMBOLS	MIN.	NOM.	MAX.
A	0.700	0.750	0.800
A1	0.000	-- --	0.050
A2	0.200 REF.		
b	0.150	0.200	0.250
D	5.900	6.000	6.100
e	0.400 TYP.		
E	5.900	6.000	6.050
k	0.250	0.350	0.450
k1	0.350	0.450	0.550
L	0.400	0.500	0.600
L1	0.300	0.400	0.500
N	48		
ND	12		
NE	12		

	EXPOSED PAD VARIATONS					
PKG. CODE	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T4866-1	4.20	4.30	4.40	4.20	4.30	4.40

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 48L THIN QFN 6x6x0.8mm BODY / 0.4mm LEAD PITCH
APPROVAL | DOCUMENT CONTROL NO. 21-0160 | REV. A | 2/2

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