6N137

Features

- 1. Super high speed response $(t_{PHL}, t_{PLH}: TYP. 45ns at R_L=350\Omega)$
- 2. Isolation voltage between input and output Viso(rms): 2.5kV
- 3. Instantaneous common mode rejection voltage CM_H : TYP. 500V/µs
- 4. LSTTL and TTL compatible output
- 5. Recognized by UL, file No. E64380

Applications

- 1. High speed interfaces for computer peripherals, microcomputer systems
- 2. High speed line receivers
- 3. Noise reduction
- 4. Interfaces for data transmission equipment

Super High Speed Response ***OPIC Photocoupler**



"OPIC" (Optical IC) is a trademark of the SHARP Corporation. An OPIC consists of a light-detecting element and signal-processing circuit integrated onto a single chip.

Absolute Maximum Ratings

	ne maximum Ratings			(Ta=25°C)
	Parameter	Symbol	Rating	Unit
	^{*1} Forward current	IF	20	mA
Input	* ² Peak forward current	I_{FM}	40	mA
	Reverse voltage	VR	5	V
	* ³ Supply voltage	V _{CC}	7	V
	^{*4} Enable voltage	CE	5.5	V
Output	Output voltage	Vo	7	V
	Output current	Io	50	mA
	Output collector power dissipation	Pc	85	mW
*5 Isolation voltage		V _{iso} (rms)	2.5	kV
Operating temperature		Topr	0 to +70	°C
Storage temperature		T _{stg}	-55 to +125	°C
	*6 Soldering temperature	T _{sol}	260	°C

*1 Ta=0 to 70°C

*2 Pulse width≤1ms

- *3 For 1 minute MAX.
- *4 Not exceed 500mV or more than supply voltage (V_{CC})

*5 AC for 1 minute, 40 to 60% RH

*6 2mm or more away from the lead base for 10 seconds

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Apply the specific voltage between all the input electrode pins connected together and all the output electrode pins connected together.

Electro-optical Characteristics

(Ta=0 to +70°C unless otherwise specified)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic (1) output current	Іон	$V_{CC}=5.5V, V_0=5.5V, I_F=250 \mu A, V_E=2.0V$	-	2	250	μA
Logic (0) output voltage	Vol	V _{CC} =5.5V, I _F =5mA, V _{EH} =2.0V, I _{OL} (Sinking)=13mA	-	0.4	0.6	V
Logic (1) enable current	I _{EH}	$V_{CC}=5.5V, V_{E}=2.0V$	-	-0.8	-	mA
Logic (0) enable current	I _{EL}	$V_{CC}=5.5V, V_{E}=0.5V$	-	-1.2	-2.0	mA
Logic (1) supply current	ICCH	V _{CC} =5.5V, I _F =0mA, V _E =0.5V	-	7	15	mA
Logic (0) supply current	I _{CCL}	$V_{CC}=5.5V$, $I_{F}=10mA$, $V_{E}=0.5V$	-	13	18	mA
*7Leak current	I _{I-O}	45%RH, Ta=25°C, t=5s, V _{I-0} =3.0kV DC	-	-	1.0	μA
*7Isolation resistance (input-output)	R _{I-O}	V _{I-O} =500V, Ta=25°C	-	1×10 ¹²	-	Ω
^{*7} Capacitance (input-output)	C _{I-O}	f=1MHz, Ta=25°C	-	0.6	-	pF
^{*8} Input forward voltage	VF	I _F =10mA, Ta=25°C	-	1.6	1.75	V
Input reverse voltage	BVR	$I_R=10\mu A$, $Ta=25^{\circ}C$	5	_	_	V
Input capacitance	CIN	$V_{F}=0, f=1MHz$	-	60	-	pF

*7 Measured as 2-pin element. Connect pins 2 and 3 connect pins 5,6,7 and 8.

*8 At I_F=10mA, V_F decreases at the rate of 1.6mV/°C if the temperature goes up.

Switching Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
*9 Propagation delay time Output $(0) \rightarrow (1)$	t _{PLH}	Ta=25°C, RL=350Ω, CL=15pF, IF=7.5mA	-	45	75	ns
*9 Propagation delay time Output $(1) \rightarrow (0)$	t PHL	Ta=25°C, RL=350Ω, CL=15pF, IF=7.5mA	-	45	75	ns
Output rise-fall time (10 to 90%)	t _r , t _f	R _L =350Ω, C _L =15pF, I _F =7.5mA	-	20, 30	-	ns
^{*10} Enable propagation delay time $(1) \rightarrow (0)$	telh	RL=350Ω, CL=15pF, IF=7.5mA, VEH=3.0V, VEL=0.5V	-	40	-	ns
*10 Enable propagation delay time $(0) \rightarrow (1)$	t _{EHL}	RL=350Ω, CL=15pF, IF=7.5mA, VEH=3.0V, VEL=0.5V	-	15	-	ns
*11 Instantaneous common mode rejection voltage "Output (1)"	CM _H	V_{CM} =10V, R _L =350 Ω , V ₀ (min.)=2V, I _F =0mA	-	500	-	$V/\mu s$
*11 Instantaneous common mode rejection voltage "Output (0) "	CML	V_{CM} =10V, R L=350 Ω , V ₀ (max.)=0.8V, I F=5mA	-	-500	-	$V/\mu s$

*9 Refer to the Fig. 1.

*10 Refer to the Fig. 2.

*11 CM_H represents a common mode voltage variation that can hold the output above (1) level (V_0 >2.0V).

 CM_L represents a common mode voltage variation that can hold the output above (0) level (V₀<0.8V)

Recommended Operating Conditions

Parameter	Symbol	MIN.	MAX.	Unit
Low level input current	I _{FL}	0	250	μΑ
High level input current	I _{FH}	7.0	15	mA
High level enable voltage	VEH	2.0	Vcc	V
Low level enable voltage	V _{EL}	0	0.8	V
Supply voltage	Vcc	4.5	5.5	V
Fanout (TTL load)	N	-	8	_
Operating temperature	Topr	0	70	°C

1. No necessary external pull-up resistor to hold enable input at high level.

2. Connect a ceramic by-pass capacitor (0.01 to 0.1μ F) between V_{CC} and GND at the position within 1cm from pin.

Circuit Block Diagram



Truth Table

Input	Enable	Output		
Н	Н	L		
L	Н	Н		
Н	L	Н		
L	L	Н		
L:Logic (0) H:Logic (1)				

Note) Typical values are all at $V_{CC}=5V$, $T_a=25^{\circ}C$



Fig.1 Test Circuit for Propagation Delay Time





















350mV(I_F=7.5mA)











Fig. 7 Low Level Output Voltage vs. Ambient Temperature



Fig. 8-b Output Voltage vs. Forward Current (Ambient Temp. Characteristics)



Fig. 10 Propagation Delay Time vs. Ambient Temperature





Fig. 11 Rise Time, Fall Time vs. Ambient Temperature

Precaution for Use

(1) Handle this product the same as with other integrated circuits against static electricity.

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