IRF820R, IRF821R, IRF822R, IRF823R

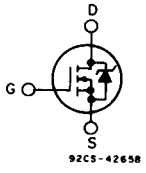
File Number **2020**

Avalanche Energy Rated N-Channel Power MOSFETs

2.0A and 2.5A, 450V-500V
$r_{DS}(on) = 3.0\Omega$ and 4.0Ω

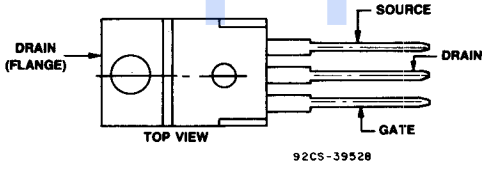
Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-220AB

The IRF820R, IRF821R, IRF822R and IRF823R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

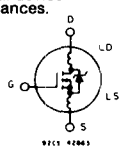
The IRF-types are supplied in the JEDEC TO-220AB plastic package.

Absolute Maximum Ratings

Parameter		IRF820R	IRF821R	IRF822R	IRF823R	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	500	450	500	450	V
I_D @ $T_C = 25°C$	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ $T_C = 100°C$	Continuous Drain Current	1.5	1.5	1.0	1.0	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	210				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF820R IRF822R	500	—	—	V	V_{GS} = 0V
		IRF821R IRF823R	450	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF820R IRF821R	2.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF822R IRF823R	2.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF820R IRF821R	—	2.5	3.0	Ω	V_{GS} = 10V, I_D = 1.0A
		IRF822R IRF823R	—	3.0	4.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.75	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 1.0A
C_{iss}	Input Capacitance	ALL	—	300	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	75	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	30	60	ns	$V_{DD} \approx 0.5BV_{DSS}$, I_D = 1.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	30	60	ns	
t_f	Fall Time	ALL	—	15	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	26	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	5.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

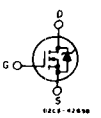


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF820R IRF821R	—	—	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF822R IRF823R	—	—	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF820R IRF821R	—	—	10	A	
		IRF822R IRF823R	—	—	8.0	A	
V_{SD}	Diode Forward Voltage ②	IRF820R IRF821R	—	—	1.6	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
		IRF822R IRF823R	—	—	1.5	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	600	—	ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	3.5	—	μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 5V, starting T_J = 25°C, L = 60mH, R_{gs} = 25Ω, I_{peak} = 2.5A. See figures 15, 16.

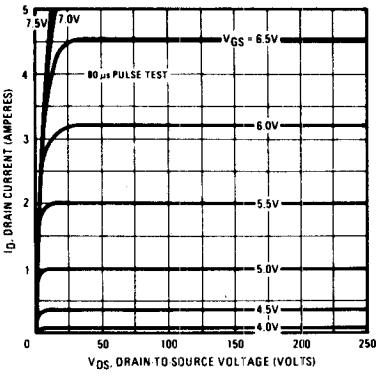


Fig. 1 – Typical Output Characteristics

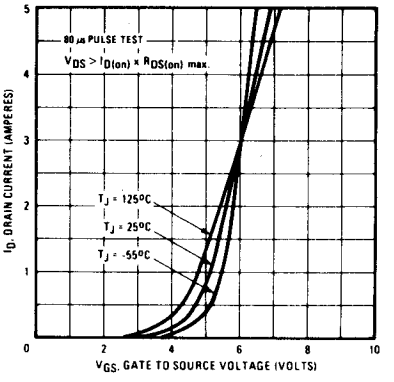


Fig. 2 – Typical Transfer Characteristics

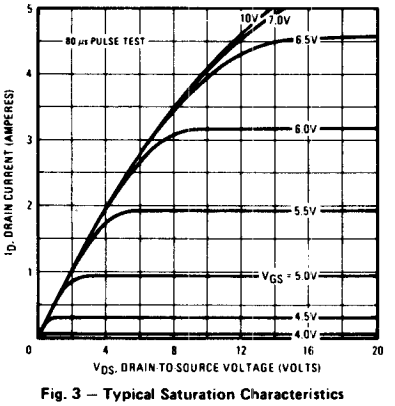


Fig. 3 – Typical Saturation Characteristics

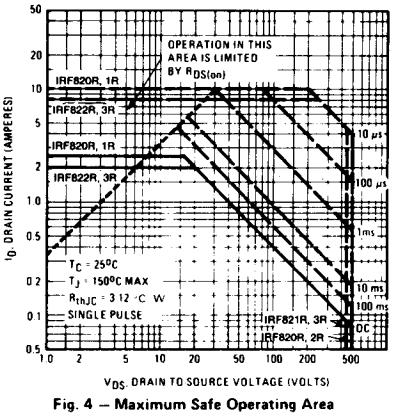


Fig. 4 – Maximum Safe Operating Area

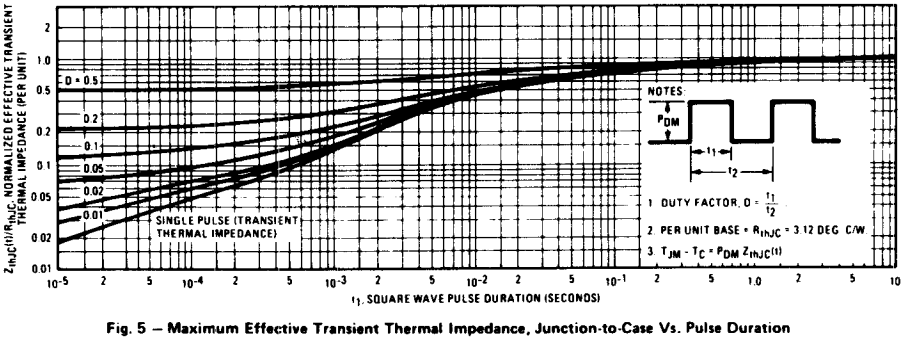


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

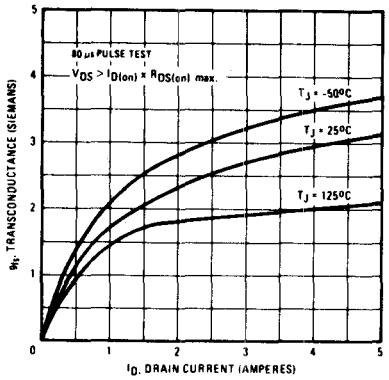


Fig. 6 – Typical Transconductance Vs. Drain Current

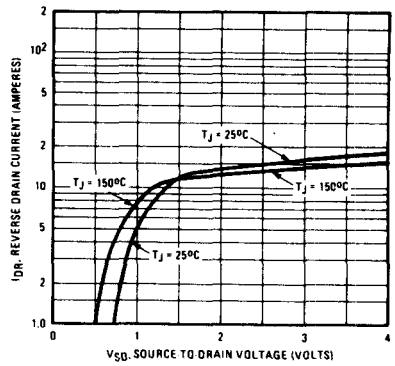


Fig. 7 – Typical Source-Drain Diode Forward Voltage

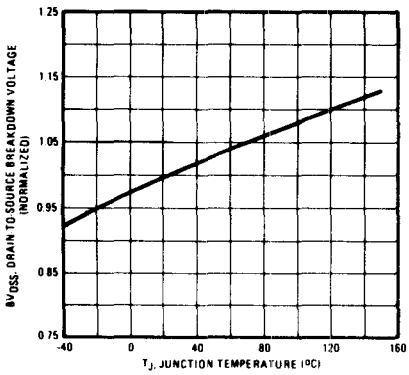


Fig. 8 – Breakdown Voltage Vs. Temperature

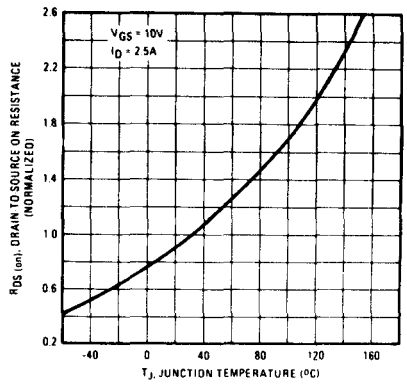


Fig. 9 – Normalized On-Resistance Vs. Temperature

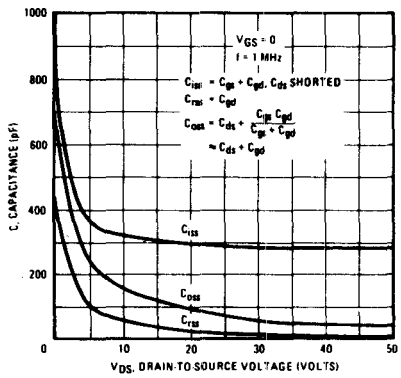


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

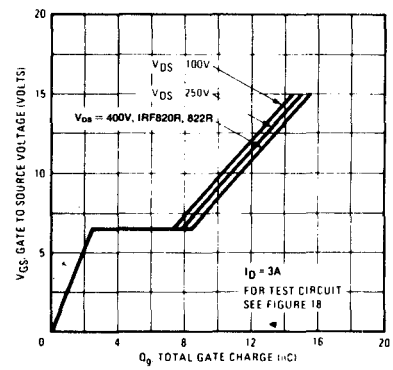


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

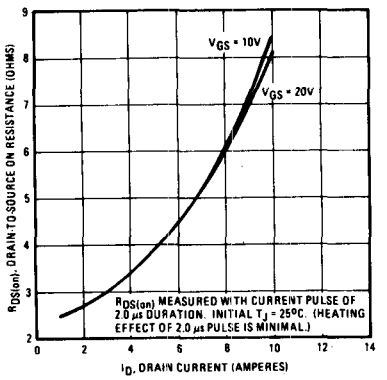


Fig. 12 – Typical On-Resistance Vs. Drain Current

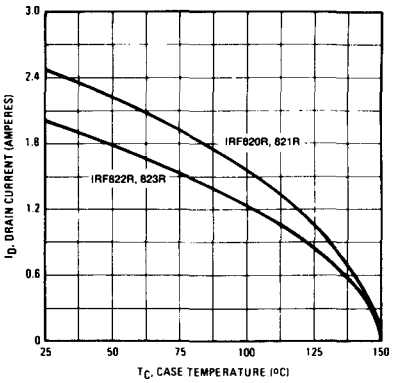


Fig. 13 – Maximum Drain Current Vs. Case Temperature

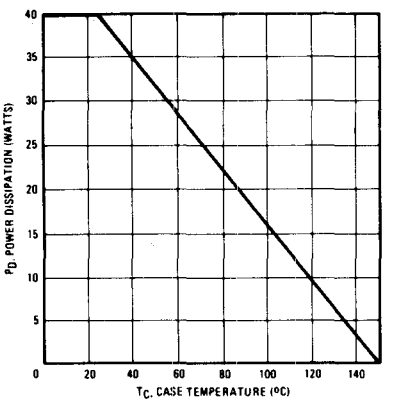


Fig. 14 – Power Vs. Temperature Derating Curve

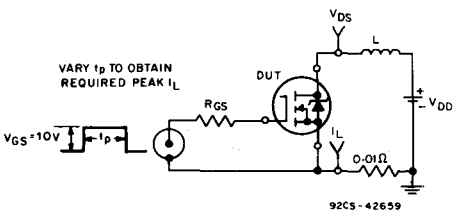


Fig. 15 — Unclamped Energy Test Circuit

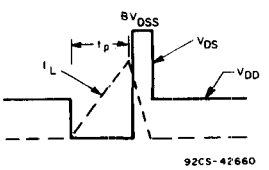


Fig. 16 — Unclamped Energy Waveforms

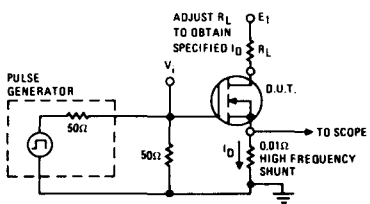


Fig. 17 – Switching Time Test Circuit

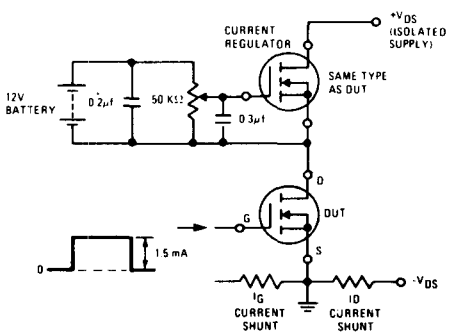


Fig. 18 – Gate Charge Test Circuit