MOTOROLA

SG1525A/SG1527A
SG2525A/SG2527A
SG3525A/SG3527A

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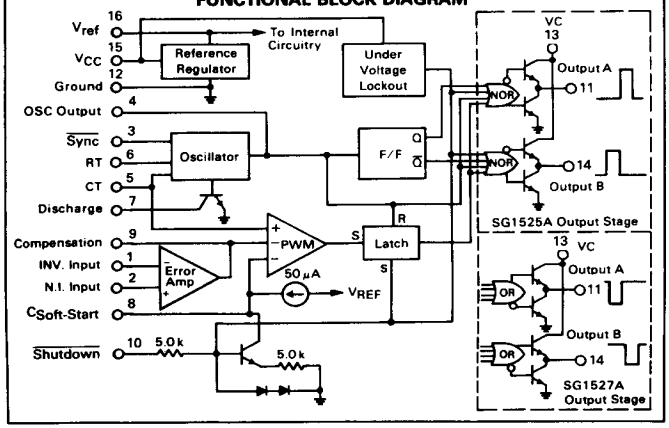
PULSE WIDTH MODULATOR CONTROL CIRCUITS

The SG1525A/1527A series of pulse width modulator control-circuits offer improved performance and lower external parts count when implemented for controlling all types of switching power supplies. The on-chip +5.1 volt reference is trimmed to ±1% and the error amplifier has an input common-mode voltage range that includes the reference voltage, thus eliminating the need for external divider resistors. A sync input to the oscillator enables multiple units to be slaved or a single unit to be synchronized to an external system clock. A wide range of dead time can be programmed by a single resistor connected between the C_T and Discharge pins. These devices also feature built-in soft-start circuitry, requiring only an external timing capacitor. A shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. The under voltage lockout inhibits the outputs and the changing of the soft-start capacitor when V_{CC} is below nominal. The output stages are totem-pole design capable of sinking and sourcing in excess of 200 mA. The output stage of the SG1525A series features NOR Logic resulting in a low output for an off state while the SG1527A series utilizes OR Logic which gives a high output when off. The devices are available in Military, Industrial and Commercial temperature ranges.

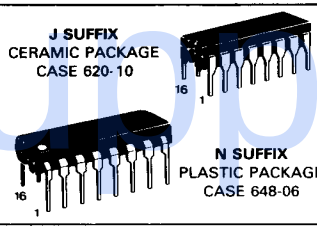
- 8.0 to 35 Volt Operation
- 5.1 Volt ± 1.0% Trimmed Reference
- 100 Hz to 400 kHz Oscillator Range
- Separate Oscillator Sync Pin
- Adjustable Dead Time Control
- Input Undervoltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Pulse-by-Pulse Shutdown
- Dual Source/Sink Outputs: ± 400 mA Peak

FUNCTIONAL BLOCK DIAGRAM

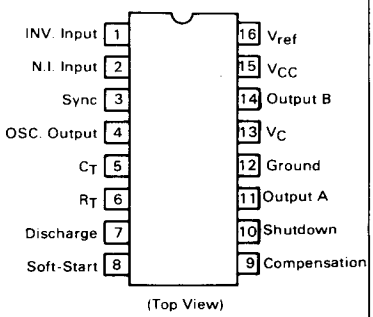


PULSE WIDTH MODULATOR CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
SG1525AJ	−55 to +125°C	Ceramic DIP
SG1527AJ	−55 to +125°C	Ceramic DIP
SG2525AJ	−25 to +85°C	Ceramic DIP
SG2525AN	−25 to +85°C	Plastic DIP
SG2527AJ	−25 to +85°C	Ceramic DIP
SG2527AN	−25 to +85°C	Plastic DIP
SG3525AJ	0 to +70°C	Ceramic DIP
SG3525AN	0 to +70°C	Plastic DIP
SG3527AJ	0 to +70°C	Ceramic DIP
SG3527AN	0 to +70°C	Plastic DIP

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs	—	-0.3 to +5.5	V
Analog Inputs	—	-0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±500	mA
Reference Output Current	I_{ref}	50	mA
Oscillator Charging Current	—	5.0	mA
Power Dissipation (Plastic & Ceramic Package) T_A = +25°C (Note 2) T_C = +25°C (Note 3)	P_D	 1000 2000	mW
Thermal Resistance Junction to Air Plastic and Ceramic Package	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction to Case Plastic and Ceramic Package	$R_{\theta JC}$	60	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	-65 to +150 -55 to +125	°C
Lead Temperature (Soldering, 10 Seconds)	T_{Solder}	+300	°C

NOTES:
1. Values beyond which damage may occur
2. Derate at 10 mW/°C for ambient temperatures above +50°C
3. Derate at 16 mW/°C for case temperatures above +25°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	+8.0	+35	Vdc
Collector Supply Voltage	V_C	+4.5	+35	Vdc
Output Sink/Source Current (Steady State) (Peak)	I_O	 0 0	 ±100 ±400	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.1	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	0.2	μF
Deadtime Resistor Range	R_D	0	500	Ω
Operating Ambient Temperature Range SG1525A, SG1527A SG2525A, SG2527A SG3525A, SG3527A	T_A	 -55 -25 0	 +125 +85 +70	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, T_A = T_{low} to T_{high} [Note 4], unless otherwise specified)

Characteristic	Symbol	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (T_J = +25°C)	V_{ref}	5.05	5.10	5.15	5.00	5.10	5.20	Vdc
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	—	10	20	—	10	20	mV
Load Regulation (0 mA ≤ I_L ≤ 20 mA)	Reg_{load}	—	20	50	—	20	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T$	—	20	—	—	20	—	mV
Total Output Variation Includes Line and Load Regulation over Temperature	ΔV_{ref}	5.00	—	5.20	4.95	—	5.25	Vdc
Short Circuit Current (V_{ref} = 0 V, T_J = +25°C)	I_{SC}	—	80	100	—	80	100	mA
Output Noise Voltage (10 Hz ≤ f ≤ 10 kHz, T_J = +25°C)	V_n	—	40	200	—	40	200	μV_{rms}
Long Term Stability (T_J = +125°C) (Note 5)	S	—	20	50	—	20	50	mV khr
OSCILLATOR SECTION (Note 6, unless otherwise specified)								
Initial Accuracy (T_J = +25°C)	—	—	±2.0	±6.0	—	±2.0	±6.0	%
Frequency Stability with Voltage (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	—	±0.3	±1.0	—	±1.0	±2.0	%
Frequency Stability with Temperature	$\frac{\Delta f_{osc}}{\Delta T}$	—	±3.0	—	—	±3.0	—	%
Minimum Frequency (R_T = 150 kΩ, C_T = 0.2 μF)	f_{min}	—	50	—	—	50	—	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 1.0 nF)	f_{max}	400	—	—	400	—	—	kHz
Current Mirror (I_{R_T} = 2.0 mA)	—	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude	—	3.0	3.5	—	3.0	3.5	—	V
Clock Width (T_J = +25°C)	—	0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold	—	1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current (Sync Voltage = +3.5 V)	—	—	1.0	2.5	—	1.0	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = +5.1 V)								
Input Offset Voltage	V_{IO}	—	0.5	5.0	—	2.0	10	mV
Input Bias Current	I_{IB}	—	1.0	10	—	1.0	10	μA
Input Offset Current	I_{IO}	—	—	1.0	—	—	1.0	μA
DC Open Loop Gain (R_L ≥ 10 MΩ)	A_{VOL}	60	75	—	60	75	—	dB
Low Level Output Voltage	V_{OL}	—	0.2	0.5	—	0.2	0.5	V
High Level Output Voltage	V_{OH}	3.8	5.6	—	3.8	5.6	—	V
Common Mode Rejection Ratio (+1.5 V ≤ V_{CM} ≤ +5.2 V)	CMRR	60	75	—	60.	75	—	dB
Power Supply Rejection Ratio (+8.0 V ≤ V_{CC} ≤ +35 V)	PSRR	50	60	—	50	60	—	dB
PWM COMPARATOR SECTION								
Minimum Duty Cycle	DC_{min}	—	—	0	—	—	0	%
Maximum Duty Cycle	DC_{max}	45	49	—	45	49	—	%
Input Threshold, Zero Duty Cycle (Note 6)	V_{TH}	0.6	0.9	—	0.6	0.9	—	V
Input Threshold, Maximum Duty Cycle (Note 6)	V_{TH}	—	3.3	3.6	—	3.3	3.6	V
Input Bias Current	I_{IB}	—	0.05	1.0	—	0.05	1.0	μA

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ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
		Min	Typ	Max	Min	Typ	Max	
SOFT-START SECTION								
Soft-Start Current ($V_{shutdown}$ = 0 V)	—	25	50	80	25	50	80	μA
Soft-Start Voltage ($V_{shutdown}$ = 2.0 V)	—	—	0.4	0.6	—	0.4	0.6	V
Shutdown Input Current ($V_{shutdown}$ = 2.5 V)	—	—	0.4	1.0	—	0.4	1.0	mA
OUTPUT DRIVERS (Each Output, V_{CC} = +20 V)								
Output Low Level (I_{sink} = 20 mA) (I_{sink} = 100 mA)	V_{OL}	 — —	 0.2 1.0	 0.4 2.0	 — —	 0.2 1.0	 0.4 2.0	V
Output High Level (I_{source} = 20 mA) (I_{source} = 100 mA)	V_{OH}	 18 17	 19 18	 — —	 18 17	 19 18	 — —	V
Under Voltage Lockout (V8 and V9 = High)	V_{UL}	6.0	7.0	8.0	6.0	7.0	8.0	V
Collector Leakage, V_C = +35 V (Note 7)	$I_{C(leak)}$	—	—	200	—	—	200	μA
Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	—	100	600	—	100	600	ns
Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	—	50	300	—	50	300	ns
Shutdown Delay (V_{SD} = +3.0 V, C_S = 0, T_J = +25°C)	t_{ds}	—	0.2	0.5	—	0.2	0.5	μs
Supply Current, (V_{CC} = +35 V)	I_{CC}	—	14	20	—	14	20	mA

NOTES:

4. T_{low} = −55°C for SG1525A/1527A
   −25°C for SG2525A/2527A
   0°C for SG3525A/3527A
   T_{high} = +125°C for SG1525A/1527A
   +85°C for SG2525A/2527A
   +70°C for SG3525A/3527A
5. Since long term stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Tested at f_{OSC} = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 μF, R_D = 0 Ω).
7. Applies to SG1525A/2525A/3525A only, due to polarity of output pulses.

APPLICATION INFORMATION

SHUTDOWN OPTIONS
(See Block Diagram, front page)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150 μA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

TYPICAL CHARACTERISTICS

FIGURE 1 — SG1525A OSCILLATOR SCHEMATIC

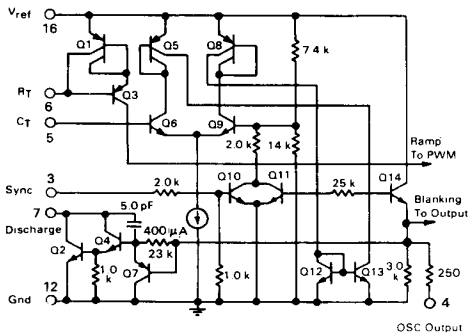

FIGURE 2 — OSCILLATOR CHARGE TIME versus R_T

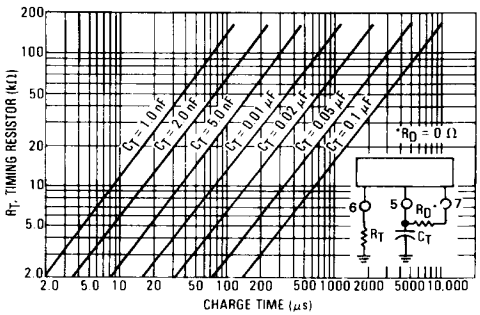

FIGURE 3 — OSCILLATOR DISCHARGE TIME versus R_D

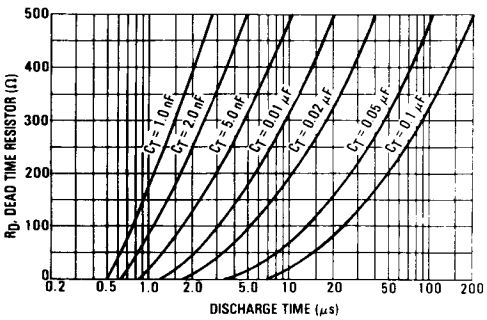

FIGURE 4 — SG1525A ERROR AMPLIFIER SCHEMATIC

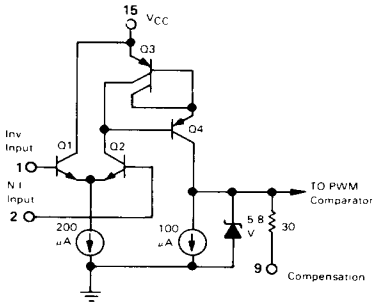

FIGURE 5 — ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE

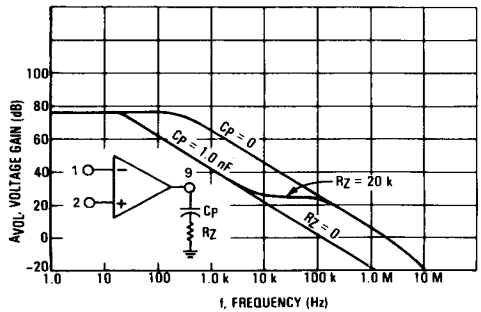

FIGURE 6 — SG1525A OUTPUT CIRCUIT (1/2 CIRCUIT SHOWN)

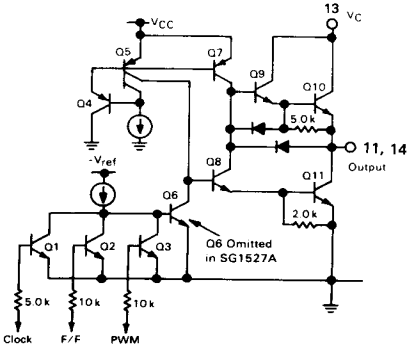

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FIGURE 7 — SG1525A/2525A/3525A
OUTPUT SATURATION CHARACTERISTICS

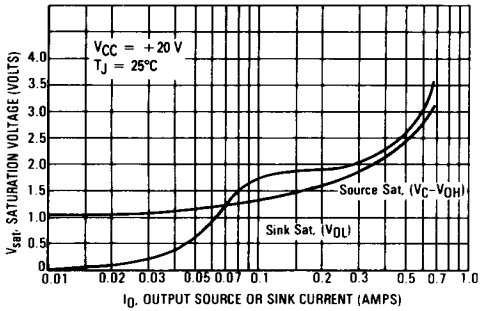
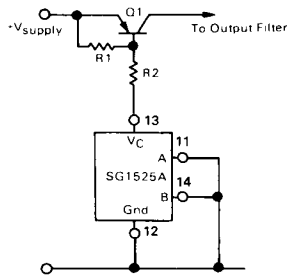
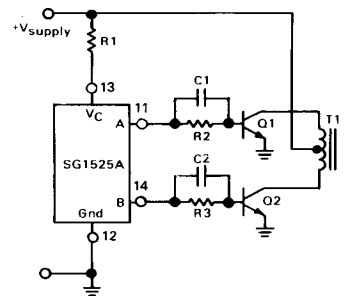


FIGURE 8 — SINGLE ENDED SUPPLY



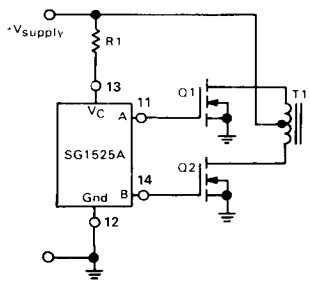
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

FIGURE 9 — PUSH-PULL CONFIGURATION



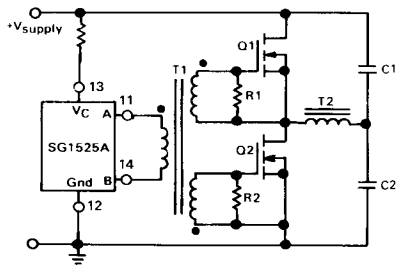
In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.

FIGURE 10 — DRIVING POWER FETS



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

FIGURE 11 — DRIVING TRANSFORMERS IN A HALF-BRIDGE CONFIGURATION



Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

FIGURE 12 — LAB TEST FIXTURE