File Number **2031**

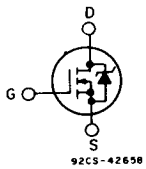
IRFF430R, IRFF431R, IRFF432R, IRFF433R

Avalanche Energy Rated N-Channel Power MOSFETs

2.25A and 2.75A, 450V-500V
$r_{DS}(on) = 1.5\Omega$ and 2.0Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE



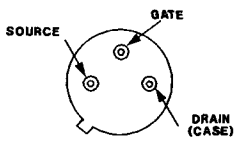
TERMINAL DIAGRAM

6

The IRFF430R, IRFF431R, IRFF432R and IRFF433R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

Absolute Maximum Ratings

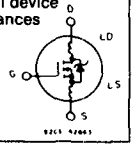
Parameter		IRFF430R	IRFF431R	IRFF432R	IRFF433R	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage ($R_{GS} = 20\ K\Omega$) ①	500	450	500	450	V
I_D @ $T_C = 25°C$	Continuous Drain Current	2.75	2.75	2.25	2.25	A
I_{DM}	Pulsed Drain Current ③	11	11	9.0	9.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ $T_C = 25°C$	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/°C
E_{as}	Single Pulse Avalanche Energy Rating ④	300				mj
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFF430R, IRFF431R, IRFF432R, IRFF433R

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF430R IRFF432R	500	—	—	V	V_{GS} = 0V
		IRFF431R IRFF433R	450	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250μ A
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF430R IRFF431R	2.75	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, V_{GS} = 10V
		IRFF432R IRFF433R	2.25	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF430R IRFF431R	—	1.3	1.5	Ω	V_{GS} = 10V, I_D = 1.5A
		IRFF432R IRFF433R	—	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.5	—	S(℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)max.}$, I_D = 1.5A
C_{iss}	Input Capacitance	ALL	—	600	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	100	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	30	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	$V_{DD} \simeq$ 225V, I_D = 1.5A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	55	ns	
t_f	Fall Time	ALL	—	—	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	22	39	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	11	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	11	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	5.0	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF430R IRFF431R	—	—	2.75	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF432R IRFF433R	—	—	2.25	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF430R IRFF431R	—	—	11	A	
		IRFF432R IRFF433R	—	—	9.0	A	
V_{SD}	Diode Forward Voltage ②	IRFF430R IRFF431R	—	—	1.4	V	T_C = 25°C, I_S = 2.75A, V_{GS} = 0V
		IRFF432R IRFF433R	—	—	1.3	V	T_C = 25°C, I_S = 2.25A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	800	—	ns	T_J = 150°C, I_F = 2.75A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	4.6	—	μC	T_J = 150°C, I_F = 2.75A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).
④ V_{DD} = 50V, starting T_J = 25°C, L = 69.42mH, R_{gs} = 50Ω, I_{peak} = 2.75A.

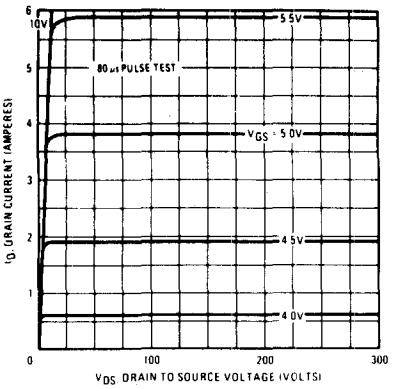


Fig. 1 - Typical output characteristics.

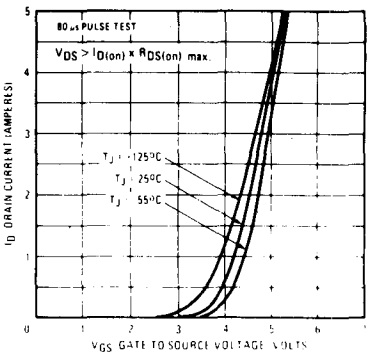


Fig. 2 - Typical transfer characteristics.

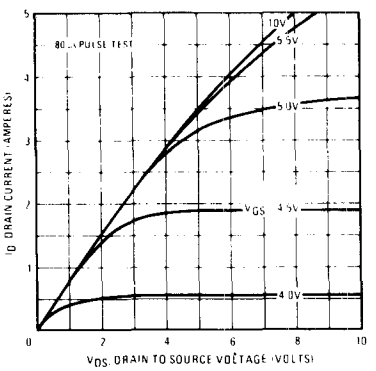


Fig. 3 - Typical saturation characteristics.

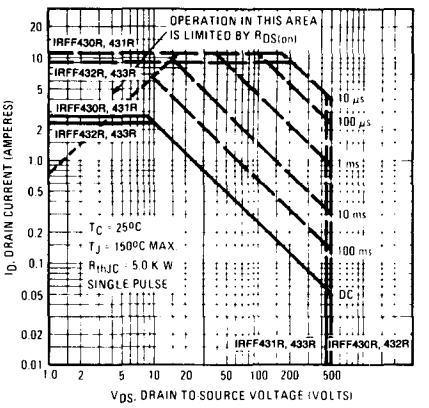


Fig. 4 - Maximum safe operating area.

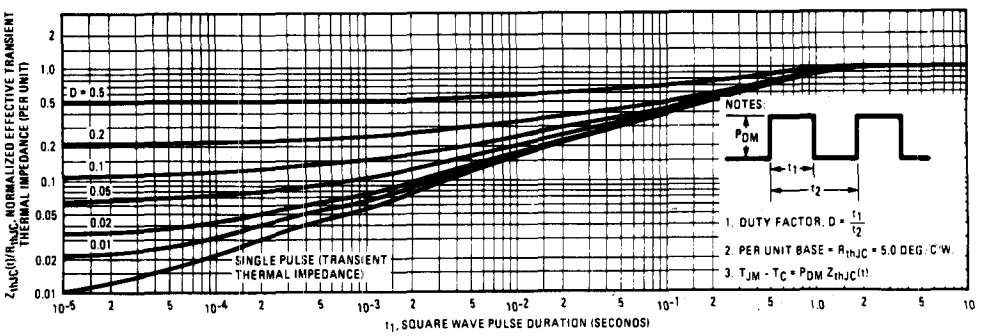


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

IRFF430R, IRFF431R, IRFF432R, IRFF433R

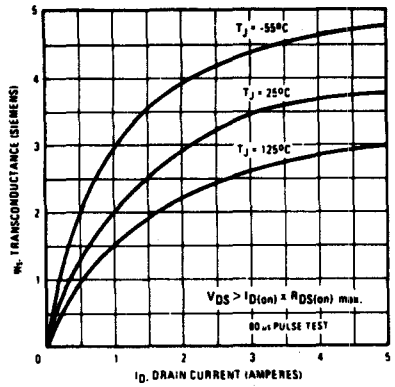


Fig. 6 - Typical transconductance vs. drain current.

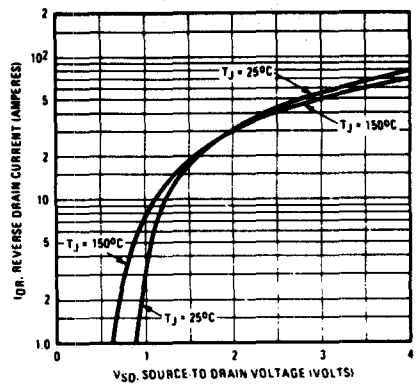


Fig. 7 - Typical source-drain diode forward voltage.

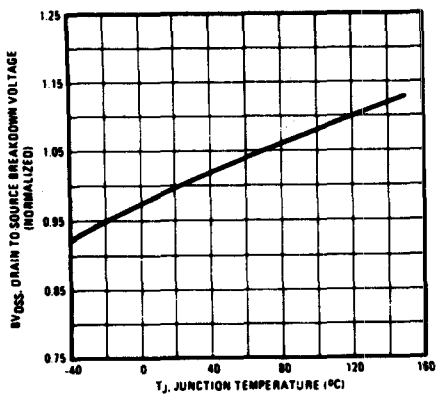


Fig. 8 - Breakdown voltage vs. temperature.

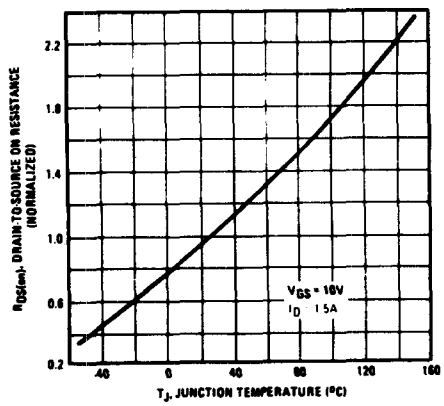


Fig. 9 - Normalized on-resistance vs. temperature.

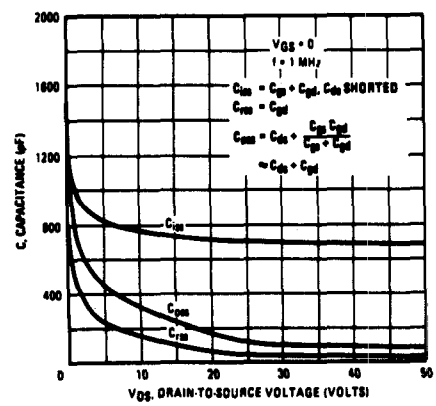


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

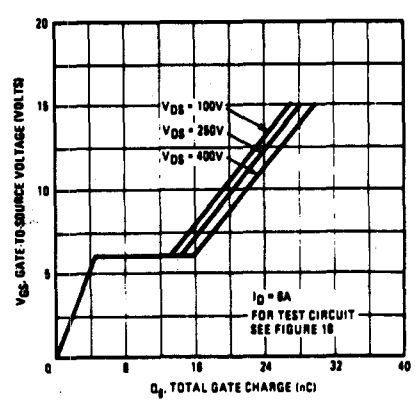


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

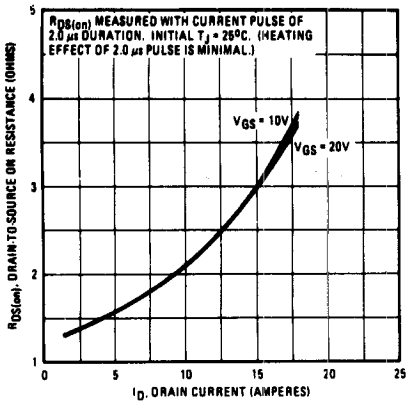


Fig. 12 - Typical on-resistance vs. drain current.

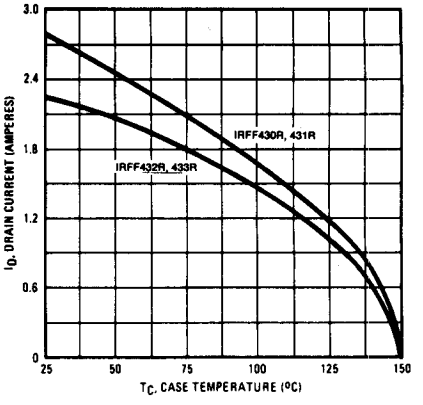


Fig. 13 - Maximum drain current vs. case temperature.

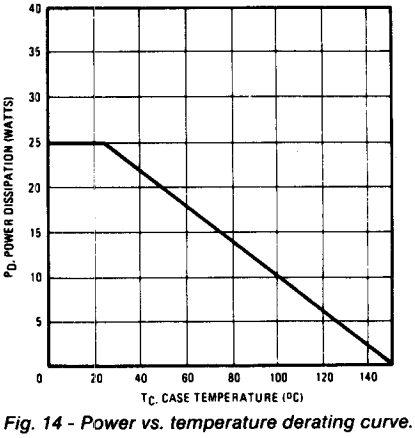


Fig. 14 - Power vs. temperature derating curve.

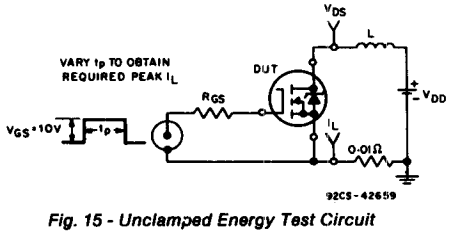


Fig. 15 - Unclamped Energy Test Circuit

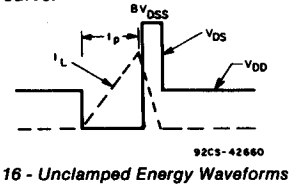


Fig. 16 - Unclamped Energy Waveforms

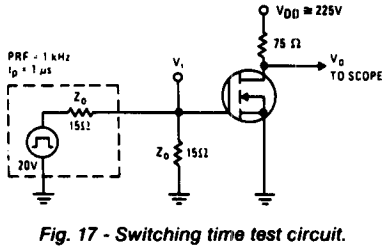


Fig. 17 - Switching time test circuit.

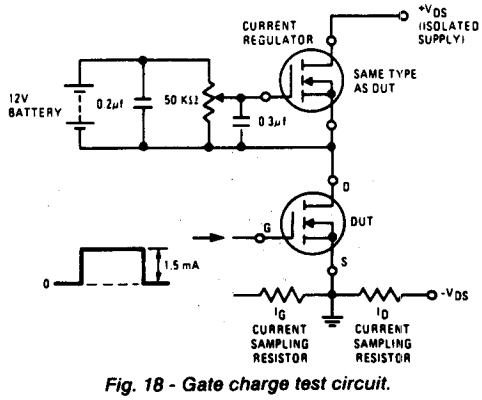


Fig. 18 - Gate charge test circuit.