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SCR AL3201 DSP

General Description

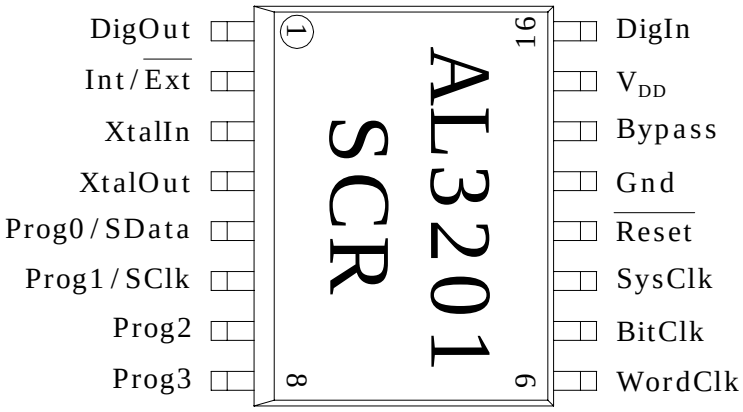
The AL3201 (SCR, or Single Chip Reverb) is a one chip reverb solution that is compact, easy to use, and yet quite powerful. Built-in DRAM eliminates the need for wide bus connections to external RAM, and the choice of built-in programs and a user programmable RAM allows instant usability or custom program design.

Features

- 16 internal ROM programs consisting of halls, rooms, plates, delays, chorus, flange, vocal cancel, and rotary speaker emulation.
- Serially programmable SRAM (Writable Control Store – WCS) for program development or dynamically changing programs
- Programs run at 128 instructions per word clock. (6 MIPS @ 48kHz sampling frequency.)
- 32k location DRAM provides over 0.68s of delay at 48kHz sampling frequency.
- Internal crystal oscillator circuit eliminates need for discrete external passive components.
- Internal voltage regulators allow operation at both 5V and 3.3V V_{DD}.
- Internal 1000pF bypass capacitor to reduce voltage swings at the rails.

Applications

- Personal stereos with reverb functions.
- Extremely portable guitar effects boxes.
- Karaoke machines utilizing the vocal cancel program.
- Hardware reverb effects for computer sound cards.
- Ambience settings for car stereos.



16 pin SOIC
300 mils wide

DS3201-0802

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Electrical Characteristics and Operating Conditions

Parameter	Description	Condition	Min	Typ	Max	Units
Electrical Characteristics and Operating Conditions						
V_{DD}	Supply Voltage		3.0/4.5	3.3/5.0	3.6/5.5	V
I_{DD}	Supply Current : SCR		6/9	7/10	8/11	mA
Gnd	Ground	Note 3	-	0.0	-	V
F_S	Sample rate		24 [1]	48	50 [1]	kHz
Temp	Temperature		0	25	70	°C
Outputs (DigOut, SysClk, BitClk, WordClk)						
V_{OH}	Logical "1" output voltage	Unloaded	0.9 V_{DD}	V_{DD}	-	V
V_{OL}	Logical "0" output voltage	Unloaded	-	0	0.05 V_{DD}	V
I_{OH}	Logical "1" output current	V_{DD}=5V V_O=4.5V	-	-	-8.0	mA
I_{OL}	Logical "0" output current	V_{DD}=5V V_O=0.4V	-	-	8.0	mA
Inputs (DigIn, Int/$\overline{\text{Ext}}$, Prog0/Sdata, Prog1/SClk, Prog2, Prog3, $\overline{\text{Reset}}$) Notes 2,4						
V_{IH}	Logical "1" input voltage		2.5	-	V_{DD}	V
V_{IL}	Logical "0" input voltage		0	-	0.5	V
I_{IH}	Logical "1" input current	V_{DD}=V_{IH}=5V	-	-	2	µA
I_{IL}	Logical "0" input current	No pullup pin	-	-	2	µA
I_{ILP}	Logical "0" input current	Pullup pin, Vin=0	83	167	333	µA
C_{IN}	Input Capacitance		-	2.0	-	pF

Note:

1. Changing the sample rate (by changing the crystal frequency) will change the maximum delay available through the DRAM proportionally. Low sample rates require more refresh instructions.
2. XtalIn, XtalOut are special pins designed to be connected to a crystal. XtalOut is a relatively weak pin (about 0.2 mA) and should not be used to drive external circuits. Instead of using a crystal, XtalIn may be driven by a standard V_{DD} to Gnd logic signal, but the logic levels are ***not specified***.
3. All other voltages are relative to Gnd.
4. Bypass (pin 14) must never exceed 3.6V

Pin Descriptions: AL3201 SCR

(*: Pullup to V_{DD} via nominal internal 30kΩ resistor)

Pin #	Name	Pin Type	Description
1	DigOut	Output	Digital serial output for stereo DAC.
2	Int/$\overline{\text{Ext}}$	Input*	Internal/external program selection. 1:Internal, 0:External.
3	XtalIn	Input	12.288MHz crystal input.
4	XtalOut	Output	12.288MHz crystal output.
5	Prog0/SData	Bidirectional*	Internal program select 0 / serial interface data line.
6	Prog1/SClk	Input*	Internal program select 1 / serial interface clock line.
7	Prog2	Input*	Internal program select 2.
8	Prog3	Input*	Internal program select 3.
9	WordClk	Output	Word clock output.
10	BitClk	Output	Bit clock output.
11	SysClk	Output	System clock output.
12	$\overline{\text{Reset}}$	Input	Active low reset.
13	Gnd	Ground	Ground connection.
14	Bypass	Bidirectional	Connect 0.1µF bypass capacitor to Gnd for internal +3.3V regulator.
15	V_{DD}	Power	+5V/+3.3V V_{DD} power pin. Connect 0.1µF capacitor to Gnd.
16	DigIn	Input	Digital serial input from stereo ADC.

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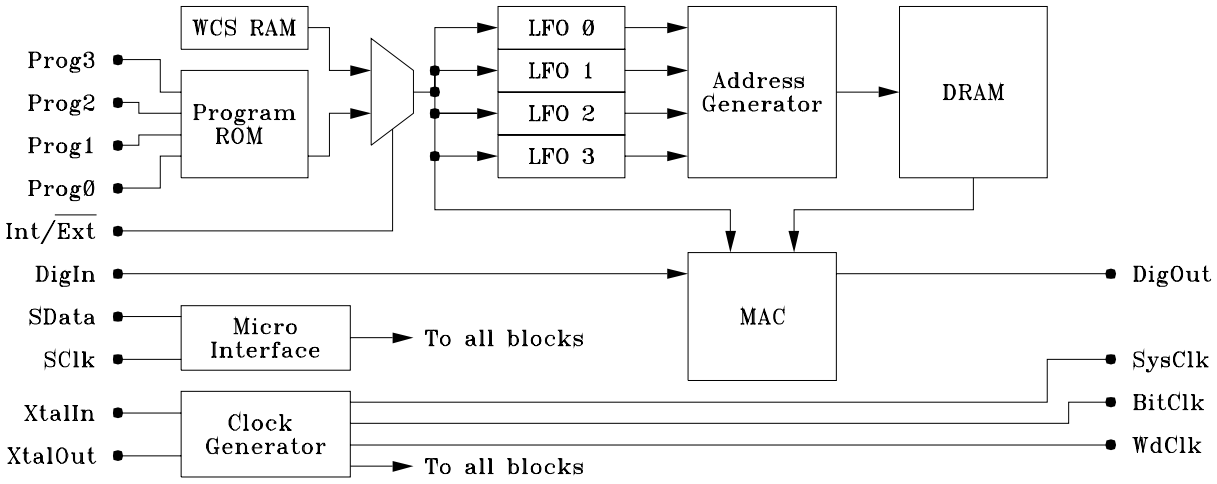
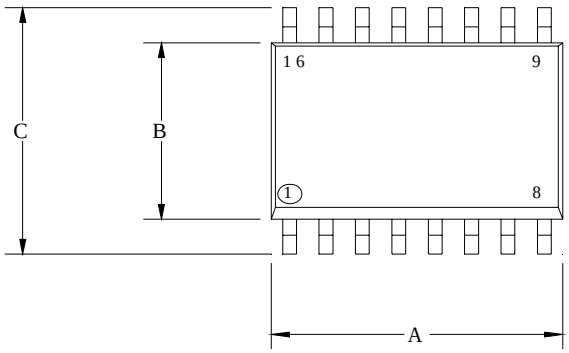
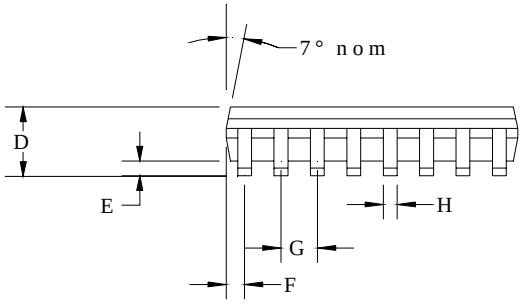
Block Diagram



Mechanical Specification

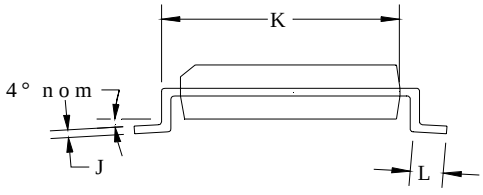




Dimensions (Typical)	Inches	Millimeters
A	.406”	10.31
B	.295”	7.49
C	.407”	10.34
D	.100”	2.50
E	.008”	0.20
F	.025”	0.64
G	.050”	1.27
H	.017”	0.42
J	.011”	0.27
K	.340”	8.66
L	.033”	0.83

Notes:

1) Dimension “A” does not include mold flash, protrusions or gate burrs.



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Internal Programs

The SCR comes with 16 internal ROM programs ready to go, utilizing the skills and techniques of the Alesis Studio Electronics effects processor programmers. By setting the chip to internal mode, the four program pins may be used to select between the different algorithms.

Program List

Prg	Name	Description
0*	Delay 1	125ms slapback delay for vocals and guitars.
1	Chorus/Room 2	Auto-wah guitar effect with reverb for lead instruments.
2	Hall 2	Warm hall for acoustic guitars, pianos, and vocals.
3	Vocal Cancel	Removes lead vocals from many stereo recordings.
4*	Delay 2	190ms delay for percussive arpeggios.
5	Chorus/Room 1	Chorus with reverb for guitars, synths, and pianos.
6	Hall 1	Bright hall reverb for drums, guitars, and vocals.
7	Rotary Speaker	Rotary speaker emulation for organs and guitars.
8	Flange	Stereo flanger for jet wash effects.
9	Plate 2	Sizzling bright plate reverb for vocals and drums.
10	Room 1	Hardwood studio for acoustic instruments.
11	Plate 1	Classic plate reverb for lead vocals and instruments.
12*	Chorus	Stereo chorus for guitars and pianos.
13	Plate 3	Short vintage plate reverb for snares and guitars.
14	Room 2	Ambience for acoustic mixes and synth sounds.
15	Room 3	Warm room for guitars and rhythm instruments.

Note: The unusual ordering of the programs allows a 16-position rotary switch's Gray code output to be connected to the program pins. The sequence of programs is then Halls 1-2, Rooms 1-3, Plates 1-3, Chorus, Flange, Delays 1-2, Chorus/Rooms 1-2, Vocal Cancel, and Rotary Speaker.

* **WARNING**

Programs 0, 4, and 12 do not meet refresh requirements. Do not depend upon these programs working in any application.

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Programming the RAM

Alongside the 16 internal programs is an externally programmable SRAM that is easily accessible through the serial clock and data pins. By setting the chip to external mode, the SClk and SData pins become available for serial communication. Except for its external programmability, there is no functional difference between the SRAM and the internal ROMs.

Memory Map

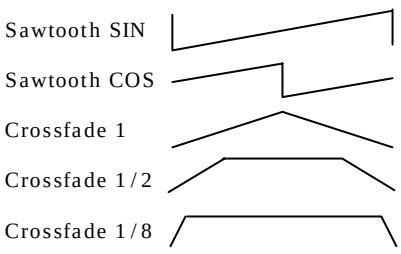
Addr	Name		
0:127	WCS RAM	Addr	Name
		0:3	LFO Coefficients
		4:127	MAC Instructions
128	Control/Status 0		
129	Control/Status 1		

A simple assembly language is available for writing programs. With the assembler and loader software available from the Alesis Semiconductor website, programs may be developed on the PC and downloaded into the chip. Please refer to the assembly language guide for a full description.

LFO Coefficient Word

Bit #	Description		
31	P: Pitch shift mode select (S must be set). [1]		
30	S: Sine/triangle select. 1:Triangle; 0: Sine.		
29:28	X[1:0]: Crossfade coefficient select. Value indicates the fraction of a half sawtooth period used in crossfading.	X[1:0]	Xfade
		11	1/16
		10	1/8
		01	1/2
		00	1
27:15	F[12:0]: Frequency coefficient, unsigned.		
14:0	A[14:0]: Amplitude coefficient, unsigned.		

Note:
If set, the output waveform is a sawtooth with double the triangle wave's frequency.



The first four instructions in the WCS RAM set the parameters for the four LFOs. The sinusoid generated by the LFOs is of the formula Asin(nF/M) or Acos(nF/M), where n is the time index, $F/M = 2\pi f/F_S$, M is the maximum internal value, f is the selected frequency, and F_S is the sampling frequency. Thus the frequency extrema are:

$f = (F/M)\, F_S/(2\pi)$

$f_{min} = (0x1/0x3ffff)\,(48kHz)/(2\pi)$
$= 0.029Hz$

$f_{max} = (0x1fff/0x3ffff)\,(48kHz)/(2\pi)$
$= 239Hz$

Triangle waves are generated by incrementally adding or subtracting 0x400000*F/M ($= 2^{22}*F/M$) from the maximum internal negative or positive value respectively. Its frequency extrema are then:

$f = \#\ Samples\ /\ \#\ Steps$
$= F_S\ /\ (4\ Max/Increment)$
$= F_S\ /\ (4\ 0x7fffff/(2^{22}*F/M))$

$f_{min} = 48kHz\ /\ (8/(0x1/0x3ffff))$
$= 0.023Hz$

$f_{max} = 48kHz\ /\ (8/(0x1fff/0x3ffff))$
$= 187Hz$

When chorus instructions are used, addresses are offset by the output an LFO. The range of this offset is plus and minus A/8 samples, or A/4 samples total.

Following the 4 LFO coefficient words are 124 MAC instruction words. These instructions allow the manipulation of the DRAM and the waveforms generated by the LFOs.

A good NOP instruction is 0x00030000. This instruction preserves the value in all registers, and is the NOP executed in the MAC during the first four ticks of every sample period while the LFO coefficients are loaded.

By judiciously choosing the LFO frequency and waveform with which to sweep through the DRAM, it is possible to generate pitch shifts, flanges, choruses, reverbs, and other effects. Please see application notes for descriptions and examples.

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MAC Instruction Word

<table>
<tr><th>Bit #</th><th>Description</th></tr>
<tr><td>31</td><td>S: Sign bit for multiplier coefficient.</td></tr>
<tr><td>30:23</td><td>C[7:1]: Multiplier coefficient, 2's complement.
C[7:0]: Chorus instruction. Only the 7 MSBs are used as multiplier coefficients. The LSB is used in chorus mode. If I[5] is set, C[7:0] is:
<table>
<tr><th>C</th><th>Description</th></tr>
<tr><td>7</td><td>Chorus/Xfade select:
1: Pass LFO address to address generator & select chorus coefficient.
0: Mask LFO address to address generator & select crossfade coefficient.</td></tr>
<tr><td>6</td><td>1's complement the LFO address sign bit. [1]</td></tr>
<tr><td>5</td><td>1's complement the LFO coefficient.</td></tr>
<tr><td>4</td><td>1's complement the LFO address.</td></tr>
<tr><td>3</td><td>LFO latch. 1: Latch in new LFO data; 0: Hold last LFO data. [2]</td></tr>
<tr><td>2:1</td><td>LFO select.</td></tr>
<tr><td>0</td><td>LFO sine/cosine select. 1: Cos; 0: Sin.</td></tr>
</table></td></tr>
<tr><td>22</td><td>W: Write select. [3, 4]</td></tr>
<tr><td>21:16</td><td>I[5:0]: Instruction field.
<table>
<tr><th>I</th><th>Description</th></tr>
<tr><td>5</td><td>Chorus select (When set, MAC coefficient is LFO block output, LFO address offset added to DRAM address).</td></tr>
<tr><td>4</td><td>Clock register C. [3]</td></tr>
<tr><td>3</td><td>Clock register B. [4]</td></tr>
<tr><td>2</td><td>Reserved – set to zero.</td></tr>
<tr><td>1:0</td><td>MAC product instruc-tion.
<table>
<tr><th>I[1:0]</th><th>Instruction</th></tr>
<tr><td>11</td><td>Acc = Prod + Acc [6]</td></tr>
<tr><td>10</td><td>Acc = Prod + C [3]</td></tr>
<tr><td>01</td><td>Acc = Prod + B [5]</td></tr>
<tr><td>00</td><td>Acc = Prod + 0</td></tr>
</table></td></tr>
</table></td></tr>
<tr><td>15:0</td><td>A[15:0]: Multiplicand address. [7, 8] (Currently only lower 15 bits used; reserve MSB for future expansion.)
Address 0x0000 = LeftIn/Out;
Address 0x0001 = RightIn/Out.</td></tr>
</table>

Notes:

1. This complement is only for the MSB, and sign-extension bits are not affected.
2. Upon latching new data, the LFO registers will store the lower or upper LFO pairs' sinusoid/triangle waves, and the lower or upper LFO pairs' crossfade coefficient. I.e. there are two pairs of registers; LFO 0/1's sinusoid /triangle/crossfade will be latched together, and LFO 2/3's sinusoid/triangle/crossfade will be latched together.
3. The LeftOut, RightOut, and C registers are in parallel with the accumulator, and will contain the same value as the accumulator if clocked at the end of the tick.
4. A write to DRAM stores the last tick's results into address A. Writes to LeftOut or RightOut should use the Acc = Product + Acc instruction with the multiplier coefficient set to 0 to pass all bits unaltered.
5. Register B, if clocked at the end of the tick, will store the value of the current tick's multiplicand. When a read is executed, B latches LeftIn, RightIn, or DRAM. When a write is executed, B latches the accumulator from the last tick.
6. The accumulator contains the result from the last instruction tick, and is updated at the end of the current instruction tick.
7. The internal DRAM address offset automatically decrements by 1 every word clock period.
8. Because addresses 0x0000 and 0x0001 are being used to access the left and right channels, those DRAM memory locations may not be directly written to or read from.

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Control/Status Word 0

Bit #	Description
31:30	Reserved. Set to zero.
29:16	B[13:0]: DRAM read data. [1]
15:11	Reserved. Set to zero.
10	O: MAC overflow. Self-clears after read. Read only.
9	P: Self test pass. Read only.
8	R: Ready indication. Read/write/test/clear complete.
7	M: DigOut mute in external mode. Resets to 1.
6	Z: DRAM zero. Initiates zeroing cycles until deasserted. Resets to 0. [2, 3, 4, 5, 6]
5	X: DRAM zero cancel. Prevents zeroing circuitry from running until deasserted. Overrides Z. Resets to 0. [3]
4	L: LFO reset pulse. Resets LFO internal status registers and clears overflow flag. Self clearing. Resets to 0.
3	I: Instruction RAM direct mode. Resets to 1. 1: Instructions are written/read as soon as received; 0: Instructions are written/read when the address counter rolls around to matching address. [7]
2	Reserved. Set to zero.
1	S[1]: DRAM self test pattern select. 1: Load DRAM with 2AAA/1555 checkerboard; 0: Load DRAM with 1555/2AAA checkerboard.
0	S[0]: DRAM self test initiate. Self-clears after test completion. Resets to 0. [2, 3, 6, 8, 9]

Notes:

1. The floating point format used in the DRAM is: E[2:0].S.F[9:0], where E is the exponent, S is the sign bit, and F is the fractional portion. The expansion of the floating point into fixed point is as follows:
   If E<7, S E*S !S FFFFFFFFFF (8-E)*0
   (where E*S means E number of S bits).
   If E=7, S SSSSSSS FFFFFFFFFF 00.
   This method encodes one extra bit for sign extensions less than 7 bits.
2. The DRAM zeroing circuitry and DRAM self test circuitry share gates; do not turn more than one on at a time.
3. The DRAM zeroing cycle will run to completion even if Z deasserted. Only the X bit may cancel it mid-cycle. Until the cycle ends, self test results will be inaccurate. Thus do not deassert Z and assert S[0] at the same time. Rather, assert X and S[0] at the same time.
   Note that Z does not self-clear, and will affect both internal and external mode.
4. After a DRAM zeroing cycle has completed, do not start another for one word clock period.
5. A DRAM zeroing cycle takes approximately 5.33ms to complete with a 12MHz crystal.
6. During DRAM zeroing and test cycles, reads and writes to the DRAM are ignored.
7. For dynamically changing programs, deassert I so that changing the program does not interrupt its execution. Otherwise reads and writes to the Instruction RAM will usurp the address bus to the RAM and cause address jumps in the instruction sequence. With I deasserted, reads and writes to each address may take up to one word clock period to complete. Thus during continuous writes, the start of each instruction word should be at least one word clock period apart, and during reads the serial clock should wait 1 word clock after the address before continuing.
8. The DRAM self test cycle will run to completion even if S[0] is deasserted. It may not be cancelled.
9. A DRAM self test cycle takes approximately 10.66ms to complete with a 12MHz crystal.

Control/Status Word 1

Bit #	Description
31	R: Read select. Read data from DRAM address A[15:0] and put data in B of control/status word 0. Self-clears after completion.
30	W: Write select. Write data D[13:0] to DRAM address A[15:0]. Self-clears after completion.
29:16	D[13:0]: DRAM write data.
15:0	A[15:0]: DRAM address. The MSB is unused and reserved for future expansion.

Note: Reading and writing DRAM will usurp DRAM access for one cycle, possibly disrupting proper code execution.

Other notes:

1. When in internal mode, program changes will start a DRAM zero cycle.
2. Resets always start a DRAM zero cycle.
3. To meet refresh requirements below 70 °C, access each address (modulo 1024) every 1.34 ms. If program code doesn't do this, then (at 48 kHz) read 16 locations each cycle spaced 1024/16 = 64 addresses apart, to meet refresh requirements. (For instance, addresses 0x0002, 0x0042, ..., 0x03C2.)
4. ROMs may not be read due to the serial interface becoming the program select interface when in internal mode.
5. Use of Reset is mandatory to obtain proper operation of the AL3201.

The 4 word formats: LFO, MAC, CS0, CS1
LFO: PSXXFFFF FFFFFFFF FAAAAAAA AAAAAAAA
MAC: SCCCCCCC CWIIIIII AAAAAAAA AAAAAAAA
CS0: --BBBBBB BBBBBBBB -----OPR MZXLI-SS
CS1: RWDDDDDD DDDDDDDD AAAAAAAA AAAAAAAA

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Serial Interface Format

The basic format for the micro serial interface is:

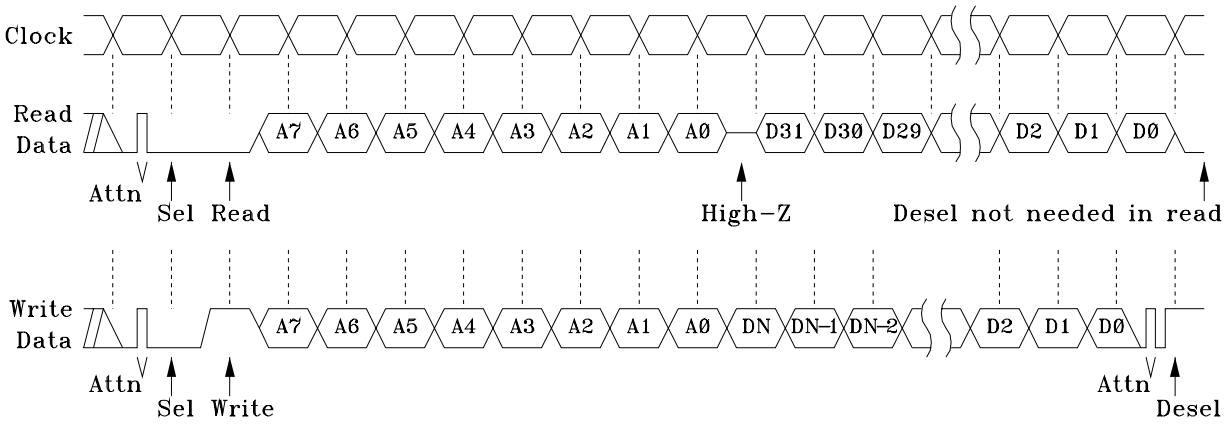
Attn Sel R/W A7 A6 A5 A4 A3 A2 A1 A0 DN DN-1 DN-2 ... D2 D1 D0 Attn Desel

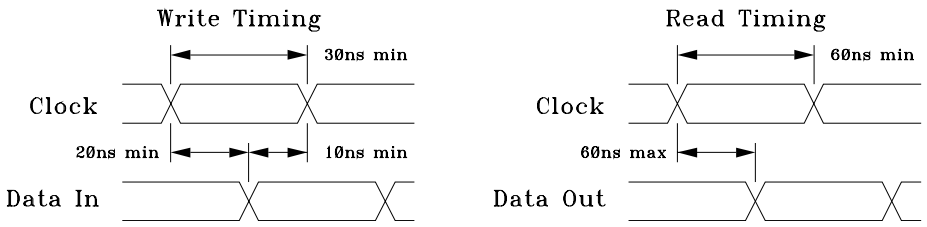
⇓ ⇓ Write mode only

Attn:	A 0-1-0 is used to signal attention/start.		
Sel/Desel:	0:Select; 1:Deselect.	A7 - A0:	Address
R/W:	0:Read; 1:Write	DN - D0:	Data

Notes:

1. There is a short period of High-Z during a read between A0 and the first data bit shifted out. This period must be at least 5 system clocks long, 1 word clock long if not in direct mode (CS0[3]).
2. As long as data is being sent during a write, the address will be automatically incremented. Therefore only a start address need be sent.
3. The phase of the clock is unimportant.





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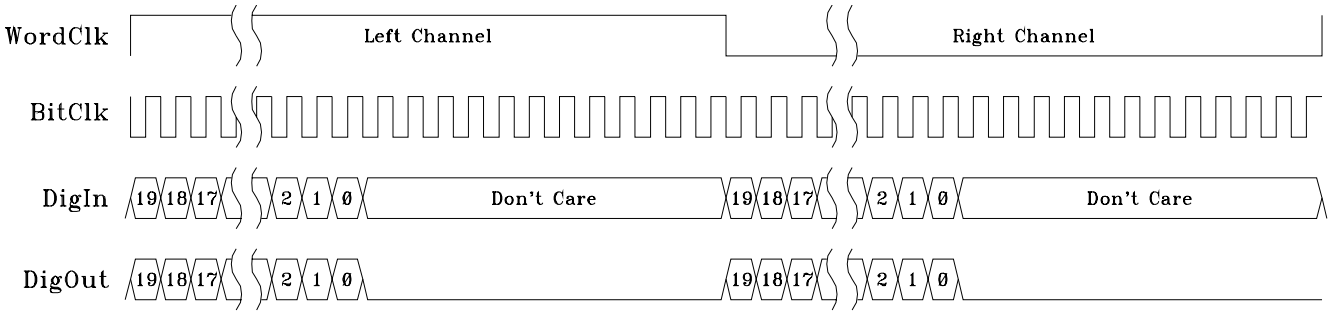
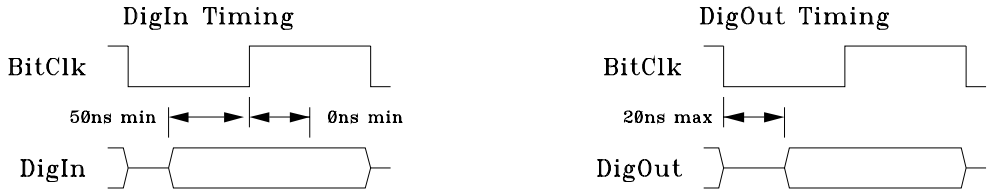
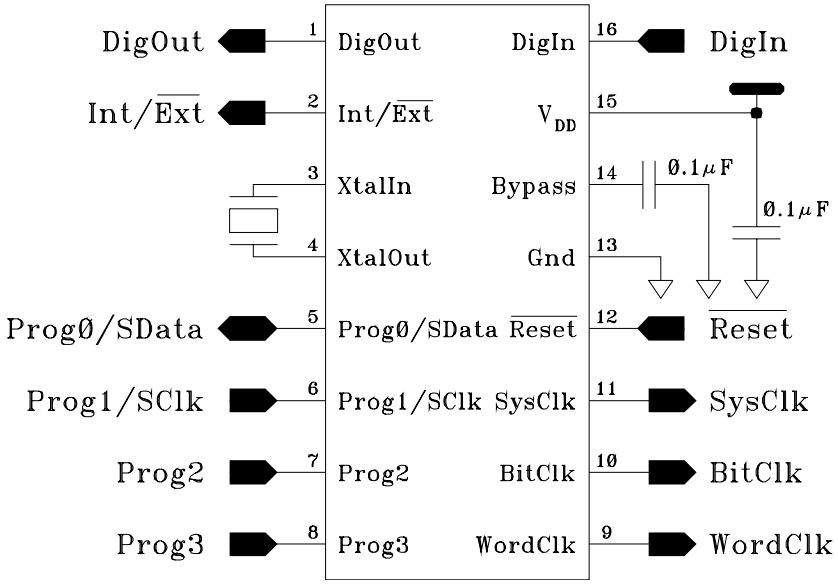
DigIn/DigOut Interface Format





Suggested Connections



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