QPRO Series Configuration PROMs (XQ) including Radiation-Hardened Series (XQR)

DS062 (v2.0) June 1, 2000

Advance Product Specification

Features

- Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams of Xilinx FPGA devices
- Simple interface to the FPGA; requires only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions
- Supports XQR4000XL/Virtex fast configuration mode (15.0 MHz) (XQR1701L and XQR1704L)
- Supports XQ4000EX/XL fast configuration mode (15.0 MHz) (XQ1701L and XQ1704L)
- Fabricated on Epitaxial Silicon to improve latch performance (parts are immune to Single Event Latch-up) (XQR1701L and XQR1704L)
- QML certified
- Single Event Bit Upset immune (XQR1701L and XQR1704L)
- Total Dose tolerance in excess of 50K rads(Si) (XQR1701L and XQR1704L)
- All lots subjected to TID Lot Qualification in accordance with method 1019 (dose rate ~9.0 rads(Si)/sec) (XQR1701L and XQR1704L)
- Available in 44-pin ceramic LCC (M grade) package
- Available in 44-pin plastic chip carrier package (XQ1704L only)
- Available in 20-pin SOIC package (XQ1701L only)
- Programming support by leading programmer manufacturers.
- Design support using the Xilinx Alliance and Foundation series software packages.

Description

The QPRO™ series XQ1701L and XQ1704L are Xilinx 3.3V high-density configuration PROMs. The XQR1701L and XQR1704L are radiation hardened. These devices are manufactured on Xilinx QML certified manufacturing lines utilizing epitaxial substrates and TID lot qualification (per method 1019).

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. A short access time after the rising clock edge, data appears on the PROM DATA output pin that is connected to the FPGA D_{IN} pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the PROM. When the FPGA is in Slave Serial mode, the PROM and the FPGA must both be clocked by an incoming signal. Figure 1 shows a simplied block diagram.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all PROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, either the Xilinx Alliance or Foundation series development system compiles the FPGA design file into a standard Hex format, which is then transferred to most commercial PROM programmers.

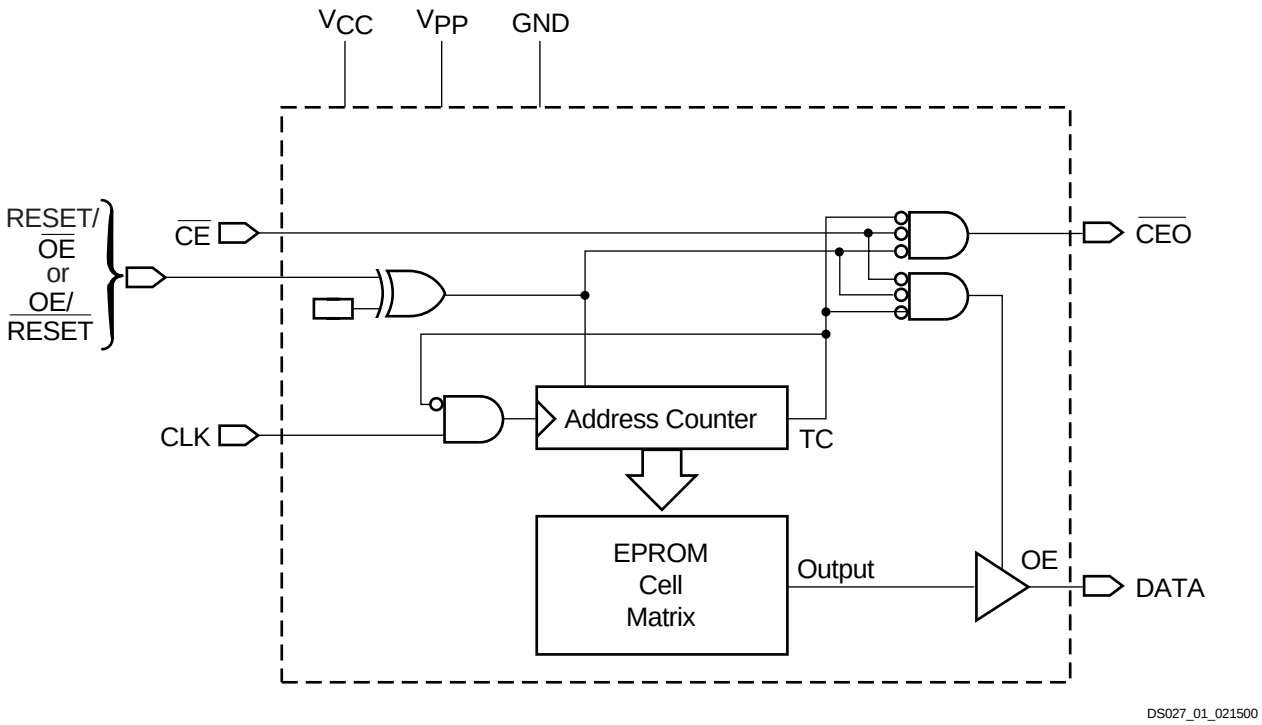


Figure 1: **Simplified Block Diagram (does not show programming circuit)**

Pin Description

DATA

Data output is in a high-impedance state when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

CLK

Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active.

RESET/$\overline{OE}$

When High, this input holds the address counter reset and puts the DATA output in a high-impedance state. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at "0", and puts the DATA output in a high-impedance state. The polarity of this input is programmable. The default is active High RESET, but the preferred option is active Low $\overline{RESET}$, because it can be driven by the FPGAs $\overline{INIT}$ pin.

The polarity of this pin is controlled in the programmer interface. This input pin is easily inverted using the Xilinx HW-130 Programmer. Third-party programmers have different methods to invert this pin.

$\overline{CE}$

When High, this pin disables the internal address counter, puts the DATA output in a high-impedance state, and forces the device into low-I_{CC} standby mode.

$\overline{CEO}$

Chip Enable output, to be connected to the $\overline{CE}$ input of the next PROM in the daisy chain. This output is Low when the $\overline{CE}$ and $\overline{OE}$ inputs are both active AND the internal address counter has been incremented beyond its Terminal Count (TC) value. In other words: when the PROM has been read, $\overline{CEO}$ will follow $\overline{CE}$ as long as $\overline{OE}$ is active. When $\overline{OE}$ goes inactive, $\overline{CEO}$ stays High until the PROM is reset. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

V_{PP}

Programming voltage. No overshoot above the specified max voltage is permitted on this pin. For normal read operation, this pin must be connected to V_{CC}. Failure to do so may lead to unpredictable, temperature-dependent operation and severe problems in circuit debugging. Do not leave V_{PP} floating!

V_{CC} and GND

Positive supply and ground pins.

PROM Pinouts

Pin Name	44-Pin CLCC
DATA	2
CLK	5
RESET/$\overline{OE}$ ($OE/\overline{RESET}$)	19
$\overline{CE}$	21
GND	3, 24
$\overline{CEO}$	27
V_{PP}	41
V_{CC}	44

Capacity

Devices	Configuration Bits
XQR1704L	4,194,304
XQR1701L	1,048,576
XQ1704L	4,194,304
XQ1701L	1,048,576

Xilinx FPGAs and Compatible PROMs.

Device	Configuration Bits	PROM
XQR4013XL	393,632	XQ1701L
XQR4036XL	832,528	XQ1701L
XQR4062XL	1,433,864	XQ1704L
XQR4013XL	393,632	XQR1701L
XQR4036XL	832,528	XQR1701L
XQR4062XL	1,433,864	XQR1704L
XQVR300	1,751,840	XQR1704L
XQVR600	3,608,000	XQR1704L
XQVR1000	6,127,776	XQR1704L x 2

Controlling PROMs

Connecting the FPGA device with the PROM.

- The DATA output(s) of the of the PROM(s) drives the D_{IN} input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s).
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The $\overline{RESET}$/OE input of all PROMs is best driven by the $\overline{INIT}$ output of the lead FPGA device. This connection assures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch. Other methods—such as driving $\overline{RESET}$/OE from $\overline{LDC}$ or system reset—assume the PROM internal power-on-reset is always in step with the FPGAs internal power-on-reset. This may not be a safe assumption.
- The PROM $\overline{CE}$ input can be driven from either the $\overline{LDC}$ or DONE pins. Using $\overline{LDC}$ avoids potential contention on the D_{IN} pin.
- The $\overline{CE}$ input of the lead (or only) PROM is driven by the DONE output of the lead FPGA device, provided that DONE is not permanently grounded. Otherwise, $\overline{LDC}$ can be used to drive $\overline{CE}$, but must then be unconditionally High during user operation. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

FPGA Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Serial mode, the FPGA automatically loads the configuration program from an external memory. The Xilinx PROMs have been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, an FPGA enters the Master Serial mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an FPGA. Data from the PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function D_{IN} pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. The Xilinx FPGA families take care of this automatically with an on-chip default pull-up resistor.

Programming the FPGA With Counters Unchanged Upon Completion

When multiple FPGA-configurations for a single FPGA are stored in a PROM, the $\overline{OE}$ pin should be tied Low. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the $\overline{OE}$ pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the DONE line is pulled Low and configuration begins at the last value of the address counters.

This method fails if a user applies $\overline{RESET}$ during the FPGA configuration process. The FPGA aborts the configuration and then restarts a new configuration, as intended, but the PROM does not reset its address counter, since it never saw a High level on its $\overline{OE}$ input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the FPGA is the master, it issues the necessary number of CCLK pulses, up to 16 million (2^{24}) and DONE goes High. However, the FPGA configuration will be completely wrong, with potential contentions inside the FPGA and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

Cascading Configuration PROMs

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded PROMs provide additional memory. After the last bit from the first PROM is read, the next clock signal to the PROM asserts its $\overline{CEO}$ output Low and disables its DATA line. The second PROM recognizes the Low level on its $\overline{CE}$ input and enables its DATA output. See Figure 2.

After configuration is complete, the address counters of all cascaded PROMs are reset if the FPGA $\overline{RESET}$ pin goes Low, assuming the PROM reset polarity option has been inverted.

To reprogram the FPGA with another program, the DONE line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of D_{IN}.

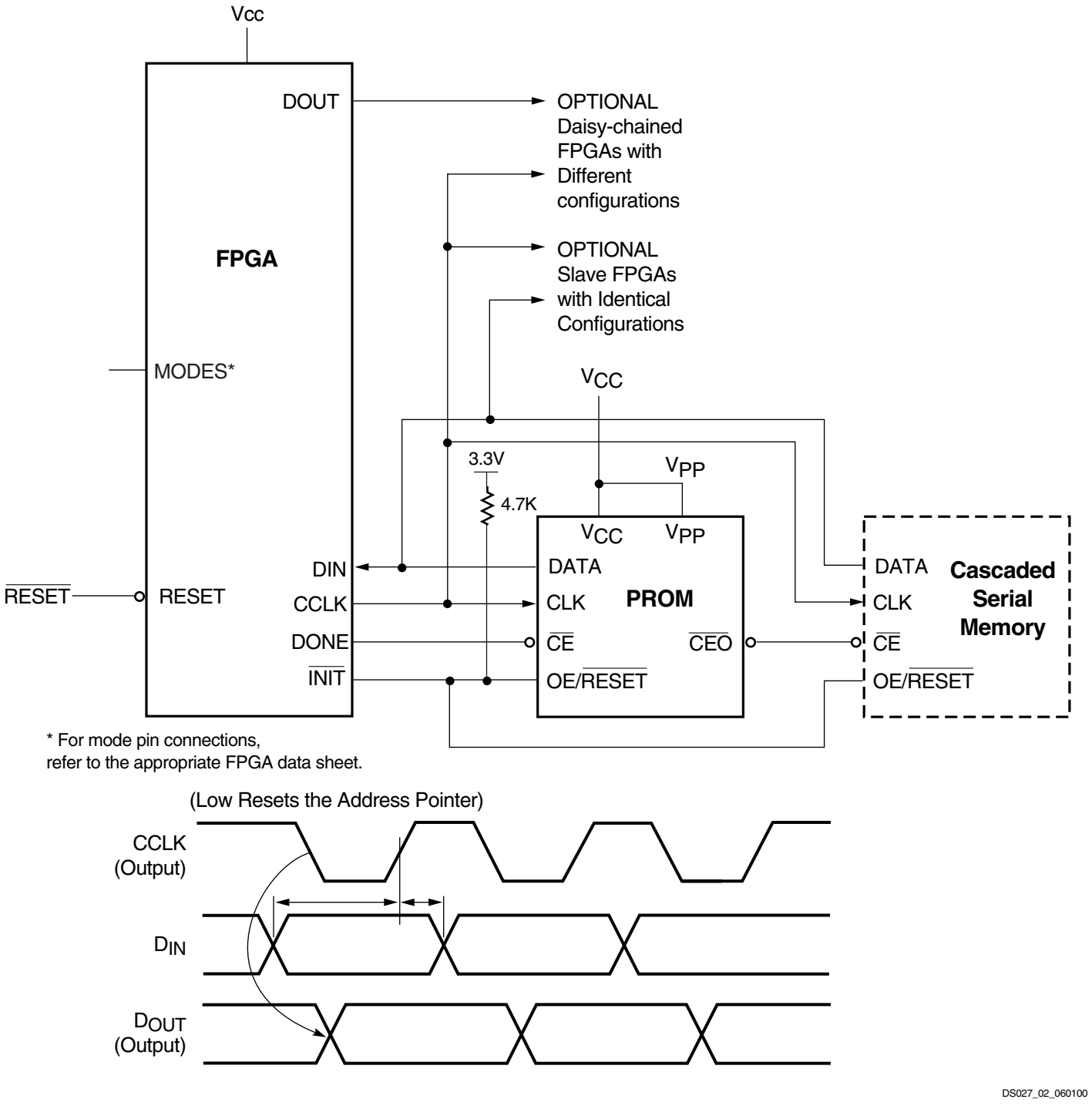


Figure 2: **Master Serial Mode.** The one-time-programmable PROM supports automatic loading of configuration programs. Multiple devices can be cascaded to support additional FPGAs. An early DONE inhibits the PROM data output one CCLK cycle before the FPGA I/Os become active.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high-impedance state regardless of the state of the $\overline{OE}$ input.

Programming

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.

Table 1: **Truth Table for Control Inputs**

Control Inputs		Internal Address	Outputs		
RESET	**$\overline{CE}$**		**DATA**	**$\overline{CEO}$**	**I_{CC}**
Inactive	Low	If address $\leq$ TC(1): increment If address > TC(1): don't change	Active High-Z	High Low	Active Reduced
Active	Low	Held reset	High-Z	High	Active
Inactive	High	Not changing	High-Z	High	Standby
Active	High	Held reset	High-Z	High	Standby

Notes:
1. The XC1700 RESET input has programmable polarity
1. TC = Terminal Count = highest address value. TC + 1 = address 0.

Radiation Characteristics (XQR1701L and XQR1704L only)

Symbol	Description	Min	Max	Units
TID	Total ionizing dose, Method 1019	50K		rads(Si)
SEL	Single event latch-up. Heavy ion saturation cross section, LET_1 > 120 MeV cm^2/mg		0	(cm^2/Device)
SEU	Single event bit upset. Heavy ion saturation cross section LET > 120 MeV cm^2/mg		0	(cm^2/Bit)
$SEFI_2$	Single event functional interupt, Heavy ion saturation cross section, 10% saturated intercept at LET = 6.0 MeV cm^2/mg		$1.2e^{-5}$	(cm^2/Device)

Notes:
1. Single Event Effects testing was performed with heavy ion to a maximum LET of 120 MeV-cm^2/mg.
2. For more information on Single Event Effects and mitigation methods refer to Xilinx Application Note XAPP185 "Space Application Design techniques for the XQR1700L QPRO Series Radiation Hardened Serial PROMs."

Absolute Maximum Ratings

Symbol	Description	Conditions	Units
V_{CC}	Supply voltage relative to GND	–0.5 to +4.0	V
V_{PP}	Supply voltage relative to GND	–0.5 to +12.5	V
V_{IN}	Input voltage relative to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to High-Z output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in.)	+260	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}(1)	Supply voltage relative to GND ceramic package (T_C = –55°C to +125°C)	Military	3.0	3.6	V

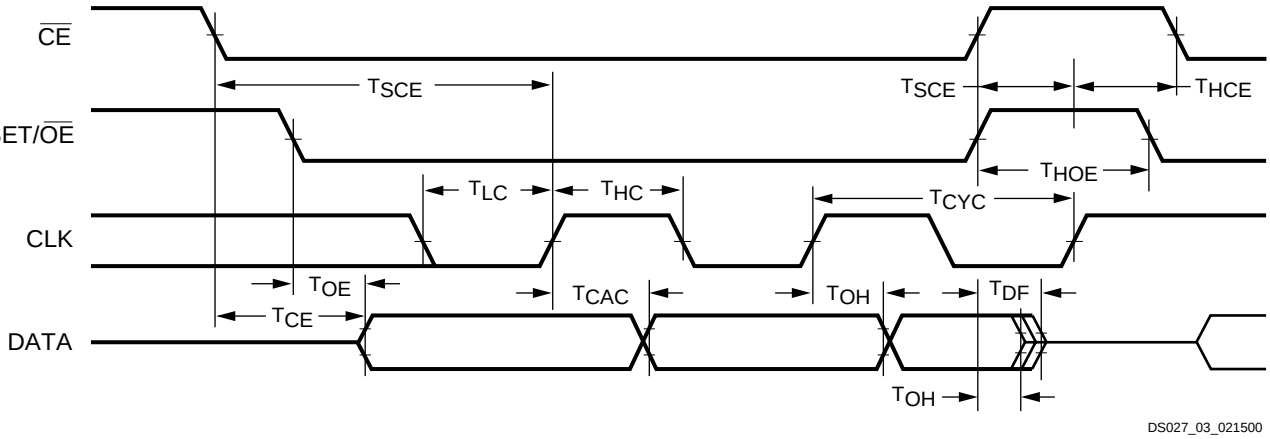
Notes:
1. During normal read operation V_{PP} MUST be connect to V_{CC}.

DC Characteristics Over Operating Condition

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = –3 mA)		2.4	-	V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)		-	0.4	V
I_{CCA}	Supply current, active mode (at maximum frequency)		-	10	mA
I_{CCS}	Supply current, standby mode (XQ1701L, XQ1704L)		-	100	µA
I_{CCS}(1)	Supply current, standby mode (XQR1701L and XQR 1704L)	Pre-rad (TID)	-	300	µA
		Post-rad (TID)	-	3	mA
I_L	Input or output leakage current		–10	10	µA
C_{IN}	Input capacitance (V_{IN} = GND, f = 1.0 MHz)		-	10	pF
C_{OUT}	Output capacitance (V_{IN} = GND, f = 1.0 MHz)		-	10	pF

Notes:
1. I_{CCS}, Standby Current is measured at +125°C for pre-radiation specifications and at room temperature for post-radiation specifications.

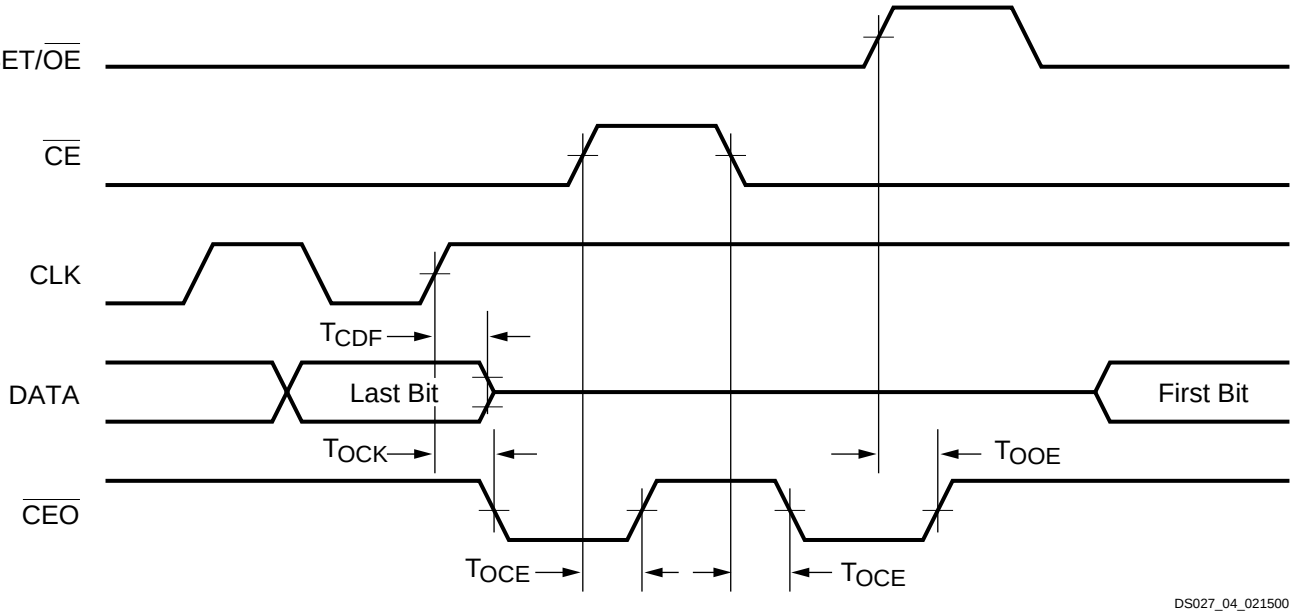
AC Characteristics Over Operating Condition



Symbol	Description	XQR1701L		XQ1701L, XQR1704L		Units
		Min	Max	Min	Max	
T_{OE}	$\overline{OE}$ to data delay	-	25	-	30	ns
T_{CE}	$\overline{CE}$ to data delay	-	45	-	45	ns
T_{CAC}	CLK to data delay	-	45	-	45	ns
T_{DF}	$\overline{CE}$ or $\overline{OE}$ to data float delay(2,3)	-	50	-	50	ns
T_{OH}	Data hold from $\overline{CE}$, $\overline{OE}$, or CLK(3)	0	-	0	-	ns
T_{CYC}	Clock periods	67	-	67	-	ns
T_{LC}	CLK Low time(3)	20	-	25	-	ns
T_{HC}	CLK High time(3)	20	-	25	-	ns
T_{SCE}	$\overline{CE}$ setup time to CLK (to guarantee proper counting)	20	-	25	-	ns
T_{HCE}	$\overline{CE}$ hold time to CLK (to guarantee proper counting)	0	-	0	-	ns
T_{HOE}	$\overline{OE}$ hold time (guarantees counters are reset)	20	-	25	-	ns

Notes:
1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.

AC Characteristics Over Operating Condition When Cascading



Symbol	Description	Min	Max	Units
T_{CDF}	CLK to data float delay(2,3)	-	50	ns
T_{OCK}	CLK to $\overline{CEO}$ delay(3)	-	30	ns
T_{OCE}	$\overline{CE}$ to $\overline{CEO}$ delay(3)	-	35	ns
T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ delay(3)	-	30	ns

Notes:
1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.

Ordering Information

XQR1701L CC44 M

Device Number

XQ1704L
XQ1701L
XQR1704L
XQR1701L

Package Type

CC44 = 44-pin Ceramic Chip Carrier
SO20 = 20-pin Plastic Small Outline Package
PC44 = 44-pin Plastic Chip Carrier

Operating Range/Processing

B = Military(T_C = –55° to +125°C) QML certified to MIL-PRF-38535
M = Military (T_C = –55° to +125°C) QML certified to MIL-PRF-38535
N = Military Plastic (T_J = –55° to +125°C)

Valid Ordering Combinations

XQR1704LCC44M	XQR1701LCC44M	XQ1701LCC44M	XQ1704LCC44M
		XQ1701LCC44B	XQ1704LCC44B
		XQ1701LSO20N	XQ1704LPC44N

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/20/00	1.0	Initial Release
06/01/00	2.0	Combined XQR1700L Rad-Hard and XQ1701L devices, added XQ1704L and updated format.