LOGICAL SOLUTIONS TECHNOLOGY INCORPORATED

Testability Chip Set Description and Specifications

Description

Logical Solutions Technology, Inc.'s (LSTI) Testability Chip Set consists of two semiconductor devices (T-Circuits), that can be used to create a complete testability system. Visibility and control circuits help you implement the exact amount of testability required for new PCBA designs, using either through-hole technology or Surface Mount Technology (SMT).

Mixing and matching as required, T-Circuits are designed into your product and included on each printed circuit board to implement a standard testability bus.

When implemented in your designs, the Testability Chip Set augments the interface between your circuit and automatic test equipment (ATE) or built in self test circuitry via the testability bus to render the assembly testable at board and system level test, as well as field service test.

The LSTI "Testability System" can drastically reduce test programming, test fixturing, test equipment, testing and troubleshooting costs, especially for surface mount technology printed circuit board designs.

System Features

The LSTI Testability Chip Set is a powerful tool for rendering assemblies testable. System features include:

- **Control and observation capability with no effect on normal circuit logic functions and with minimal impact on circuit design.**
- **Control and observation functions on both combinatorial and sequential functional logic circuits.**
- **Compatibility with: SSI through VLSI, Synchronous or Asynchronous Circuits, and Scan Techniques.**
- **Support of a standard Testability Bus that can be used at the board or final assembly level in both manufacturing test and field service test.**
- **Configurations for commercial and military applications.**
- **Capability to observe nodal activity by latching data in parallel and outputting it serially at lower speeds, or to monitor data in real time.**
- **Capability to control nodal activity by applying a pattern to all controlled nodes in parallel, or by selecting individual nodes and applying data in real time.**

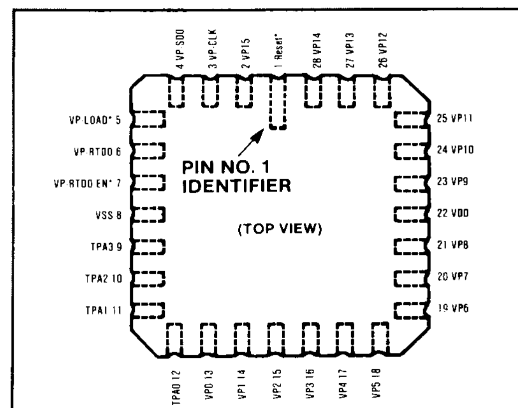

Figure 1: 16 Point Visibility Circuit LT54/74CV16CL

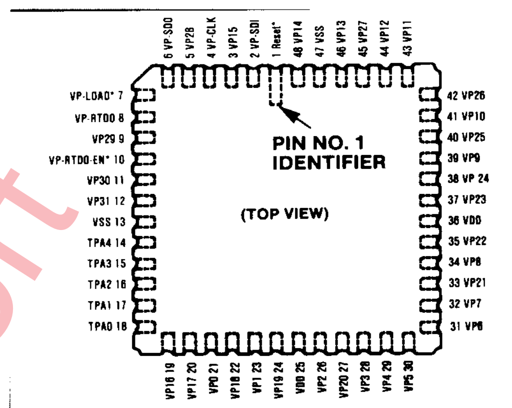

Figure 2: 16 Point Control Circuit LT54/74CC16CL

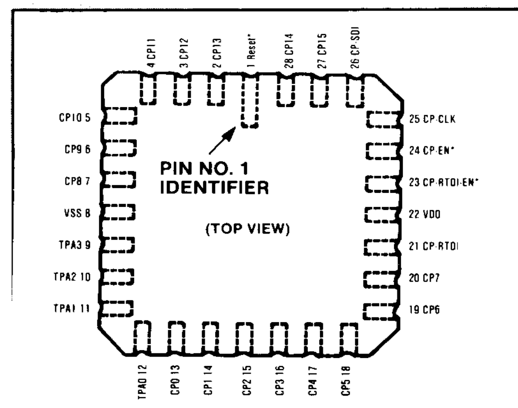

Figure 3: 32 Point Visibility Circuit LT54/74CV32CL

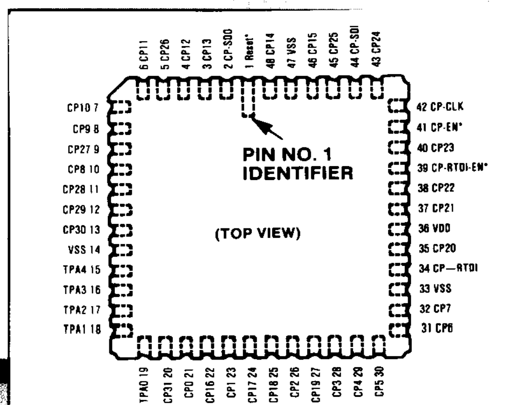

Figure 4: 32 Point Control Circuit LT54/74CC32CL

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Individual Device Features

LSTI's control and visibility devices are fabricated with a high performance complementary metal oxide semiconductor (CMOS) process. Device features include:

- **TTL compatible 2-Micron CMOS technology**
- **Very low quiescent power dissipation**
- **High noise immunity**
- **Full input protection on both power and ground sources**
- **Full buffering on all outputs**
- **Input pull-up resistors on all Testability Bus input pins so that T-Circuits have no effect on circuit operation or performance when not in use**

LSTI T-Circuits are available for both commercial ("74" series) and military ("54" series) applications. Output current sink and drive capability is guaranteed over -40° to +85° for "74" series devices and -55° to +125° for "54" series devices.

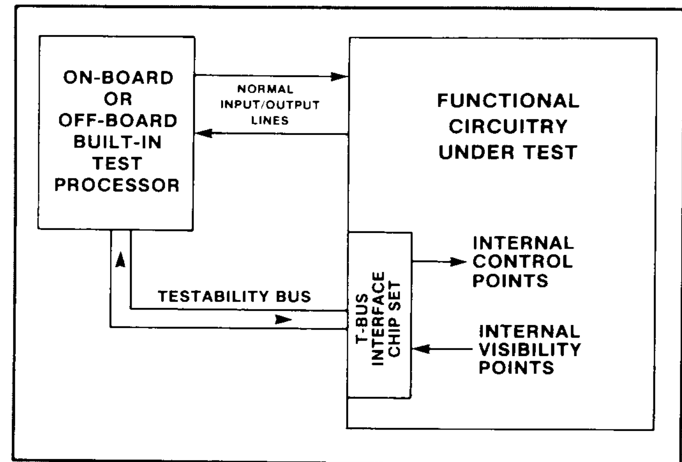

Figure 5

Built-In Testability

The LSTI Testability Chip Set is a specific circuit architecture that builds in enhanced testability characteristics for the functional circuitry when applied at the printed circuit board assembly or electronic system level.

The chip set allows control of any or all of the internal test points added to the circuit elements in the functional circuitry, and concurrent observation of existing or resulting logic states at the critical internal nodes of that functional circuitry.

The LSTI Testability Chip Set allows serial data (i.e., signature analysis) based test equipment to evaluate parallel logic states within the functional combinatorial and sequential circuitry. It also allows parallel data (i.e., stored vector) based test equipment and techniques to be used in place of, or in conjunction with, the serial data only input/output techniques required by other testability enhancement architectures and circuits.

The LSTI Testability Chip Set transparently provides input data to and obtains output data from the internal nodes of the functional circuitry to provide enhanced controllability and visibility, via the testability bus interface, which augments the normal input/output connections of the functional circuitry under test.

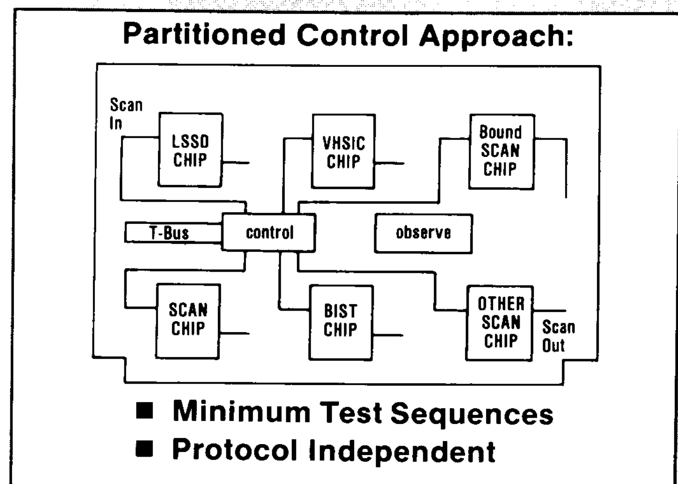

Figure 6

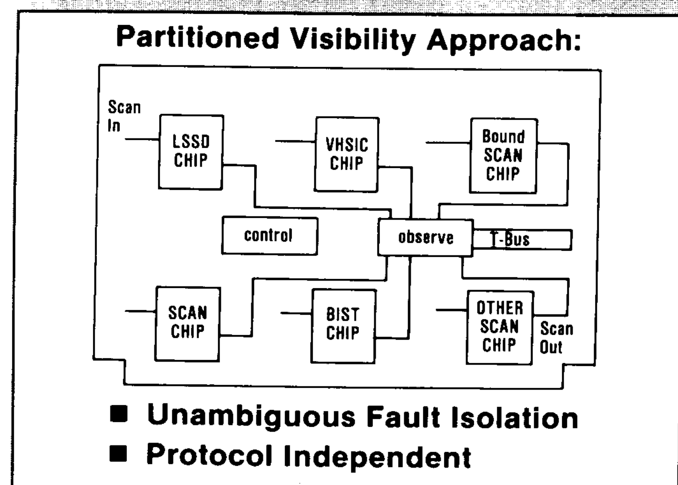

Figure 7

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Visibility Circuit Pin Description

VP 0-n — The VP 0-n (Visibility Point) signals are the actual connections to the functional circuit to be tested. As many visibility points can be added as required by the design. Visibility T-Circuits are available in 16, 32 and 64 point versions.

The visibility points can be monitored serially via the VP LOAD*, VP SDO, and VP CLK signals, or they can be addressed and monitored individually using TPA 0-n, VP RTDO, and VP RTD EN*.

RESET* — The RESET* signal is active low. It sets all visibility T-Circuit internal memory elements into a known state.

The RESET* signal must be in the logic 1 state for the visibility circuits to operate in any mode other than the initialize mode.

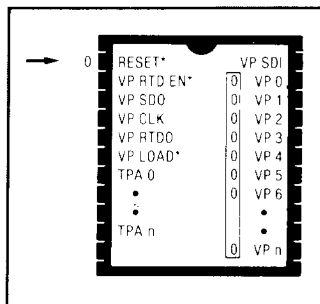

Figure 14

VP SDO — The VP SDO (Visibility Point Serial Data Output) signal is used in conjunction with the VP CLK signal to output visibility point logic states which have been previously loaded. The first signal appearing on VP SDO is the state of the highest numbered visibility point register. Consecutively lower numbered visibility point register states appear at VP SDO as CP CLK is successively activated.

VP SDO is not a tri-state line.

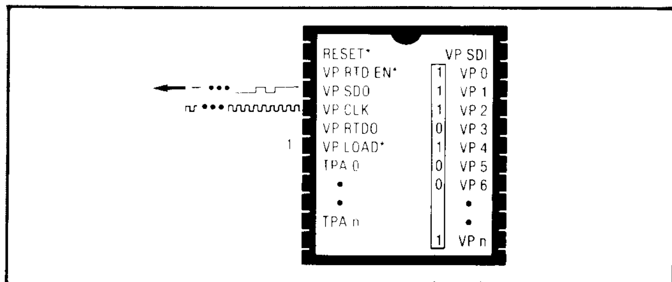

Figure 15

VP LOAD* — The VP LOAD* (Visibility Point Load) signal is used to latch data from all visibility points. The latched data can then be output serially via VP SDO and VP CLK. While VP LOAD* is at a logic 0, the T-Circuits internal registers follow their respective visibility point inputs. On the rising edge of VP LOAD*, the current visibility point input states are latched into the internal registers. It is recommended that VP LOAD* be pulsed to latch data and that data on the visibility point inputs remain stable during the time that VP LOAD* is at a logic 0.

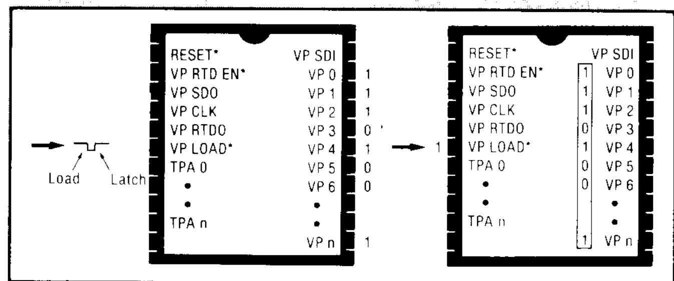

Figure 16

VP CLK — The VP CLK (Visibility Point Clock) signal is used to clock data serially through the visibility T-Circuit.

VP CLK is used in conjunction with VP SDI to serially output a loaded pattern of 1's and 0's out of the visibility T-Circuit.

VP SDI — The VP SDI (Visibility Point Serial Data Input) signal is an expansion input.

The VP SDI of one visibility T-Circuit is connected to the VP SDO of another visibility T-Circuit when more than one visibility chip is needed. The first state applied to VP SDI will go to the lowest numbered visibility point register. Consecutively higher visibility point registers will change state upon successive activations of VP CLK. The VP SDI signal also aids in testing visibility circuits. Data can be sent into VP SDI and observed at VP SDO to verify visibility circuit internal registers. See Figure 17.

VP RTDO — The VP RTDO (Visibility Point Real Time Data Output) signal is used in conjunction with the Test Point Address signals to monitor any series of 1's and 0's at a selected visibility point.

VP RTDO is tri-stated when VP RTD EN* is at a logic 1.

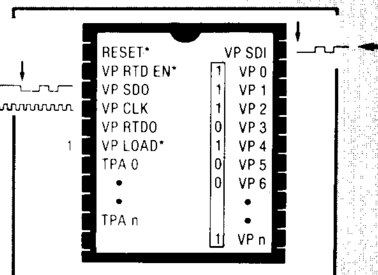

Figure 17

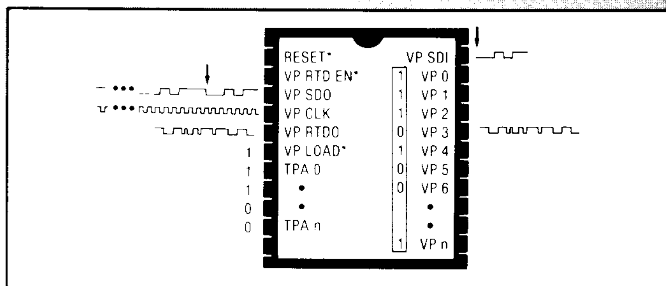

Figure 18

VP RTD EN* — The VP RTD EN* (Visibility Point Real Time Data Enable) signal allows the VP RTDO to be tri-stated.

When the VP RTD EN* signal is at a logic 1, the VP RTDO signal does not output any data.

VP RTD EN* allows multiple visibility T-Circuits to have their VP RTDO signals connected to a common line.

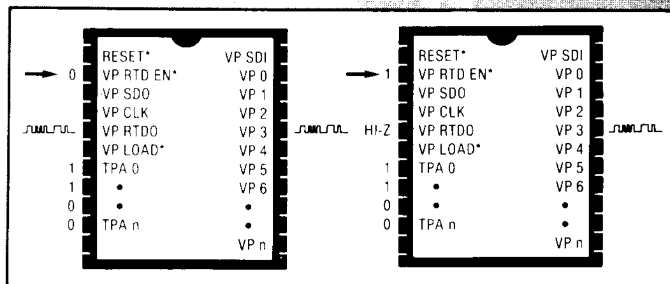

Figure 19

TPA 0-n — The TPA 0-n (Test Point Address) signals are high active binary address lines used to select individual points on visibility T-Circuits (4 address lines are required for 16 visibility points, 5 for 32 and 6 for 64). See Figure 13.

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Detailed Characteristics and Specifications

Input Configuration

All inputs are dual diode protected against transients and represent a high impedance and a low capacitance load to functional circuit nodes in the circuit under test.

Testability bus inputs are augmented with an active pull-up resistor so that no connections to the testability bus are required to maintain the quiescent condition of the control and visibility circuits. In the quiescent state, control point outputs are in the high impedance mode.

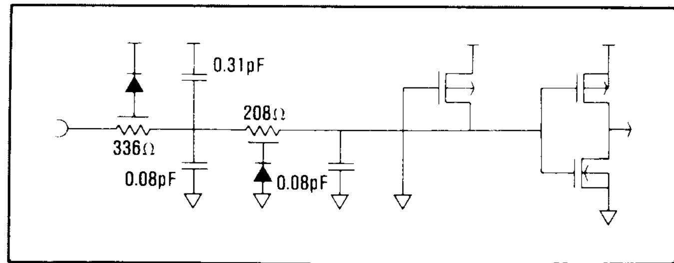

Figure 20

Output Configuration

The outputs of the LSTI control circuits are symmetrical TTL compatible CMOS outputs. The circuits can sometimes be used to "pull down" a normally high control point in the functional circuit under test, as this action normally has no detrimental effect on either the LSTI control circuit or the functional circuitry being pulled down (for most TTL compatible logic families). The circuits do not have the capability of "pulling up" a normally low control point input in the functional circuit under test. Exceeding the absolute maximum current ratings may cause damage to T-Circuit output drivers.

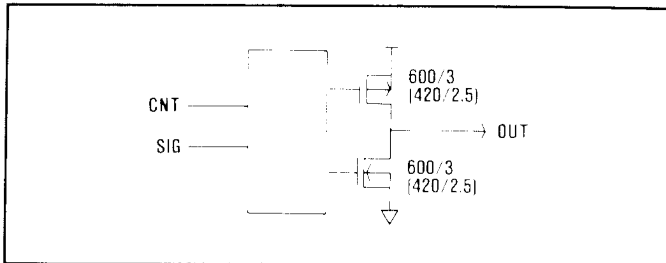

Figure 21

Operating Characteristics

LSTI T-Circuits consume very low power and have low input and output leakage currents. They may be implemented into designs with no detrimental effects on the functional unit under test. Due to the use of 2-micron CMOS device technology, T-Circuits can operate at high rates of operating speed.

AC Characteristics

Control T-Circuit

	MIN.	TYP.	MAX.	UNITS
CP CLK Period	12	25	44	nSEC
CP Output Skew	0	<1	2	nSEC
RESET Pulse Width	10	25	40	nSEC
Propagation Delay (CP RTDI - CP n)	18	40	64	nSEC
CP Address Change Time	20	42	66	nSEC

Visibility T-Circuit

	MIN.	TYP.	MAX.	UNITS
VP CLK Period	10	25	44	nSEC
VP Load Pulse/VP Data Valid	10	25	40	nSEC
RESET Pulse Width	10	25	42	nSEC
Propagation Delay (VP RTD - VP n)	13	40	64	nSEC
VP Address Change Time	16	44	72	nSEC

DC Characteristics
Control & Visibility T-Circuits

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Static Current	IQ	Vin = Vdd or Vss Ioh = Iol = 0	1	5	10	uA
Input Leakage & Output Leakage	IL Ioz	Vdd=5.5V Vin = Vdd Vil = Vss	-5	±1	5	uA
Input "H"	Vin3	Vdd = 5.5V	2.4			V
Input "L"	Vin3	Vdd = 4.5V			0.5	V
Pull-up Resistor	R PL 1	Vdd = 5.0V	55		1000	KΩ
Output "H"	Voh 1	Vdd = 4.5V Ioh = -2mA	Vdd -0.5			V
Output "L"	Vol 1	Vdd = 4.5V Ioh = 6mA			Vss +0.5	V

All devices contain diodes to protect inputs against damage due to high static voltages or electrical fields, however, it is advised that precautions be taken not to exceed the maximum recommended input voltage.

Recommended Operating Conditions
Control & Visibility T-Circuits

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Power Supply Voltage	Vdd	4.5	5.0	5.5	V
Input Voltage	Vin	Vss		Vdd	V
Storage Temperature	Topr	-55		+125	°C

Vs = 0

Device Configuration Options

Configuration options of the LSTI Testability Chip Set are as follows:

1. Operating temperature ranges industrial (-40 to 85° C) and military (-55 to 125° C).
2. Logic level compatibility: TTL.
3. Number of active lines in either the control or visibility chip: 16, 32 or 64.
4. Package material: plastic and ceramic.
5. Package type: Dual in line, small outline DIP, leaded and leadless chip carrier, mini-flat pack, and pin grid array.

These options are identified in the LSTI Testability Chip Set Part Numbering System.

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Control Circuit Pin Description

CP 0-n — The CP 0-n (Control Point) signals are the actual connections to the functional circuit to be tested. As many control points can be added as required by the design. Control T-Circuits are available in 16, 32 and 64 point versions.

The control points can be controlled serially via the CP SDI and CP CLK signal, or they can be addressed and controlled individually using TPA 0-n, CP RTDI, and CP RTD EN*.

RESET* — The RESET* signal is active low. It sets all control T-Circuit internal memory elements into a known state.

When activated, all control point circuit internal registers go to a logic 0. If the CP EN* signal is at logic 0, all control output signals go to a logic 0 when RESET* is activated.

Figure 8

The RESET* signal must be in the logic 1 state for the control circuits to operate in any mode other than the initialize mode.

CP EN* — The CP EN* (Control Point Enable) signal is used to tri-state the control point output of the control T-Circuit.

When CP EN* is at a logic 1, the control points are tri-stated. Prior to applying CP EN*, individual control points can be addressed and set to a logic 1 or 0. When the CP EN* signal is then set to a logic 0, the preset pattern is applied to the control points.

Figure 9

CP SDI — The CP SDI (Control Point Serial Data Input) signal is used in conjunction with the CP CLK signal to load data serially into the control T-Circuit.

When CP EN* is at a logic 0, CP CLK causes the data on CP SDI to be rippled through the control point outputs. Data on CP SDI appears first on the lowest numbered control point (e.g. CP 0) and then on consecutively higher numbered control points as the CP CLK signal is successively activated.

When CP EN* is at a logic 1, CP CLK causes the data on CP SDI to be clocked through the T-Circuit internal control point registers. When CP EN* is returned to a logic 0, the content of the output registers is applied at the control point outputs.

CP CLK — The CP CLK (Control Point Clock) signal is used to clock data serially through the control T-Circuit.

CP CLK is used in conjunction with CP SDI to serially load a pattern of 1's and 0's into the control T-Circuit. See Figure 10.

Figure 10

CP SDO — The CP SDO (Control Point Serial Data Output) signal is an expansion output. The CP SDO of one control T-Circuit is connected to the CP SDI of another control T-Circuit when more than one control circuit is needed.

The CP SDO signal also aids in testing control T-Circuits. Control points can be set serially using CP SDI and CP CLK or addressed and preset with real time data. CP CLK can then be used to clock that data out CP SDO for verification. The first signal appearing on CP SDO is the highest numbered control point state. Consequently lower control point register states are output on CP SDO for successive activations of CP CLK.

Figure 11

CP RTDI — The CP RTDI (Control Point Real Time Data Input) signal is used in conjunction with the Test Point Address signals to apply any series of 1's and 0's to an individually addressed control point.

CP RTD EN* — The CP RTD EN* (Control Point Real Time Data Enable) signal is used to enable data from the CP RTDI signal to be applied at the addressed control point.

When CP RTD EN* is at a logic 0, the addressed control point follows CP RTDI.

Figure 12

When CP RTD EN* is at a logic 1, the CP RTDI signal has no effect on the addressed control point.

TPA 0-n — The TPA 0-n (Test Point Address) signals are high active binary address lines used to select individual points on control T-Circuits (4 address lines are required for 16 control points, 5 for 32 and 6 for 64).

TA4	TA3	TA2	TA1	TA0	VP/CP
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
•	•	•	•	•	•
•	•	•	•	•	•
1	1	1	1	1	31

Figure 13

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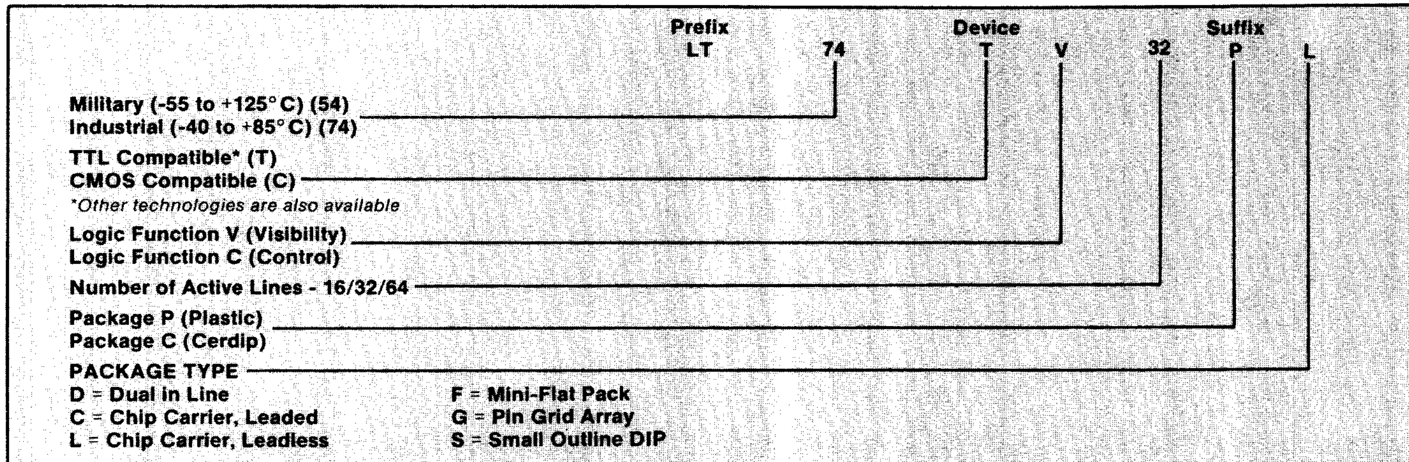
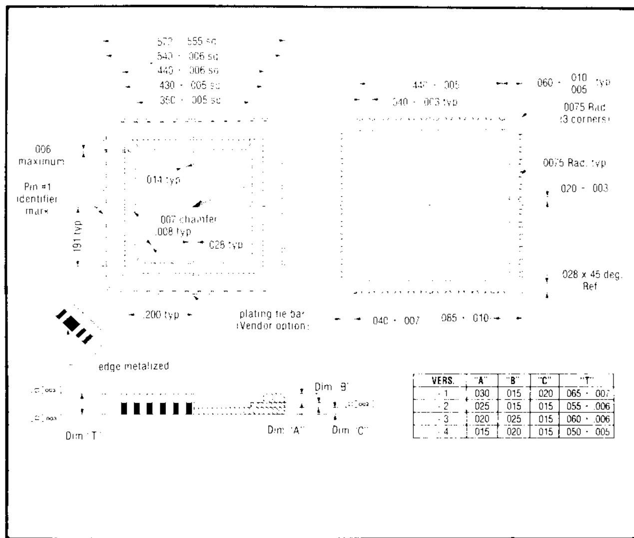
Detailed Characteristics and Specifications (cont.)

Part Numbering System



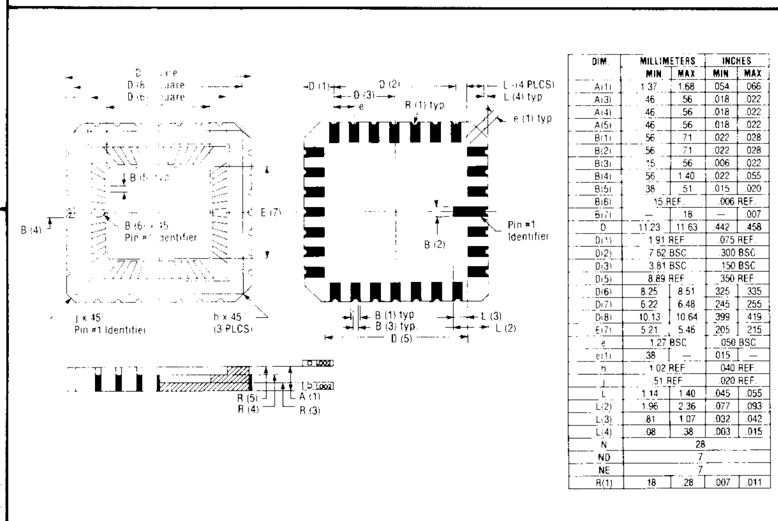
For more information in the economics, applications and package configurations available, contact LSTI or your nearest LSTI representative. We have management briefings, application seminars and workshops and schematic review services to help you get the most out of your testing process. Call us today!



VERS.	"A"	"B"	"C"	"T"
· 1	030	015	020	065 · 007
· 2	025	015	015	055 · .006
· 3	020	025	015	060 · .006
· 4	015	020	015	050 · 005

Note: Seal area and die attach area should be isolated from any lead (zero ground).

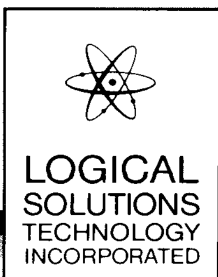
Figure 22
32 Point Circuit Dimensions



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A(1)	1 37	1.68	054	066
A(3)	46	56	.018	.022
A(4)	46	.56	.018	.022
A(5)	46	.56	.018	.022
B(1)	56	71	.022	028
B(2)	.56	71	.022	028
B(3)	15	56	.006	.022
B(4)	56	1 40	.022	.055
B(5)	38	51	.015	.020
B(6)	15 REF.		.006 REF.	
B(7)	—	18	—	.007
D	11.23	11 63	.442	.458
D(1)	1 91 REF		.075 REF.	
D(2)	7 62 BSC		.300 BSC	
D(3)	3.81 BSC		150 BSC	
D(5)	8.89 REF		350 REF	
D(6)	8.25	8 51	325	335
D(7)	6.22	6.48	245	255
D(8)	10.13	10.64	399	419
E(7)	5 21	5.46	205	215
e	1.27 BSC		.050 BSC	
e(1)	.38	—	015	—
h	1 02 REF		040 REF.	
j	.51 REF		.020 REF.	
L	1 14	1 40	.045	.055
L(2)	1.96	2.36	.077	.093
L(3)	.81	1 07	.032	.042
L(4)	.08	.38	.003	.015
N	28			
ND	7			
NE	7			
R(1)	18	.28	.007	.011

Figure 23
16 Point Circuit Dimensions

Notes:
1. Intended to meet MIL-M-38510 appendix C. C-4 outline and JEDEC MS-004 CC outline.
2. No lead to be electrically connected to the die attach pad or seal ring. Seal ring to be isolated from die attach pad.



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The Testability Company

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