# ProASIC3L Low-Power Flash FPGAs
## with Flash*Freeze Technology

FlashLock

## Features and Benefits

### Low Power
- Dramatic Reduction in Dynamic and Static Power Savings
- 1.2 V to 1.5 V Core and I/O Voltage Support for Low Power
- Low Power Consumption in Flash*Freeze Mode Allows for Instantaneous Entry to / Exit from Low-Power Flash*Freeze Mode
- Supports Single-Voltage System Operation
- Low-Impedance Switches

### High Capacity
- 250 k to 3 M System Gates
- Up to 504 kbits of True Dual-Port SRAM
- Up to 620 User I/Os

### Reprogrammable Flash Technology
- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Live-at-Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design when Powered Off

### High Performance
- 350 MHz (1.5 V systems) and 250 MHz (1.2 V systems) System Performance
- 3.3 V, 66 MHz, 66-Bit PCI (1.5 V systems) and 66 MHz, 32-Bit PCI (1.2 V systems)

### In-System Programming (ISP) and Security
- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE 1532–compliant)
- FlashLock® to Secure FPGA Contents

### High-Performance Routing Hierarchy
- Segmented, Hierarchical Routing and Clock Structure
- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

### Advanced and Pro (Professional) I/Os
- 700 Mbps DDR, LVDS-Capable I/Os
- 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—up to 8 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V / 1.2 V, 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, and M-LVDS
- Voltage-Referenced I/O Standards: GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II (A3PE3000L only)
- Wide Range Power Supply Voltage Support per JESD8-B, Allowing I/Os to Operate from 2.7 V to 3.6 V
- Wide Range Power Supply Voltage Support per JESD8-12, Allowing I/Os to Operate from 1.14 V to 1.575 V
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold-Sparing I/Os Programmable Output Slew Rate and Drive Strength
- Programmable Input Delay (A3PE3000L only)
- Schmitt Trigger Option on Single-Ended Inputs (A3PE3000L)
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the ProASIC®3L Family (except PQ208)

### Clock Conditioning Circuit (CCC) and PLL
- Six CCC Blocks, One with Integrated PLL (ProASIC3L) and All with Integrated PLL (ProASIC3EL)
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range 1.5 MHz to 250 MHz (1.2 V systems) and 350 MHz (1.5 V systems))

### SRAMs and FIFOs
- Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations available)
- True Dual-Port SRAM (except ×18)
- 24 SRAM and FIFO Configurations with Synchronous Operation:
  - 250 MHz: For 1.2 V systems
  - 350 MHz: For 1.5 V systems

### ARM® Processor Support in ProASIC3L FPGAs
- ARM Cortex™-M1 Soft Processor Available with or without Debug

*Table 1 •* **ProASIC3 Low-Power Product Family**

| ProASIC3L Devices | A3P250L | A3P600L | A3P1000L | A3PE3000L |
|---|---|---|---|---|
| ARM Cortex-M1 Devices [1] | | M1A3P600L | M1A3P1000L | M1A3PE3000L |
| System Gates | 250 k | 600 k | 1 M | 3 M |
| VersaTiles (D-flip-flops) | 6,144 | 13,824 | 24,576 | 75,264 |
| RAM kbits (1,024 bits) | 36 | 108 | 144 | 504 |
| 4,608-Bit Blocks | 8 | 24 | 32 | 112 |
| FlashROM Bits | 1 k | 1 k | 1 k | 1 k |
| Secure (AES) ISP [2] | Yes | Yes | Yes | Yes |
| Integrated PLL in CCCs [3] | 1 | 1 | 1 | 6 |
| VersaNet Globals | 18 | 18 | 18 | 18 |
| I/O Banks | 4 | 4 | 4 | 8 |
| Maximum User I/Os | 157 | 235 | 300 | 620 |
| Package Pins<br>VQFP<br>PQFP<br>FBGA | <br>VQ100<br>PQ208<br>FG144, FG256 | <br><br>PQ208<br>FG144, FG256, FG484 | <br><br>PQ208<br>FG144, FG256, FG484 | <br><br>PQ208 [3]<br>FG324, FG484, FG896 |

*Notes:*
1. *Refer to the Cortex-M1 product brief for more information.*
2. *AES is not available for ARM-enabled ProASIC3L devices.*
3. *For the A3PE3000L, the PQ208 package has six CCCs and two PLLs.*

# I/Os Per Package [1]

| ProASIC3L Low-Power Devices | A3P250L [2] | | A3P600L | | A3P1000L | | A3PE3000L | |
|---|---|---|---|---|---|---|---|---|
| ARM Cortex-M1 Devices | | | M1A3P600L | | M1A3P1000L | | M1A3PE3000L [3] | |
| | I/O Type | | | | | | | |
| Package | Single-Ended I/O [4] | Differential I/O Pairs | Single-Ended I/O [4] | Differential I/O Pairs | Single-Ended I/O [4] | Differential I/O Pairs | Single-Ended I/O [4] | Differential I/O Pairs |
| VQ100 | 68 | 13 | | – | – | – | – | – |
| PQ208 | 151 | 34 | 154 | 35 | 154 | 35 | 147 | 65 |
| FG144 | 97 | 24 | 97 | 25 | 97 | 25 | | |
| FG256 | 157 | 38 | 177 | 43 | 177 | 44 | – | – |
| FG324 | – | – | – | – | – | – | 221 | 110 |
| FG484 | – | – | 235 | 60 | 300 | 74 | 341 | 168 |
| FG896 | – | – | – | – | – | – | 620 | 310 |

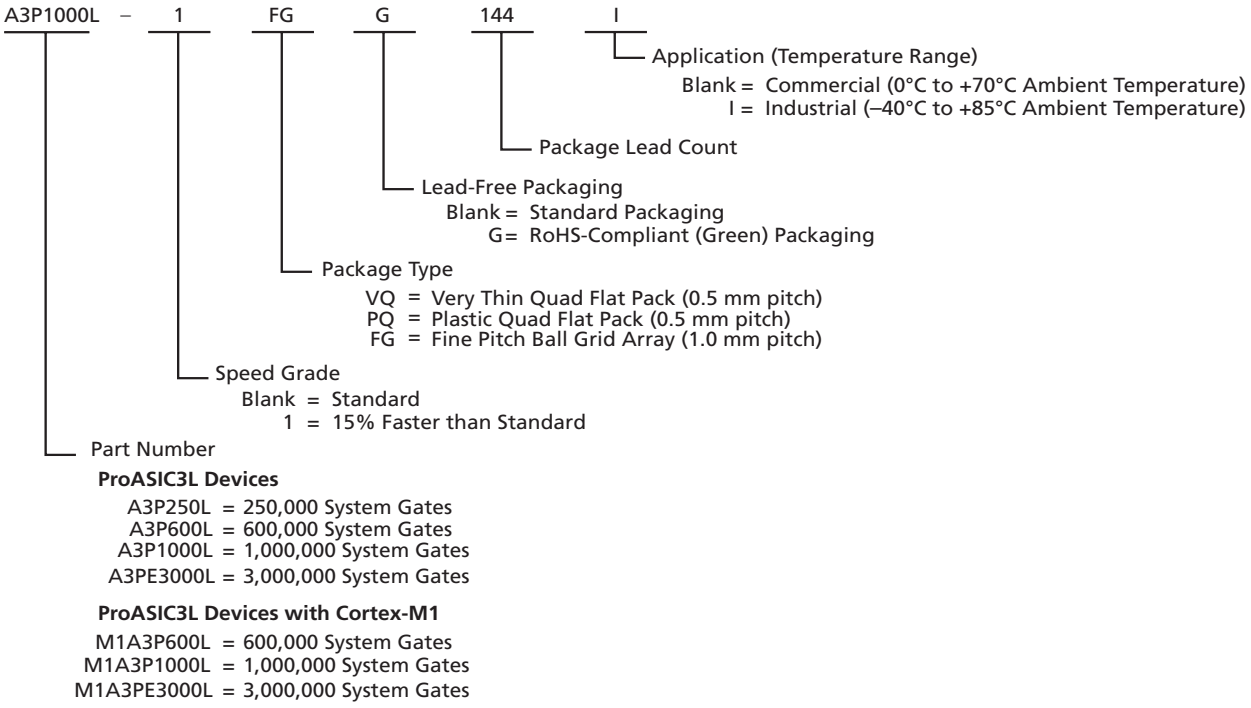
*Notes:*

1. *When considering migrating your design to a lower- or higher-density device, refer to the packaging section of the datasheet to ensure you are complying with design and board migration requirements.*
2. *For A3P250L devices, the maximum number of LVPECL pairs in east and west banks cannot exceed 15.*
3. *ARM Cortex-M1 support is TBD on this device.*
4. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
5. *FG256 and FG484 are footprint-compatible packages.*
6. *"G" indicates RoHS-compliant packages. Refer to "ProASIC3L Ordering Information" on page III for the location of the "G" in the part number.*
7. *For A3PE3000L devices, the usage of certain I/O standards is limited as follows:*
   *– SSTL3(I) and (II): up to 40 I/Os per north or south bank*
   *– LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank*
   *– SSTL2(I) and (II) / GTL+ 2.5 V/ GTL 2.5 V: up to 72 I/Os per north or south bank*
8. *When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not as a regular I/O, the number of single-ended user I/Os available is reduced by one.*

***Table 2 •*** **ProASIC3L FPGAs Package Sizes Dimensions**

| Package | VQ100 | PQ208 | FG144 | FG256 | FG324 | FG484 | FG896 |
|---|---|---|---|---|---|---|---|
| Length × Width (mm\mm) | 14 × 14 | 28 × 28 | 13 × 13 | 17 × 17 | 19 × 19 | 23 × 23 | 31 × 31 |
| Nominal Area ($mm^2$) | 196 | 784 | 169 | 289 | 361 | 529 | 961 |
| Pitch (mm) | 0.5 | 0.5 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| Height (mm) | 1.00 | 3.40 | 1.45 | 1.60 | 1.63 | 2.23 | 2.23 |

# ProASIC3L Ordering Information



## Temperature Grade Offerings

| Package | A3P250L | A3P600L | A3P1000L | A3PE3000L |
|---|---|---|---|---|
| **ARM Cortex-M1 Devices** | | **M1A3P600L** | **M1A3P1000L** | **M1A3PE3000L** |
| **VQ100** | C, I | – | – | |
| **PQ208** | C, I | C, I | C, I | C, I |
| **FG144** | C, I | C, I | C, I | |
| **FG256** | C, I | C, I | C, I | |
| **FG324** | – | – | – | C, I |
| **FG484** | – | C, I | C, I | C, I |
| **FG896** | – | – | – | C, I |

*Notes:*

1. *C = Commercial temperature range: 0°C to 70°C ambient temperature.*
2. *I = Industrial temperature range: –40°C to 85°C ambient temperature.*

## Speed Grade and Temperature Grade Matrix

| Temperature Grade | Std. | –1 |
|---|---|---|
| C [1] | ✓ | ✓ |
| I [2] | ✓ | ✓ |

*Notes:*

1. *C = Commercial temperature range: 0°C to 70°C ambient temperature.*
2. *I = Industrial temperature range: –40°C to 85°C ambient temperature.*

Contact your local Actel representative for device availability:
http://www.actel.com/contact/default.aspx.

# 1 – ProASIC3L Device Family Overview

## General Description

The ProASIC3L family of Actel flash FPGAs dramatically reduces dynamic power consumption by 40% and static power by 50%. These power savings are coupled with performance, density, true single-chip, 1.2 V to 1.5 V core and I/O operation as low as 1.2 V, reprogrammability, and advanced features.

Using Actel's proven Flash*Freeze technology enables users to shut off dynamic power instantaneously and switch the device to static mode without the need to switch off clocks or power supplies while retaining internal states of the device. This greatly simplifies power management on a board done through I/Os and clocks. In addition, optimized software tools using power-driven layout provide instant push-button power reduction.

Nonvolatile flash technology gives ProASIC3L devices the advantage of being a secure, low-power, single-chip solution that is live at power-up (LAPU). ProASIC3L offers dramatic dynamic power savings giving the FPGA users flexibility to combine low power with high performance.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC3L devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry (CCC) based on an integrated phase-locked loop (PLL). ProASIC3L devices support devices from 250 k system gates to 3 million system gates with up to 504 kbits of true dual-port SRAM and 620 user I/Os.

M1 ProASIC3L devices support the high-performance, 32-bit Cortex-M1 processor developed by ARM for implementation in FPGAs. ARM Cortex-M1 is a soft processor that is fully implemented in the FPGA fabric. It has a three-stage pipeline that offers a good balance between low-power consumption and speed when implemented in an M1 ProASIC3L device. The processor runs the ARMv6-M instruction set, has a configurable nested interrupt controller, and can be implemented with or without the debug block. ARM Cortex-M1 is available for free from Actel for use in M1 ProASIC3L FPGAs.

The ARM-enabled devices have Actel ordering numbers that begin with M1 and do not support AES decryption.

### Flash*Freeze Technology

The ProASIC3L devices offer Actel's proven Flash*Freeze technology, which allows instantaneous switching from an active state to a static state. ProASIC3L devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of ProASIC3L devices to support a wide range core voltage (1.2 V to 1.5 V) allows for an even greater reduction in power consumption, which enables low total system power.

When the ProASIC3L device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

The availability of low-power modes, combined with a reprogrammable, single-chip, single-voltage solution, make ProASIC3L devices suitable for low-power data transfer and manipulation in portable media, secure communications, radio applications as well as high performance portable, industrial, test, scientific, and medical applications.

## Flash Advantages

### Low Power

The ProASIC3L family of Actel flash-based FPGAs provide a low-power advantage, and when coupled with high performance, enables designers to make power-smart choices using a single-chip, reprogrammable, and live-at-power-up device.

ProASIC3L devices offer 40% dynamic power and 50% static power savings by reducing the core operating voltage to 1.2 V. In addition, the Power Driven Layout (PDL) feature in Libero® Integrated Design Environment (IDE) offers up to 30% additional power reduction. With Flash*Freeze technology, ProASIC3L is able to retain device SRAM and logic while dynamic power is reduced to a minimum, without the need to stop clock or power supplies. Combining these features provides a low-power, feature-rich and high-performance solution.

### Security

Nonvolatile, flash-based ProASIC3L devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC3L devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

ProASIC3L devices utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in ProASIC3L devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. ProASIC3L devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC3L devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed device cannot be read back, although secure design verification is possible.

Security, built into the FPGA fabric, is an inherent component of the ProASIC3L family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The ProASIC3L family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. A ProASIC3L device provides the most impenetrable security for programmable logic designs.

### Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based ProASIC3L FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

### Live at Power-Up

The Actel flash-based ProASIC3L devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based ProASIC3L devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the ProASIC3L device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC3L devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

### Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based ProASIC3L devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC3L family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC3L family a cost-effective ASIC replacement solution, manipulation in portable media and secure communications, radio applications as well as high performance portable Industrial, test, scientific and medical applications.

### Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of ProASIC3L flash-based FPGAs. Once it is programmed, the flash cell configuration element of ProASIC3L FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

## Advanced Flash Technology

The ProASIC3L family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with 7 layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

## Advanced Architecture

The proprietary ProASIC3L architecture provides granularity comparable to standard-cell ASICs. The ProASIC3L device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC3L core tile, as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable, allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of ProASIC3L devices via an IEEE 1532 JTAG interface.

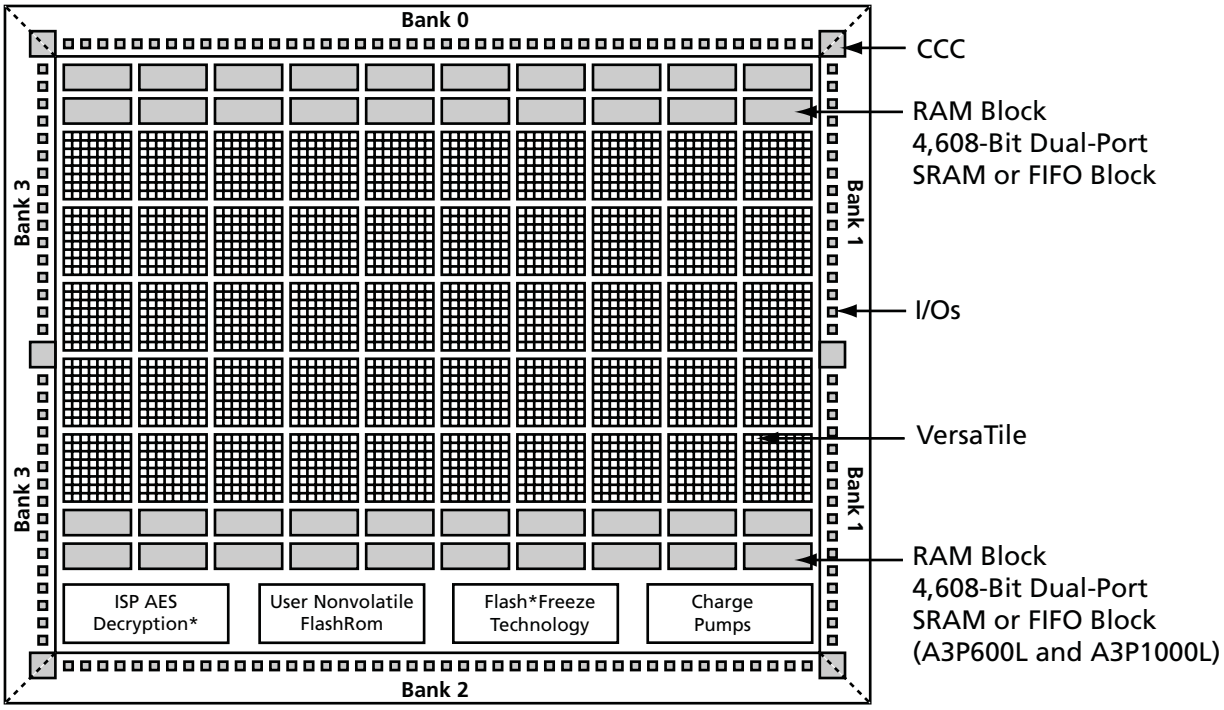



***Figure 1-1 •*** **ProASIC3L Device Architecture Overview with Four I/O Banks (A3P250L, A3P600L, and A3P1000L)**

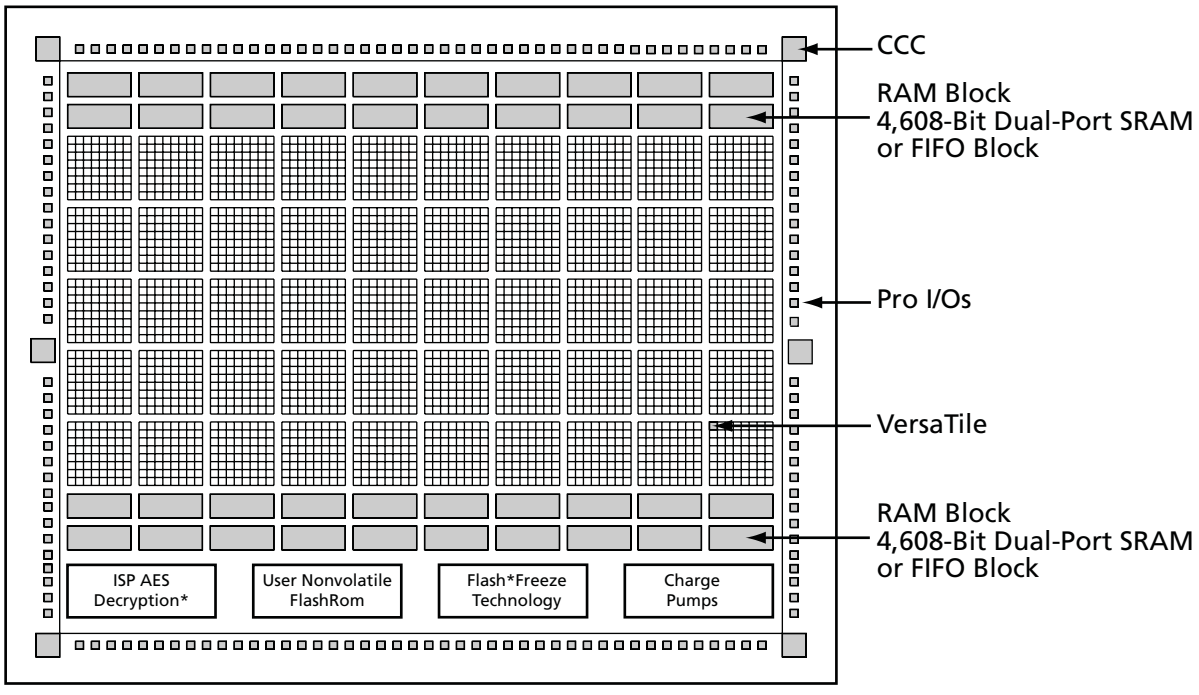



***Figure 1-2 •*** **ProASIC3EL Device Architecture Overview**

## Flash*Freeze Technology

The ProASIC3L devices offer Actel's proven Flash*Freeze technology, which enables designers to instantaneously shut off dynamic power consumption while retaining all SRAM and register information. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze (FF) pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption; clocks can still be driven or can be toggling without impact on power consumption; and the device retains all core registers, SRAM information, and states. I/O states are tristated during Flash*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL. Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The FF pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the FF pin as a regular I/O if Flash*Freeze mode usage is not planned, which is advantageous because of the inherent low-power static and dynamic capabilities of the ProASIC3L device. Refer to Figure 1-3 for an illustration of entering/exiting Flash*Freeze mode.

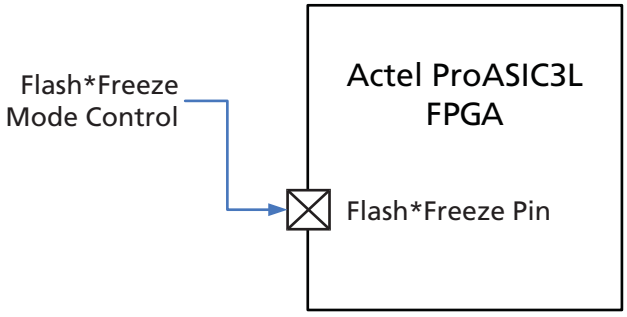



***Figure 1-3 •*** **ProASIC3L Flash*Freeze Mode**

### *VersaTiles*

The ProASIC3L core consists of VersaTiles, which have been enhanced beyond the ProASIC[PLUS]® core tiles. The ProASIC3L VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-4 for VersaTile configurations.

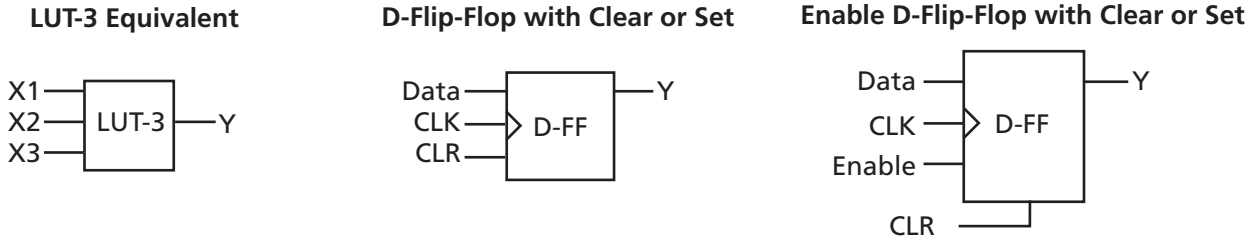



***Figure 1-4 •*** **VersaTile Configurations**

## User Nonvolatile FlashROM

Actel ProASIC3L devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet Protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3L IEEE 1532 JTAG programming interface.The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel ProASIC3L development software solutions, Libero IDE and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

## SRAM and FIFO

ProASIC3L devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

## PLL and CCC

ProASIC3L devices provide designers with flexible clock conditioning circuit (CCC) capabilities. Each member of the ProASIC3L family contains six CCCs. One CCC (center west side) has a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range ($f_{IN\_CCC}$) = 1.5 MHz up to 250 MHz
- Output frequency range ($f_{OUT\_CCC}$) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time is 300 µs
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / $f_{OUT\_CCC}$

### Global Clocking

ProASIC3L devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

#### I/Os with Advanced I/O Standards

The ProASIC3L family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V). ProASIC3L FPGAs support different I/O standards, including single-ended, differential, and voltage-referenced (ProASIC3EL only). The I/Os are organized into banks, with two, four, or eight (ProASIC3EL only) banks per device. The configuration of these banks determines the I/O standards supported. For ProASIC3EL, each I/O bank is subdivided into $V_{REF}$ minibanks, which are used by voltage-referenced I/Os. $V_{REF}$ minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common $V_{REF}$ line. Therefore, if any I/O in a given $V_{REF}$ minibank is configured as a $V_{REF}$ pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-data-rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-data-Rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II).

ProASIC3L banks support LVPECL, LVDS, B-LVDS, and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

## Wide Range I/O Support

Actel ProASIC3L devices support JEDEC-defined wide range I/O operation. ProASIC3L devices support both the JESD8-B specification, covering 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

# Part Number and Revision Date

Part Number 51700100-001-4
Revised February 2009

# List of Changes

The following table lists critical changes that were made in the current version of the document.

| Previous Version | Changes in Current Version (v1.3) | Page |
|---|---|---|
| v1.2 (February 2009) | The "I/Os Per Package [1]" table was revised to change the number of differential I/O pairs for A3PE3000L from 300 to 310. | II |
| | Table 2 · ProASIC3L FPGAs Package Sizes Dimensions is new. | II |
| v1.1 (July 2008) | The "Advanced and Pro (Professional) I/Os" section was revised to add two bullets regarding wide range power supply voltage support. | I |
| | 3.0 V wide range was added to the list of supported voltages in the "I/Os with Advanced I/O Standards" section. The "Wide Range I/O Support" section is new. | 1-7 |
| v1.0 (April 2008) | As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V. | N/A |
| 51700100-001-1 (April 2008) | This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview. | N/A |
| 51700100-001-0 (January 2008) | Reference to M1A3P250L was removed from Table 1 · ProASIC3 Low-Power Product Family, the "I/Os Per Package [1]" table, the "ProASIC3L Ordering Information" section, and the "Temperature Grade Offerings" table. The table note regarding M1A3P250L was removed from the "I/Os Per Package [1]" table. | I, II, III, IV |

# Datasheet Categories

### *Categories*

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advance," "Preliminary," and "Production." The definitions of these categories are as follows:

### *Product Brief*

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

### *Advance*

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

### *Preliminary*

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

### *Unmarked (production)*

This version contains information that is considered to be final.

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