2N6804 File Number **2217**

Avalanche-Energy-Rated P-Channel Power MOSFETs

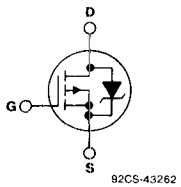
-11A, -100V
$r_{DS(on)}$ = 0.30Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

The 2N6804 is an advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. This is a p-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits

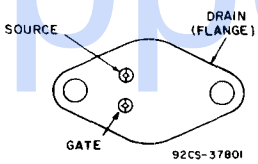
The 2N6804 is supplied in the JEDEC TO-204AA steel package.

TERMINAL DIAGRAM



P-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATION



JEDEC TO-204AA

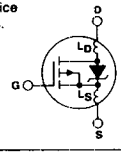
Absolute Maximum Ratings

Parameter		2N6804	Units
V_{DS}	Drain-Source Voltage	-100*	V
V_{DG}	Drain-Gate Voltage (R_{GS} = 20kΩ)	-100*	V
I_D @ T_C = 25°C	Continuous Drain Current	-11*	A
I_D @ T_C = 100°C	Continuous Drain Current	-7.0*	A
I_{DM}	Pulsed Drain Current ②	-50*	A
V_{GS}	Gate-Source Voltage	±20*	V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 14)	W
	Linear Derating Factor	0.6* (See Fig. 14)	W/°C
E_{AS}	Single Pulse Avalanche Energy ③	500	mJ
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55* to 150*	°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	−100*	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	−2.0*	—	−4.0*	V	V_{DS} = V_{GS}, I_D = −0.25mA
I_{GSS}	Gate-Source Leakage Forward	—	—	−100	nA	V_{GS} = −20V
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	−0.25*	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		—	—	−1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Drain Current ①	−11*	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = −10V
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	—	—	0.30	Ω	V_{GS} = −10V, I_D = −6.5A
g_{fs}	Forward Transconductance ①	2.0	3.7	—	S(℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = −6.5A
C_{iss}	Input Capacitance	400	500	—	pF	V_{GS} = 0V, V_{DS} = −25V, f = 1.0 MHz
C_{oss}	Output Capacitance	100	300	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	50	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	30	60	ns	V_{DD} = −35V, I_D = −7.0A, Z_o = 50Ω
t_r	Rise Time	—	70	140	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	—	70	140	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	—	70	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	25	45	nC	V_{GS} = −15V, I_D = −15A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	13	23	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	12	22	nC	
L_D	Internal Drain Inductance	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

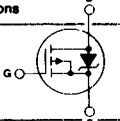


Thermal Resistance

$R_{\theta JC}$	Junction-to-Case	—	—	1.67*	°C/W	
$R_{\theta CS}$	Case-to-Sink	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
$R_{\theta JA}$	Junction-to-Ambient	—	—	30	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

Parameter		Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	−11*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ②	—	—	−50	A	
V_{SD}	Diode Forward Voltage ①	—	—	−1.5	V	T_C = 25°C, I_S = −11A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	—	—	250	ns	T_J = 25°C, I_F = −11A, dI_F/dt = −100 A/μs
Q_{RR}	Reverse Recovered Charge	—	1.8	—	μC	T_J = 25°C, I_F = −11A, dI_F/dt = −100 A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



*JEDEC Registered Value

① Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

② Repetitive Rating: Pulse width limited by max. junction temperature, See Transient Thermal Impedance Curve (Fig. 5).

③ V_{DD} = 25V, Starting T_J = 25°C, L = 6.2 mH, R_g = 25Ω, Peak I_L = 11 A, (See Fig. 15 and 16).

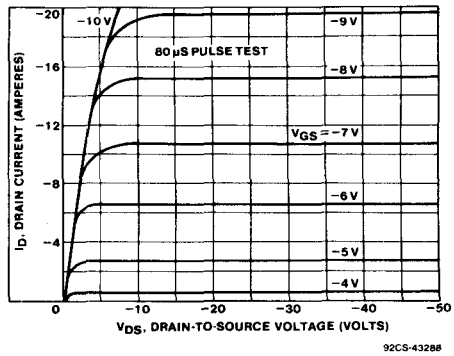


Fig. 1 - Typical Output Characteristics

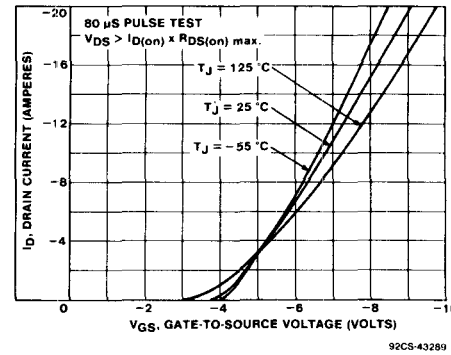


Fig. 2 - Typical Transfer Characteristics

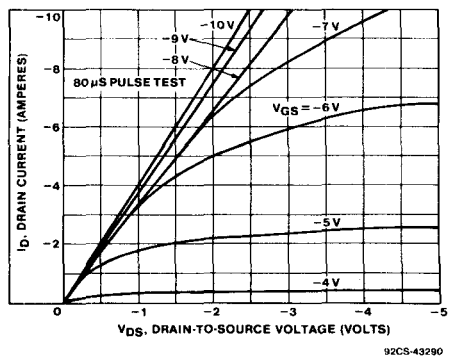


Fig. 3 - Typical saturation characteristic.

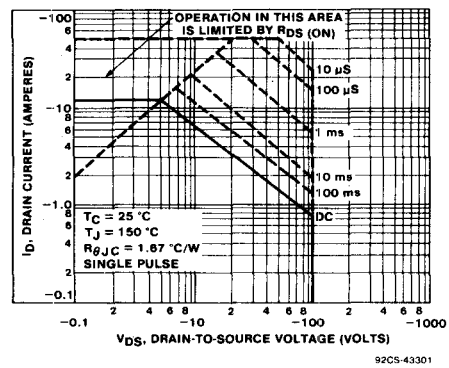


Fig. 4 - Maximum safe operating area.

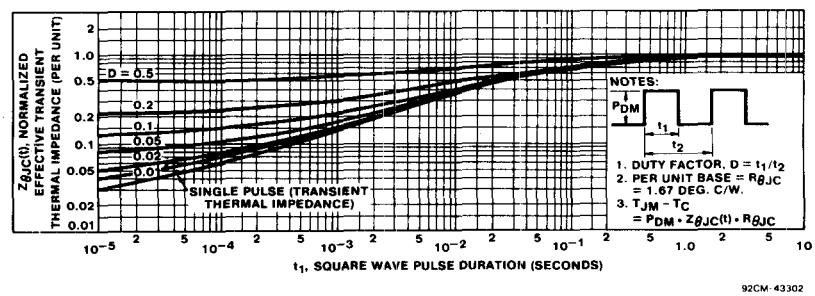


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

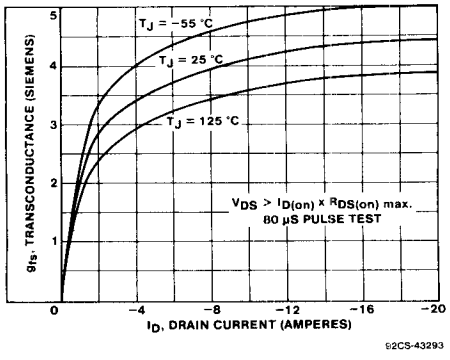


Fig. 6 - Typical transconductance vs. drain current.

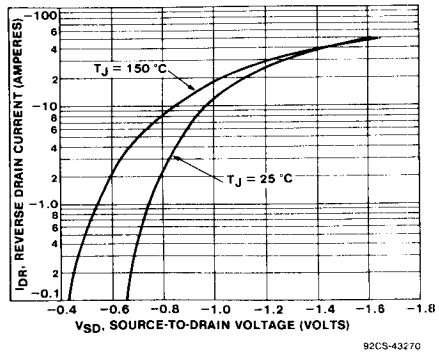


Fig. 7 - Typical source-drain diode forward voltage.

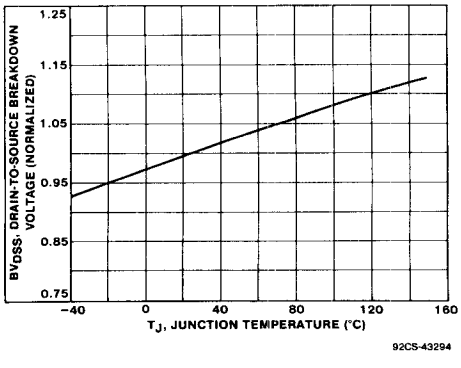


Fig. 8 - Breakdown voltage vs. temperature.

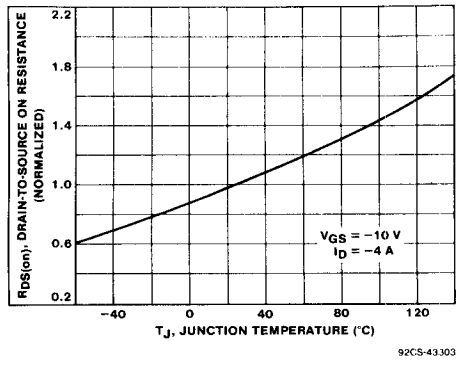


Fig. 9 - Normalized on-resistance vs. temperature.

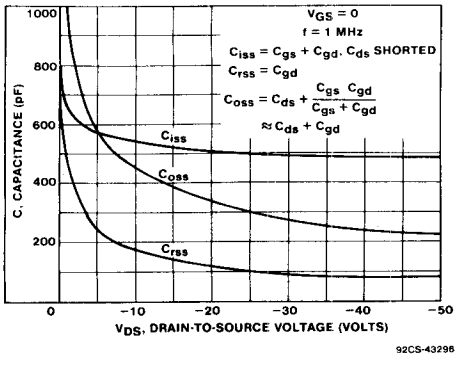


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

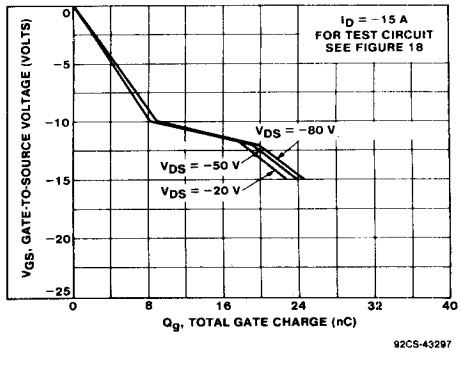


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

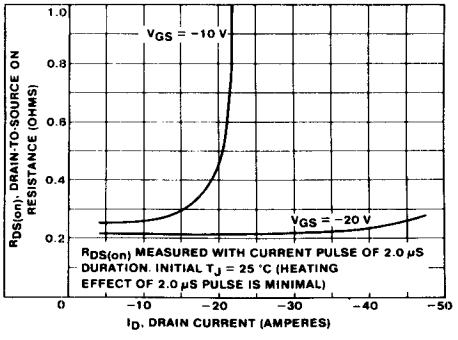


Fig. 12 - Typical on-resistance vs. drain current.

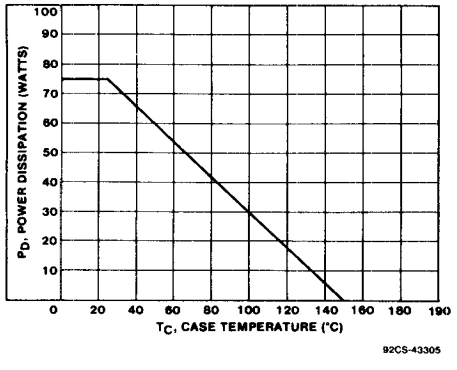


Fig. 14 - Power vs. temperature derating curve.

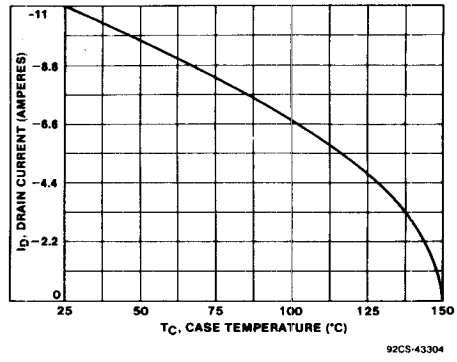


Fig. 13 - Maximum drain current vs. case temperature.

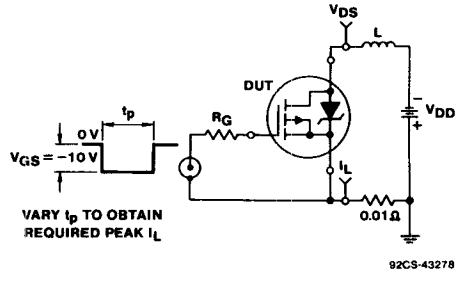


Fig. 15 - Unclamped inductive test circuit.

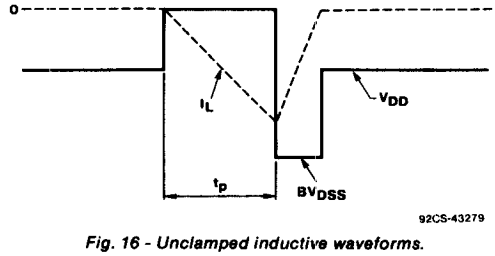


Fig. 16 - Unclamped inductive waveforms.

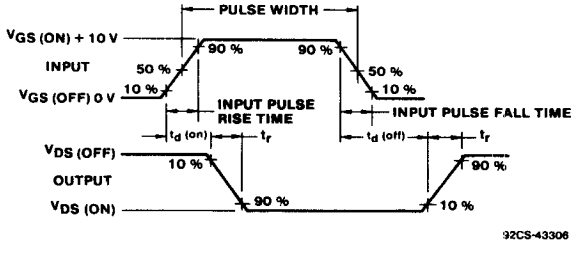


Fig. 17 - Switching time test circuit.

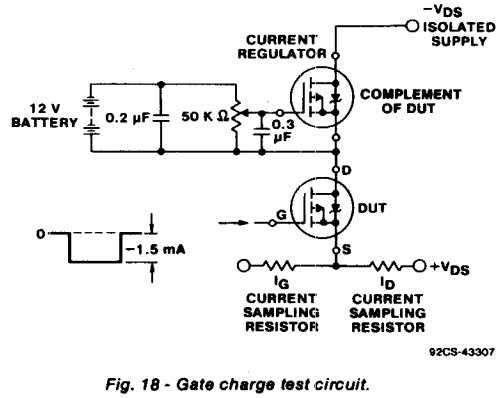


Fig. 18 - Gate charge test circuit.